BSTXCLX100

Programmable logic array circuit

Military Product Manual

Product overview

BSTXCLX100-1148 is a high-density programmable logic array circuit based on SRAM configuration.

Contains 1 92 rows × 64 columns, a total of 1 2,288 programmable logic blocks, 1 10,592 logic u nits, and 9 6 XtremeDSP Slice, 4 320K programmable Block RAM and programmable ports, DCM, P DCM and other modules. Can replace 1000000

It is suitable for applications with fixed digital logic circuits below the gate level and has high requirements on logic resources.

Product features

The BSTXCLX100-1148 combines the Advanced Silicon Wafer Combined Module (ASMBL) architecture with a wide range of flexible functions to greatly improve

It improves the programmable logic design capability, thus becoming a powerful product to replace ASIC technology. Energy logic application solution. BSTXCLX100-1148 has the following features:

- Xesium clock technology, including: Digital Clock Manager (DCM) block; additional phase-matched clock dividers
- (PMCD); Differential Global C lock;
- Xtreme DSP Slice technology, including: 1 8×18-bit signed multiplier with two’s complement function; optional pipeline stage Number; built-in accumulator (48 bits) and adder/subtractor;
- Smart RAM memory hierarchy technology, including: distributed RAM; dual-port 1 8Kb RAM blocks; optional pipeline stages

  Optional programmable FIFO logic automatically remaps RAM signals to FIFO

signals; high-speed memory interface support
Supports D DR SDRAM, D DR-2 SDRAM, Q DR-II a nd RLDRAM-II;

- SelectIO technology, including: 1.5V to 3.3VI/O operating voltage; built-in ChipSync source synchronization technology; digital Controlled Impedance (DCI) active termination; fine-grained I /O bank placement (configured in a bank);
- Flexible logic resources;
- Security chip AES bitstream encryption;
- 6 5 nm CMOS process;
- 1.2V core voltage;
- Flip chip packaging.