BSTTR28S12(F)

DC/DC Converter

Data Sheet

I. Product Introduction

BSTTR28S12(F) is a single-channel 12V/3.33A, 40W output. Manufactured using thick-film hybrid integrated circuit technology, it features a fully sealed metal housing and an input voltage range of 15V to 50V. It can withstand 80V, 1s surge voltages with minimal ripple voltage. It is used in DC power supply systems to implement DC voltage conversion.

II. Product Performance Indicators

The electrical characteristics shall be as specified in Table 1.

Table 1. Electrical characteristics

CHARACTERISTIC	SYMBOL	CONDITION (UNLESS OTHERWISE SPECIFIED, -55°C ≤ T_C ≤ 125°C, V_I = 28 V ± 0.5 V, C_L = 0.1 μF)	GROUP A GROUPING	LIMIT VALUE		UNIT
				MINIMUM	MAXIMUM	
Output voltage	V_O	V_I=15V~50V, I_O=3.33A	1	11.88	12.12	V
			2,3	11.70	12.30	
Output current	I_O	V_I=15V～50V	1,2,3	-	3.33	A
Output ripple voltage (peak-to-peak)	V_{RIP}	BW=6MHz, I_O=3.33A	1,2,3	-	60	mV
Voltage regulation	S_V	V_I=15V～50V, I_O=3.33A	1,2,3	-	20	mV
Current regulation	S_I	I_O=0A→3.33A	1,2,3	-	50	mV
Input current	I_I	No load, no termination to input ground	1,2,3	-	6	mA
		No load, open circuit prohibited		-	60	
Input ripple current (peak-to-peak)	I_{RIP}	BW=20MHz, I_O =3.33A	1,2,3	-	80	mA
Start threshold	V_{ION}	Full load, input voltage from 0V → 28V	1,2,3	11.0	14.8	V
Input undervoltage threshold [b]	V_{IOFF}	Full load, input voltage from 28V → 0V	1,2,3	11.0	14.5	V
Efficiency	η	I_O =3.33A	1,2,3	79	-	%
Insulation resistance	R_I	DC between the input and output or between any terminal (except terminals 7 and 8) and the housing, T_A =25℃	1	100	-	MΩ

CHARACTERISTIC	SYMBOL	CONDITION (UNLESS OTHERWISE SPECIFIED, -55℃ ≤ T_C ≤ 125℃, V_I = 28 V ± 0.5 V, C_L = 0.1 μF)	GROUP A GROUPING	LIMIT VALUE		UNIT
				MINIMUM	MAXIMUM	
Short-circuit power consumption	P_D	Output short circuit	1,2,3	-	8	W
Capacitive load [ab]	C_L	T_A =25℃	4	-	500	μF
Switching frequency	f_s	I_O =3.33A	4,5,6	400	550	kHz
External synchronization frequency range [b]	f_{SYNC}	I_O =3.33, pin 9 connected to TTL level, V_{IH} - V_{IL} =5V, duty cycle 20% to 80%	4,5,6	400	550	kHz
[bc] (peak value) during load transient	V_{LOR}	50% load → full load or full load → 50% load	4,5,6	-700	700	mV
Output voltage recovery time during load transients [bcd]	t_{LOR}	50% load → full load or full load → 50% load	4,5,6	-	500	μs
Output voltage change (peak value) when input voltage changes transiently	V_{VOR}	Input voltage V_I : 16V→40V, I_O =3.33A or Input voltage V_I : 40V→16V, I_O =3.33A	4,5,6	-900	900	mV
Output voltage [bde] recovery time when input voltage transient	t_{VOR}	Input voltage V_I : 16V→40V, I_O =3.33A or Input voltage V_I : 40V→16V, I_O =3.33A	4,5,6	-	900	μs
Start-up overshoot [b] (peak value)	V_{TO}	Input voltage V_I : 0V→28V, I_O =3.33A	4,5,6	-	50	mV
Start delay [bf]	t_{TR}	Input voltage V_I : 0V→28V, I_O =3.33A	4,5,6	-	20	ms

a. Capacitive load can be any value between 0 and the maximum limit value without affecting the DC parameters;
b. This parameter is guaranteed by design and is only tested during the initial quality consistency inspection or when the design or process is changed;
c. The load transition time should be greater than 10 μs;
d. Recovery time refers to the time from the start of the jump until the output voltage returns to the corresponding stable value within ±1%;
e. The transition time of the input voltage should be greater than 10 μs;
f. can be calculated from the start of the power supply jump or from the disconnection of the grounded inhibit terminal.

III. Appearance and Size

The outer shape of the housing shall be as specified in Figure 1.

Unit is millimeter

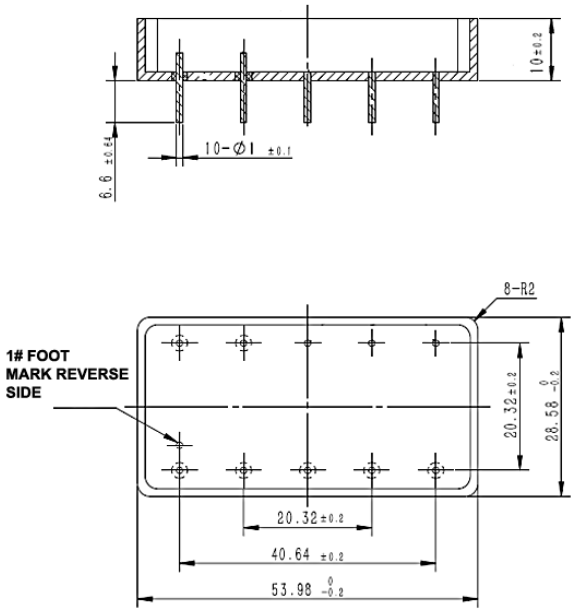

Figure 1a. BSTTR28S12 dimensions

Unit is millimeter

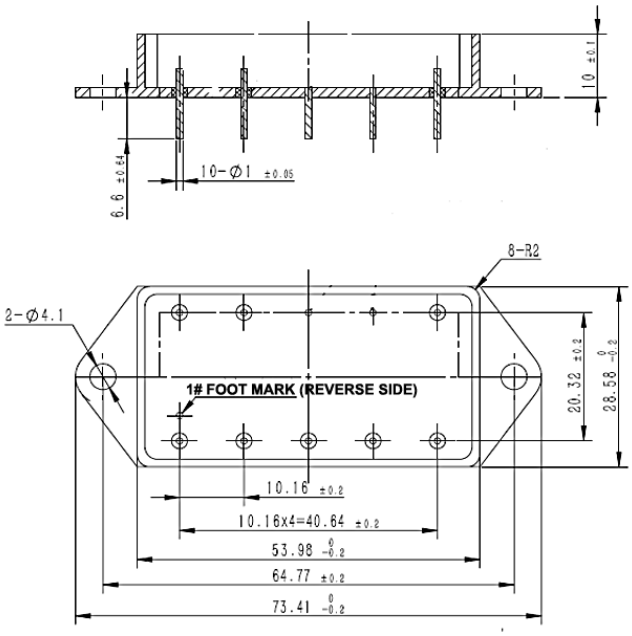

Figure 1b. BSTTR28S12F dimensions

IV. Pin Function Description

The terminal arrangement should comply with the requirements of Figure 2.

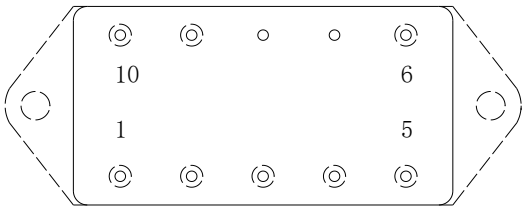

Figure 2. Terminal arrangement (top view)

Table 2

PIN NUMBER	SYMB2OL	FUNCTION	PIN NUMBER	SYMBOL	FUNCTION
1	VI	Positive input	6	SEN+	Positive sensing terminal
2	INH	Prohibited End	7	CASE	Shell
3	SEN-	Negative sensing terminal	8	CASE	Shell
4	GND_O	Output	9	SYN	Synchronous end
5	V_O	Output	10	GND_I	Input

V. Typical Application Diagram

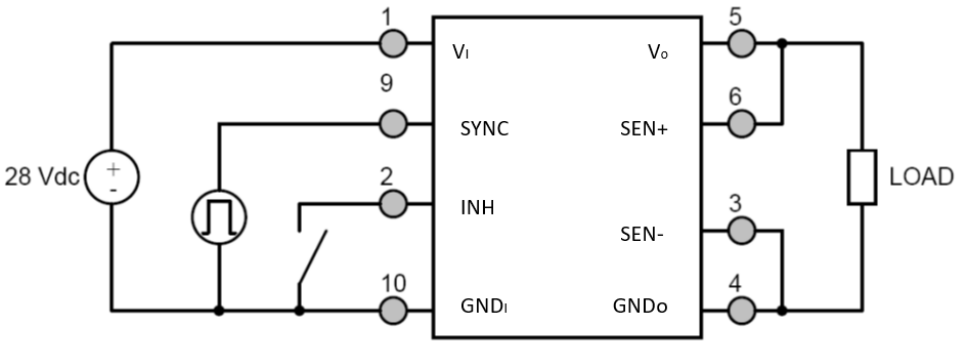

Figure 3. Typical application diagram

VI. Application Description

6.1. Trim Function Application Description

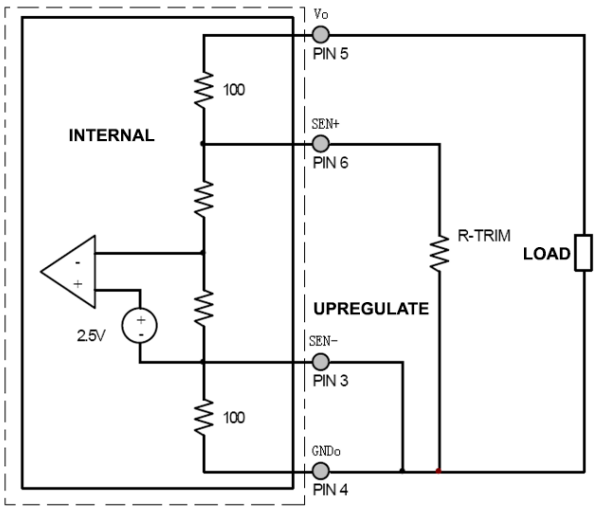

Figure 4. External connection diagram

The output voltage can be increased by external connection: pin 3 SEN- and pin 4 GND $_O$ Short-circuit, connect the 6-pin SEN+ to a regulating resistor R-TRIM and connect it to the pin 4 GND$_O$.

The relationship between the adjustment resistor R-TRIM (KΩ) and the output voltage V_O (V) is as follows.

$$Vo = \frac{1.21}{R\text{-}TRIM} + 12.1$$

Table 2. Relationship between trim resistor ($R_{\text{-}TRIM}$) and output voltage V_O

R-TRIM(KΩ)	—	270	41.76	7.18	4.54	3.34	2.66
V_O(V)	12.0	12.10	12.20	12.30	12.40	12.50	12.60
R-TRIM(KΩ)	2.18	1.86	1.62	1.43	1.34	1.20	1.09
V_O (V)	12.70	12.80	12.90	13.00	13.10	13.20	13.30

6.2. SENSE Function Application Description

When the load current is high, a voltage drop occurs in the wires between the DC/DC converter output and the load, causing a drop in the actual voltage across the load RL. Therefore, during normal operation, SEN+ must be connected to the positive voltage terminal of the load RL (i.e., Vo on the DC/DC converter), and SEN- must be connected to the negative voltage terminal of

the load RL (i.e., GNDo on the DC/DC converter) as a load voltage sensing port (see Figure 5). This ensures that the load RL receives the nominal output voltage. Failure to connect these terminals or connecting them incorrectly can cause permanent damage to the power module.

It is important to note that if the wires from SEN+ and SEN- to the load are too long, it may cause self-excitation. If the wires are too long, you can directly connect SEN- to GNDo at the module end.

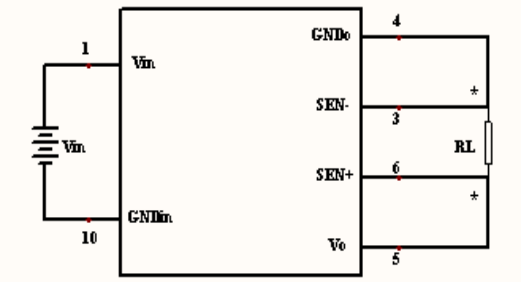

Figure 5. Schematic diagram of SENSE terminal wiring

6.3. Application Instructions for the Disable Terminal Function

(When the disable function is not used, leave the disable terminal unconnected)

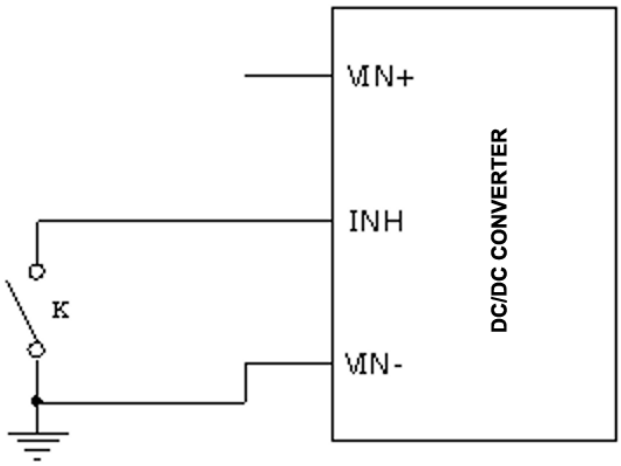

Figure 6. Schematic diagram of prohibit terminal wiring

6.4. Power-on Sequence Description

If an external synchronization signal is required, first input the TTL signal and then input 28V. Refer to Figure 3 for the typical application diagram for wiring diagram.

VII. Notes

- Prevent product collision;
- The glass insulators that protect the pins are prohibited from bending or hitting the pins. Products with flanges should be fixed to the structural parts before welding the lead pins;
- Do not connect the power supply polarity in reverse and pay attention to the input voltage range;
- A heat sink should be installed to ensure that the shell temperature is lower than the maximum operating temperature specified for the product;
- Pay attention to the “1” foot mark" and install the board and weld it in the correct installation direction;
- The lead welding temperature should be less than 300℃, and the welding time should not exceed 10 seconds.