

Qiyao cost-effective series

BSTSW300T type FPGA

Product manual

I. Product Overview

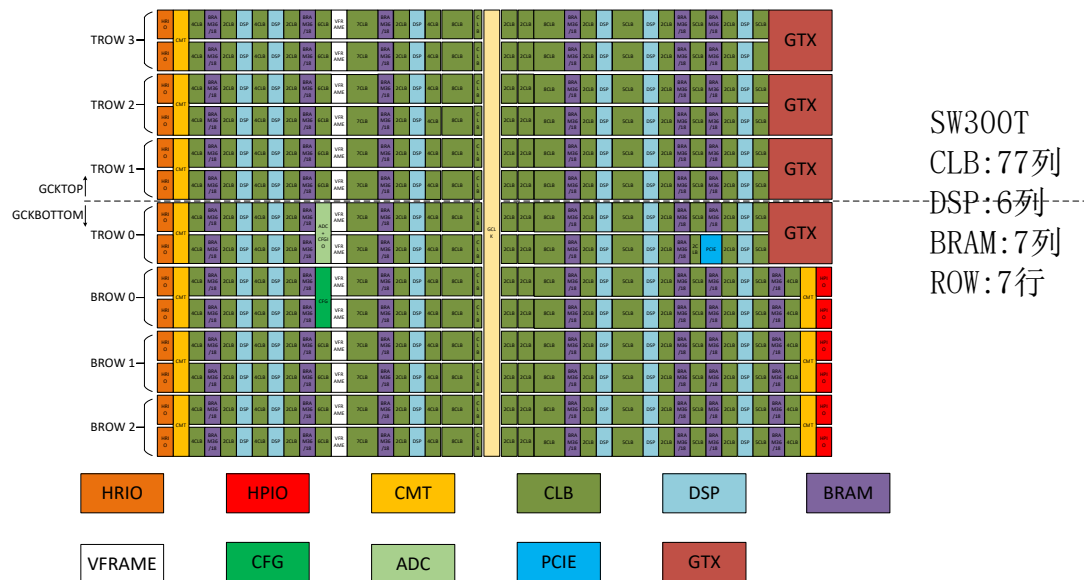
The BSTSW300T type FPGA is benchmarked against the XC7K325T and is a SRAM type FPGA. Logic resources include 6-input LUT CLB, high-performance user IO module, Block RAM with a single block capacity of 36k bits, digital signal processing module DSP, clock management module CMT, ADC module, PCIe module, high-speed serial interface SERDES module, configuration Modules and interconnect resources, etc.

II. Main Features

- The logic implementation is based on a 6-input lookup table (can be configured as distributed RAM);
- The on-chip data cache block RAM has a single block capacity of 36 Kb, dual- port mode , and built-in FI FO ;
- User IO can support multiple level standards such as single-ended LVCMOS and LVTTTL, and supports multiple differential level standards. The high-performance IO (HPIO) voltage range supports 1.2V~1.8V and wide-range IO (HRIO) The voltage range supports 1.2V~ 3.3V;
- high-performance user IO interface supports DDR3, with a maximum rate of 1 600 M b/s;
- DSP module contains a 25×18 multiplier, 48 -bit accumulator and pre- adder, which can be used for high-performance filtering algorithms, such as optimal symmetric coefficient filtering;
- High-precision low-jitter clock management unit (CMT), including phase-locked loop (PLL) and mixed-mode clock management (MMCM) . The maximum input frequency of the clock management module can reach 933MHz (speed grade - 1 devices can reach up to 800MHz) ;
- Global clock tree frequency up to 710 MHz (up to 625 MHz for speed grade -1 devices);
- High-speed serial interface SERDES module, line rate from 5 00M b/s to up to 10.3125 G b/s (speed grade -1 device up to 8 G b/s , speed grade-2 device within the device junction temperature range of 0 ~ 85 °C Up to 10.3125 G b/s);
- Integrated PCIe hard core, supports Gen2 x8 ;
- Integrated 12-bit 1 MSPS ADC for on-chip temperature and voltage sensor monitoring;
- Supports multiple configuration modes, including support for universal memory interface and 256-bit AES encryption.

III. Functional Block

BSTSW 3 00T architecture block diagram is as follows:



Picture 1 -1BSTSW300T chip architecture detailed arrangement