Qiyan low power series
BSTSL100T FPGA
Product Brochure

Product Overview

BSTSL100T FPGA is a SRAM FPGA that is comparable to XC7A100T . Its logic resources include CLB with 6-input LUT, high-performance user IO module, single-block Block RAM with a capacity of 36k bits, signal processing module DSP, clock management module CMT, ADC module, PCIe module, high-speed serial interface SERDES module, configuration module and interconnection resources.

Product features

- The logic implementation is based on a 6-input lookup table (which can be configured as a distributed RAM);
- chip data cache RAM has a single block capacity of 36 Kb , dual- port mode , and built-in FIFO logic function ;
- Wide range user IO can support multiple level standards such as single-ended LVCMOS, LVTTL, and multiple differential level standards, and the voltage range supports 1.2V~3.3V;
- High-speed user IO interface supports DDR3, with a maximum rate of up to 800 Mb /s ;
- DSP module contains 25 × 18 multipliers, 48 -bit accumulators and pre-adders, which can be used for high-performance filtering algorithms such as optimal symmetric coefficient filtering ;
- High-precision low-jitter clock management unit (CMT) , including phase-locked loop (PLL) and mixed-mode clock management (MMCM) , the clock management module has a maximum input frequency of up to 800MHz
- global clock tree frequency can reach up to 464 MHz ;
- speed serial interface SERDES module, line rate from 500M b/s to a maximum of 3.75 G b /s ;
- Integrated PCI e hard core , supports Gen2 ;

- Integrated 12-bit 1 MSPS ADC for on-chip temperature and voltage sensor monitoring ;
- Supports multiple configuration modes , including support for universal memory interface and 256-bit AES encryption.

Table 1 BSTSL100T product contains internal resources

Resource Item	BSTSL100T			
	FG256 package	CS324 package	F G484 package	F G676 package
Equivalent logic unit number	101440			
Number of Slices	15850			
C LB constitutes distributed RAM (Kb)	1188			
Number of DSPs	240			
Number of BRAMs	270 (single BRAM capacity 18K b) 135 (single BRAM capacity 36 Kb)			
Maximum BRAM capacity (Kb)	4860			
CMT quantity	6			
Number of ADCs	1			
PCIE quantity	0	0	1	1
High-speed interface SERDES channel number	0	0	4	8
Wide range of user IO quantity	1 70	210	2 85	3 00

Functional Block Diagram

the BSTSL100T FPGA is as follows:

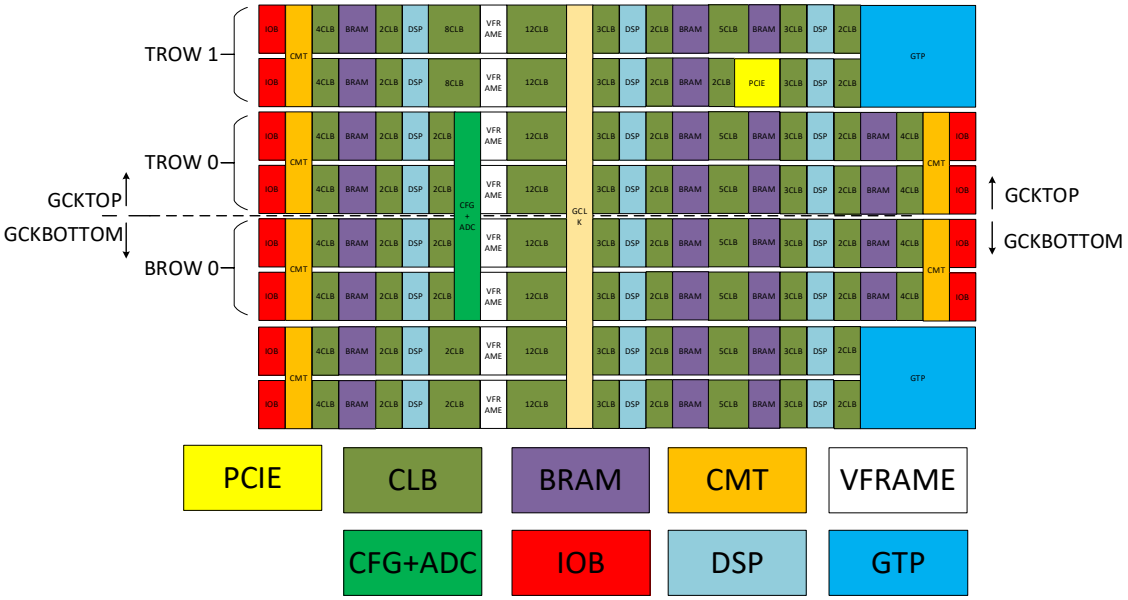

Figure1 Detailed layout of BSTSL100T chip architecture