BSTRTAX1000-CQ352 1 million gate antifuse

FPGA Aerospace Product Manual

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Product Introduction

Product Overview

BSTRTAX1000-CQ352 is a radiation-hardened 1 million-gate MTM (Metal-To-Metal) anti-fuse FPGA. The circuit is mainly composed of programmable logic modules (C units and R units), on-chip RAM/FIFO, charge pump, high-voltage programming circuit, JTAG configuration circuit module, I/O port circuit, clock routing network, testability

circuit module and other modules. The system gate count of BSTRTAX1000-CQ352 is 1,000,000 gates. The logic units inside the device: 6048 register units (R-Cell, radiation-resistant triple-mode redundancy) and 12096 combinational units (C-Cell). Users can interconnect and configure the logic units by programming anti-fuses to achieve specific logic functions. There are 198 user-configurable I/O ports distributed around the device, which can be configured as input, output, high-impedance, and bidirectional modes. At the same time, the device contains rich clock resources, a large amount of test logic and specific encryption logic. Users can test the circuit through JTAG test logic and encrypt the circuit by burning encryption anti-fuse.

Product Features

- Equivalent system integrated gate count: 1 million gates
- Combinational logic C unit: 12096
- Sequential logic R unit: 6048 (radiation-resistant triple-mode redundancy)
- On-chip RAM capacity: 162Kbits
- Clock resources: 8
- CQ352 package I/O quantity: 198
- Core operating voltage VCCA: 1.5V
- I/O voltage VCCI: 3.3V/2.5V/1.8V/1.5V
- Differential I/O voltage VCCDA: 3.3V/2.5V
- Available differential ports: 196 (Pin 34303P andPin 86193P is not paired, the rest can be used for differential ports)
- Maximum system operating frequency: 350MHz
- Maximum quiescent current: 450mA (125℃)
- Package: CQFP352

- Total radiation dose (TID): ≥ 150k rad (Si)
- Single event latch-up threshold (SEL): ≥75MeV•cm2/mg
- Single event upset rate:
  - Block RAM (with EDAC turned on and timer 2MHz refresh) ≤10-10 errors/bit·day,
  - Flip-flop logic unit ≤ 10-10 errors/bit·day
- Single event upset threshold (SEU): ≥ 13MeV•cm2/mg (Block RAM with EDAC turned on and timer 2MHz refresh)
- Working temperature: -55℃～+125℃
- ESD: ≥2000V

This product does not use new materials and new processes.

Product use and application range

This product is a radiation-resistant anti-fuse FPGA, a programmable logic device that allows users to customize complex digital processing and control functions through programming. This product is widely used in radiation environments such as industrial control, military, and aerospace.

Benchmarking against foreign products

Benchmarking against Actel's BSTRTAX1000-CQ352 circuit, it can replace BSTRTAX1000-CQ352 in situ, and its functions and main performance indicators are consistent with those of foreign samples, and they are compatible. At the same time, it can replace the AX1000-CQ352 circuit.

Product appearance

Product size

The device shape is in accordance with GB/T 7092-1993, using 0.50mm pitch 352 lead ceramic quad flat (CQFP352) package, the specific dimensions are shown in the figure below:

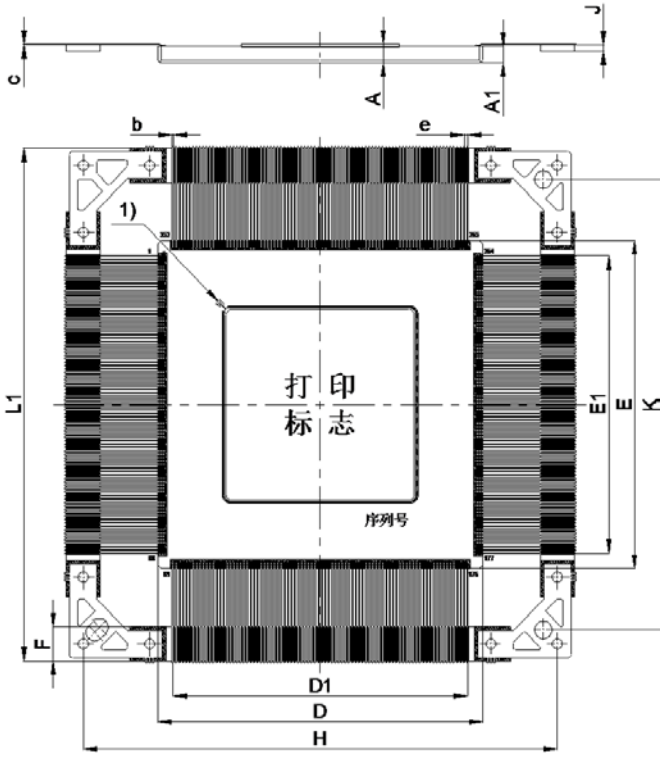


Figure 1. Dimensions

Table 1. Dimensions

Dimension symbols	Value, unit: mm		
	Minimum	Nominal	maximum
A	2.47	2.75	3.03
A1	2.07	2.30	2.53
b	0.15	0.20	0.25
c	0.10	0.15	0.20
D (E)	47.80	48.00	48.20

D1 (E1)	-	43.51	-
e	-	0.50	-
F	4.87	5.00	5.13
H	69.80	70.00	70.20
J	0.77	0.90	1.03
K	65.70	65.90	66.10
L1	74.70	75.00	75.30

Weight

Weight of CQFP352 packaged device: 26g±2g (with lead frame); 22±1g (without lead frame).

Packaging process

The device is manufactured using radiation-resistant MTM anti-fuse 0.13μm 1P7M process. The circuit integration scale is 1,000,000 gates and the chip area is 13.2mm×14.3mm.

The shell base is made of alumina ceramics, the cover is made of kovar, and the shell coating thickness and related conditions meet the requirements of GJB 1420B-2011. The lead material and coating meet the requirements of 3.5.3 and 3.6.3 of Q/QJA 20084A-2017.

The lead material is kovar alloy, the surface is plated with nickel-gold, the thickness of the nickel layer is (2.54~8.90) μm, the outermost coating material is gold, and the thickness of the gold plating layer is (1.5~5.7) μm.

The device is mounted using the JM7000 conductive adhesive bonding process; the bonding uses the Φ31.75μm silicon-aluminum wire ultrasonic bonding process; the cap is sealed using alloy melting, and the cover is grounded; the marking uses the metal ink pad printing process.

Product logo descriptions

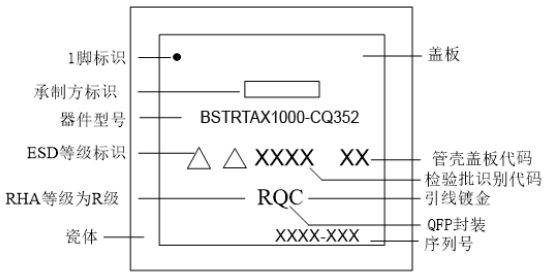


Figure 2: Device photos and logos

Standard Implementation

This productThe quality level is implemented according to the B level specified in GJB 597B-2012, and meets the YC quality level assurance requirements specified in Q/QJA 20084/553-2022 (WS). The products meet the requirements of GJB 597B-2012 "General Specification for Semiconductor Integrated Circuits" and GJB 548B "Test Methods and Procedures for Microelectronic Devices".

Brief description of basic working principle

Circuit Function Block Diagram

The device is an MTM anti-fuse FPGA. The device is mainly composed of programmable logic modules (C, R units), Block RAM modules, charge pump modules, high-voltage programming modules, I/O port modules, clock routing networks, JTAG configuration test modules and other built-in test modules. The overall main structure includes 8 I/O Bank and 3×3 CoreTiles. Each CoreTile includes 4 4608-bit Block RAMs. The functional block diagram of the anti-fuse FPGA chip is shown below.

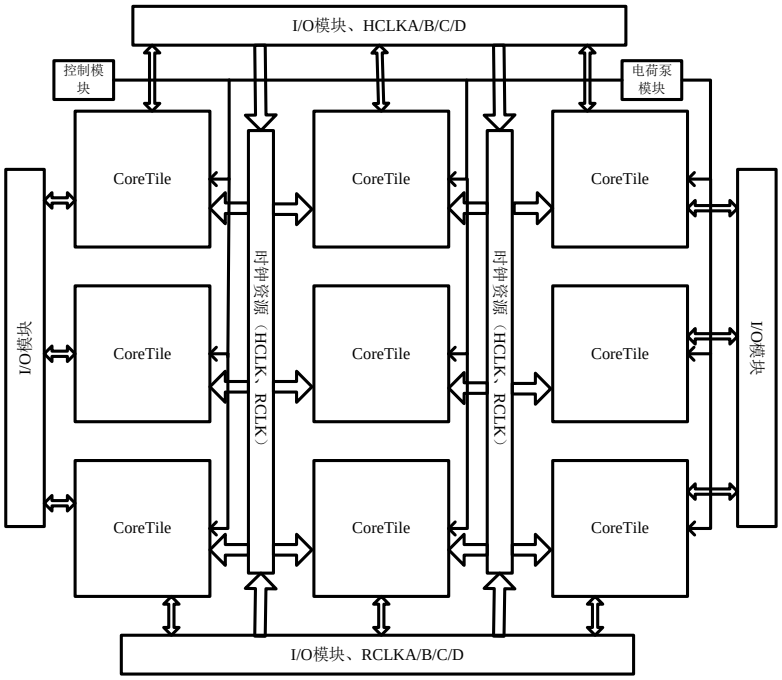


Figure 3. Functional Block Diagram

This product is an anti-fuse FPGA circuit. Through programming and configuration, users can realize customized functions. Anti-fuse FPGA products can be configured so that some key modules can realize different functions according to the configuration.

Package and pin description

The device adopts CQFP352 package. The package dimensions, pin arrangement and definition are shown in Appendix A.

I/O Ports

I/O Port Overview

- Maximum number of I/Os available to users of BSTRTAX1000 circuit: 418(Total number in the circuit), the number of I/Os packaged by CQ352: 198.
- Available differential ports: When using differential ports, paired I/O ports are required, and the two paired ports need to be located adjacent to each other.

For example, IO02N and IO02P form a differential pair, and IO04N and IO04P form a differential pair. When not configured as differential pairs, these I/O ports can be used independently as normal ports.

- High impedance state of I/O ports

Table 2. I/O port high impedance state

I/O Ports	state	Is it high impedance?
Used I/O	Power on	It is in high impedance state before reaching the set state
	Power off	High impedance
Unused I/O	Power on	High impedance
	Power off	High impedance

In Microsemi Designer software, unused I/Os are configured as high-impedance without pull-up resistors by default. If no special settings are made, unused I/Os are configured as high-impedance by default.

Power port:

GND Ground

VCCA core supply voltage (1.5V)

VCCIBx port supply voltage

I/O supply voltage. Bx is the ID of the I/O block, from 0 to 7. VCCIBx of unused I/O blocks can be connected to ground or to other used I/O VCCIBx blocks in the chip.

VCCDA differential supply voltage

Supply voltage for differential I/O ports, JTAG, and diagnostic interfaces. VCCDA can be 3.3V or 2.5V, but when using reference voltage or differential ports,

VCCDA must be connected to 3.3V. In addition, VCCDA must be greater than or equal to any VCCI voltage.

VPUMP External charge pump voltage

The external supply voltage used to drive the charge pump is used to control the isolation transistor in the logic module. There is also a charge pump inside. The current of the charge pump driven by the external voltage is smaller than that of the internal charge pump. The VPUMP current is included in ICCDA. Therefore, ICCDA will be smaller when the user uses an external voltage to drive the charge pump.

When using an external charge pump, VPUMP must be 3.3 V to 3.6 V. When using the internal charge pump, VCCA must be powered up and VPUMP can be connected directly to ground or through a 1k resistor.

There is no power-on sequence requirement for VPUMP. If VPUMP is powered on before VCCA, the chip is initialized by the external charge pump. If VPUMP is powered on after VCCA, the chip is initialized by the internal charge pump first, and then powered by the external VPUMP when VPUMP reaches 3.3V.

User configurable pins

VREF

Reference level of I/O Bank. Users can configure regular I/O pins as VREF pins. The location of VREF is not fixed. There can be one or more VREFs in an I/O bank. Users do not need to specify VREF pins for OUTBUF and TRIBUF. Only input and bidirectional I/O require VREF pins.

Global clock port:

HCLKA/B/C/D dedicated hard-wire clock A, B, C, D

These pins are the input clocks for the sequential circuits. The input levels are compatible with all supported I/O standards (differential I/O level standards have a pair of P/N pins). These inputs are directly connected to each R unit, and the clock speed is not affected by the number of driven R units. The HCLK pins can be used as HCLK inputs or user I/O. If the above functions are not used, it is recommended to connect them to a known state.

CLKE/F/G/H Global clock E, F, G, H

These pins are the clock input ports in the clock distribution network. The input level is compatible with all supported I/O standards (differential I/O level standards have a pair of P/N pins). The input clock drives the R unit after passing through the buffer. The CLK pin can be used as a clock input or user I/O. If the above functions are not used, it is recommended to connect them to a known state.

JTAG and monitoring port:

PRA/B/C/D Probes A, B, C, D

Dedicated probe pins are used to output any user defined design node within the chip. These independent diagnostic pins can be used to allow real-time diagnostic output of any signal path within the device. The pin's probe function can be permanently disabled to protect the confidentiality of the programmed design.

TCK test clock

Test clock input for JTAG boundary-scan testing and diagnostic probes.

TDI test data input

Serial input for JTAG boundary scan test and diagnostic probe. The TDI port has an internal 10kΩ pull-up resistor.

TDO test data output

Serial output for JTAG boundary scan testing.

TMS test mode selection

The TMS pin controls the IEEE 1149.1 boundary scan pins (TCK, TDI, TDO, TRST). The TMS port has an internal 10kΩ pull-up resistor.

TRST boundary scan reset pin

The TRST pin is an active low input port used to asynchronously initialize or reset the boundary scan circuit. TRST is equipped with a programmable 10kΩ pull-up resistor. This pin must be connected to ground for normal operation.

NC floating pin

These pins are not connected to other pins in the chip or package. These pins can be driven to any voltage or left floating without affecting the operation of the chip.

User configurable I/O ports

BSTRTAX1000-CQ352 has a flexible I/O structure, supports a range of mixed voltages (1.5V, 1.8V, 2.5V and 3.3V) and can select I/O blocks. The I/O level standards supported by BSTRTAX1000-CQ352 are shown in Table 3.

The unused I/O configurations are as follows:

- Disable output buffer (high impedance state)

- Disable input buffer (high impedance state)
- No pull-up and pull-down resistors are used

In Microsemi Designer software, unused I/Os are configured by default as high-impedance without pull-up or pull-down resistors.

Each I/O's slew rate, drive strength, weak pull-up and weak pull-down circuits can be programmed. Setting the slew rate is valid for both rising and falling edges.

All I/Os support 3.3V voltage. Other I/O level standards except 3.3V PCI can support hot plug and cold backup. 3.3V PCI can support 5V voltage by connecting external resistors.

Each I/O contains three registers: input register (InReg), output register (OutReg) and enable register (EnReg). All user triggers in BSTRTAX1000-CQ352 (including input register, output register and enable register of I/O unit) adopt triple-module redundant reinforcement structure.

The I/O is divided into blocks, with 8 blocks per chip, 2 in each direction. Each I/O block shares a common VCCI (I/O supply voltage).

For I/O with reference voltage, each I/O block has a common reference voltage VREF. Although the entire I/O block must share a reference voltage VREF, the user can select its location. In other words, one or more I/Os in the block can be selected as VREF.

Table 3. Different characteristics under different I/O port level configurations

I/O Standard	Clamp Diode	Hot swap/cold backup	5V Tolerance	Input Buffer	Output Buffer
3.3V LVTTL	yes(1)	no	yes(1,2)	Enabled/Disabled	
3.3V PCI	yes	no	yes(2)		
LVCMOS 2.5V	no	yes	no		
LVCMOS 1.8V	no	yes	no		
LVCMOS 1.5V (JESD8-11)	no	yes	no		

Reference voltage input buffer	no	yes	no		
Differential LVDS/LVPECL input	no	yes	no	Enabled	Disabled(3)
Differential LVDS/LVPECL output	no	yes	no	Disabled	Enabled(4)

Note:

- The PCI clamp diode is turned on by default, and the LVTTL clamp diode is turned off by default. The LVTTL clamp diode must be turned on to withstand 5V voltage. After the clamp diode is turned on, hot plugging and cold backup cannot be supported. 5V withstand and hot plugging/cold backup cannot be used at the same time.
- 5V tolerance for 3.3V LVTTL and 3.3V PCI can be achieved through external resistors;
- In differential LVDS/LVPECL input mode, the OE port of the output buffer is automatically cancelled;
- In differential LVDS/LVPECL output mode, the OE port of the output buffer is automatically declared.

3.3V LVTTL and 3.3V PCI ports can withstand 5V level by turning on the clamp diode. 3.3V PCI ports do not support cold backup and hot plug.

When the Clamp Diode is not turned on, the I/O port cannot withstand the 5V level, the LVTTL level can ensure the cold backup and hot plug functions, and the I/O port is in a high-impedance state when the power is off; conversely, when the Clamp Diode is turned on, the I/O port can withstand the 5V level, but the LVTTL level no longer supports the cold backup and hot plug functions, and the I/O port is no longer in a high-impedance state when the power is off.

I/O ports can withstand 3V voltage in all I/O level standards. All port levels except 3.3V PCI support cold backup and hot swap. Cold backup and hot swap are automatically enabled in other port level standards except 3.3V LVTTL and 3.3V PCI.

Connection of special pins

The connections for these pins are shown in the table below.

Table 4. Connection method of special pins (when Silicon Explorer II tool is not needed to detect internal signals of the chip)

Pinout	Connection method
VPUMP	Normally, when using the internal charge pump, VPUMP needs to be grounded. When VPUMP is 3.3V, the internal charge pump needs to be turned off. VPUMP needs to have high drive, low output impedance, and good decoupling properties It is recommended that this pin be connected directly to 3.3V.
TMS	Connect a pull-down resistor to ground, the resistance must be less than 650Ω; or connect a pull-up resistor to VCCDA, the resistance value is unlimited; Can be left floating (there is an internal 10kΩ pull-up resistor on chip).
TDI	Connect a pull-down resistor to ground, the resistance must be less than 650Ω; or connect a pull-up resistor to VCCDA, the resistance value is unlimited; Can be left floating (there is an internal 10kΩ pull-up resistor on chip).
TCK	Connect a pull-up resistor to VCCDA or a pull-down resistor to ground. The resistance value is unlimited. TCK must not be unterminated.
TDO	Must be left floating.
TRST	Connect the pull-down resistor to ground. The resistance must be less than 650Ω (there is a programmable 10kΩ internal pull-up resistor on the chip);
PRA/B/C/D	It can be left floating or connected to VCCI or GND through a pull-up/pull-down resistor (resistance value is unlimited).
NC	This pin is not connected to any other pin on the internal circuit or external package. These pins can be driven to any voltage or left floating.
Unused I/O pins	The default is high impedance. It can be driven to any voltage or left floating.

The resistors listed in Table 4 must be less than a certain value, or the resistor value is unlimited - no resistor is required.

During ground debugging, if you need to use the Silicon Explorer II tool (Silicon Explorer II is a special debugging tool launched by Microsemi for its anti-fuse FPGA products, which can be used to access the internal network of the anti-fuse FPGA and lead out the relevant signals for observation) to detect the internal signals of the chip, you need to lead out the JTAG pin. At this time, the connection method is slightly different, as shown in Table 5. It should be noted that after the ground debugging is completed, the JTAG port needs to be restored to the connection method described in Table 4.

Table 5. Connection method of special pins (when using Silicon Explorer II tool to detect internal signals of chip)

Pinout	**Connection method**
VPUMP	Normally, when using the internal charge pump, VPUMP needs to be grounded. When VPUMP is 3.3V, the internal charge pump needs to be turned off. VPUMP needs to have high drive, low output impedance, and good decoupling properties. It is recommended that this pin be connected directly to 3.3V.
TMS	Leave a place for the pull-up or pull-down resistor on the PCB, and do not solder the resistor when debugging.
TDI	Leave a place for the pull-up or pull-down resistor on the PCB, and do not solder the resistor when debugging.
TCK	Leave a place for the pull-up or pull-down resistor on the PCB, and do not solder the resistor when debugging.
TDO	The pins are directly brought out without the need for connecting pull-up and pull-down resistors in series.
TRST	A position for a pull-up resistor is reserved on the PCB. During debugging, the resistor is not soldered.
PRA/B/C/D	Connect a 70Ω resistor in series and then lead out.
NC	This pin is not connected to any other pin on the internal circuit or external package. These pins can be driven to any voltage or left floating.

Unused I/O pins	The default is high impedance. It can be driven to any voltage or left floating.

If the function used includes Reset, it is recommended to connect CLK ports such as CLKE/F/G/H. These ports have their own driver buffer and consume almost no resources. You can also use ordinary I/O ports, but you need to pay attention to the drive capability.

Hot Swapping

The device I/O ports can be configured to be hot-plug compatible (except for the 3.3V PCI port level), in which all I/O ports are in high impedance during the device power-on and power-off process, and the output ports are released from high impedance only after the device reaches working conditions. Direct insertion of the device into a live system will not reduce its reliability or cause damage to the host system.

Cold backup

The device supports cold backup, and signals can be applied to the I/O ports when the device is not powered or is in the power-on process. Notes on cold backup applications:

- 3.3V PCI ports do not support cold backup, but other types of ports support cold backup.
- During cold backup, the sneak current of each port to which a high-level signal is applied shall not exceed 100μA.

Logical Function Unit

The device provides two types of logic function units: combinational logic unit (C-cell) and register unit (R-cell). Two C-cells and one R-cell form a logic block Cluster, and two logic blocks form a group SupperCluster. The main array of the device is composed of 3×3 CoreTiles, and each CoreTile includes 336 SupperClusters.

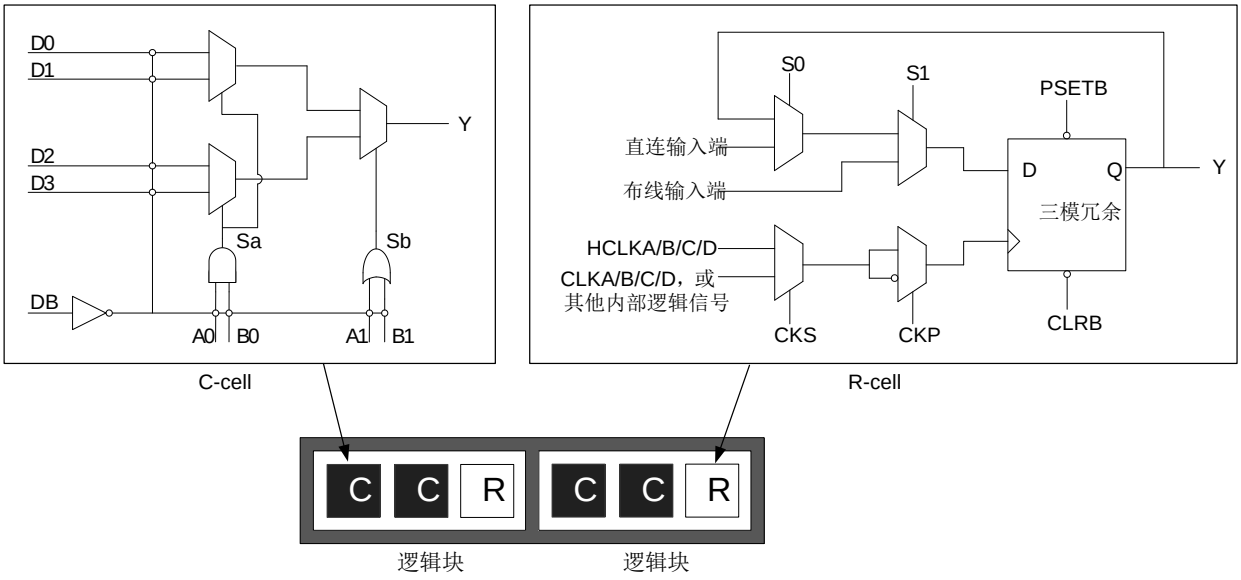


Figure 4. A SuperCluster structure

Unit C

The circuit structure of the C unit is an 8-input multiplexer MUX (data terminals: D0, D1, D2, D3, selection terminals: A0, B0, A1, B1). The structure of the C unit is shown in the figure above. The C unit has the following characteristics:

- Users can connect the signal to any input terminal of the C unit through wiring. The selection terminal (A0, A1, B0, B1) of the C unit can be connected to the wiring clock (CLKE/F/G/H).
- The inverter input terminal DB serves as a supplementary input terminal and can provide a signal to any input terminal of the C unit.

R unit

The core of the R unit is a D flip-flop with a triple-module redundant structure, and its main features are as follows:

- It has two data input terminals: a direct input terminal and a wiring input terminal. The direct input terminal means that the output of the adjacent C unit is directly connected to the input terminal through an aluminum wire,

and the line delay is very small, not exceeding 0.1ns; the wiring input terminal means that the user-defined signal is connected to the input terminal through anti-fuse programming.

- It has asynchronous clear (CLRB) and asynchronous reset (PSETB) functions, both of which are valid at low level. When both are valid, CLRB has a higher priority.
- The R cell can be used as an independent trigger. It can be driven by other C cells or I/O modules through the conventional wiring structure.
- The following three types of clock signals can be used as the clock input of the trigger. The latter two need to be connected by programming anti-fuses. The CKP signal selects the polarity of the clock.
    - Fastest direct input clock HCLKA/B/C/D
    - Four routing clocks (CLKE/F/G/H)
    - User-defined signals
- S0, S1, PSETB and CLRB can be driven by CLKE/F/G/H or user-defined signals.

Logical interconnection

The routing network of the anti-fuse FPGA mainly has four types of routing channels: direct routing channel, fast routing channel, carry-connection routing channel, and horizontal and vertical routing channels. The main routing channels in the anti-fuse FPGA are shown in the figure below. Among the routing channels of the anti-fuse FPGA, the direct routing channel, fast routing channel, and carry-connection routing channel are the bottom-level routing channels, which realize the connection within the Super Cluster and between Super Clusters. The horizontal and vertical routing channels are further divided into local channels and global channels. The local routing channel realizes the connection between each sub-module inside the Core Tile. The global routing channel realizes the signal

connection in the entire FPGA chip, from the south end to the north end, and the east end to the west end of the FPGA chip.

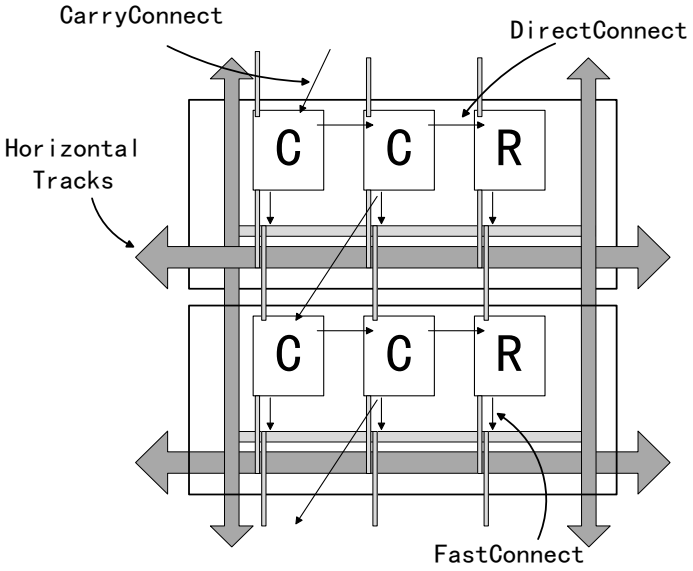


Figure 5 Routing Channels in Antifuse FPGAs

DirectConnect connects the C unit and the adjacent R unit in the Super Cluster, providing the highest performance wiring connection. This connection channel connects the DCOUT of the C unit to the DCIN of the adjacent R unit by configuring the S1 line of the R unit. Direct connection does not require an anti-fuse and can provide a high-speed connection with a delay of less than 0.1ns.

FastConnect is located between the vertical Super Cluster and the Super Cluster immediately below it, and provides high-performance horizontal connections, as shown in the figure above. FastConnect enables high-speed connection of logic signals, and an anti-fuse can be used to establish short-distance connections. FastConnect provides a connection channel with a delay of no more than 0.4ns. The output of each logic module is directly connected to the output track of the same Cluster. The signal on the output track can be connected through an anti-fuse and drive the input of the logic module of the same Super Cluster or the Super Cluster below it.

The CarryConnect channel is used for the carry logic between adjacent Super Clusters and is used to implement a carry chain for the algorithm logic. The FCO output of the C unit on the right side of a Cluster drives the FCI input of the C unit on the left side of the Cluster below the Cluster. The carry connection does not require an anti-fuse structure.

Wiring interconnect: Interconnection made by programming antifuses.

Block RAM/FIFO

In the anti-fuse FPGA of BSTRTAX1000, the main structure is mainly composed of CoreTile, each CoreTile includes a large number of SuperClusters and 4 Block RAM/FIFOs. Block RAM/FIFO is an IP module, which can be configured to realize RAM function or FIFO function. When each Block RAM/FIFO is configured as RAM, the storage capacity is 4608 bits, as shown in the figure below. Each Block RAM/FIFO can be configured as 128×36, 256×18, 512×9, 1K×4, 2K×2 or 4K×1 bits according to needs. RAM modules have independent read and write ports, and both read and write ports can be configured to different bit widths. For example, data can be written in with 8-bit bit width and read out with 1-bit bit width.

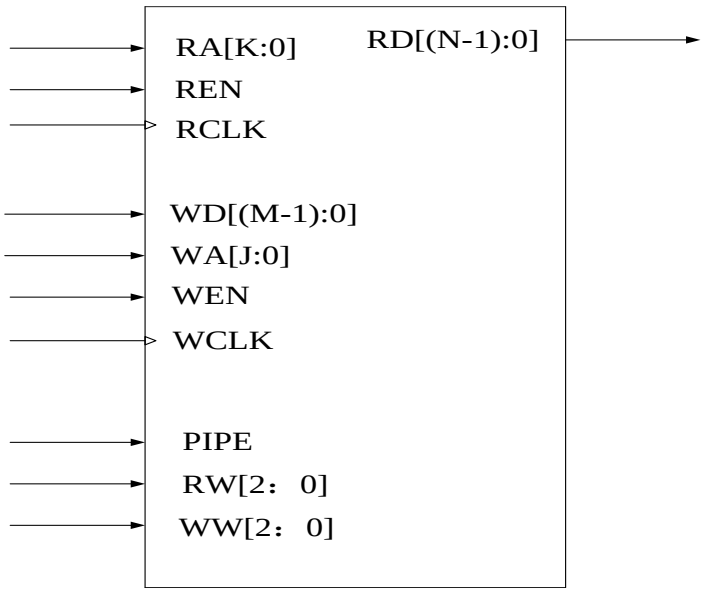


Figure 6 RAM module unit

In addition, each Block RAM/FIFO module has an embedded FIFO control unit, as shown below. This control unit allows the RAM module to be configured as a synchronous FIFO without calling additional logic modules. The width and depth of the FIFO are programmable. In addition to the normal EMPTY and FULL flags, the FIFO also has additional programmable ALMOST-EMPTY (AEMPTY) and ALMOST-FULL (AFULL) flags. In addition to the logic flags, the embedded FIFO control unit also contains the counters necessary to generate read and write addresses, as well as control circuits to avoid metastable and erroneous operations. Embedded RAM/FIFO modules can be cascaded to achieve larger capacity configurations.

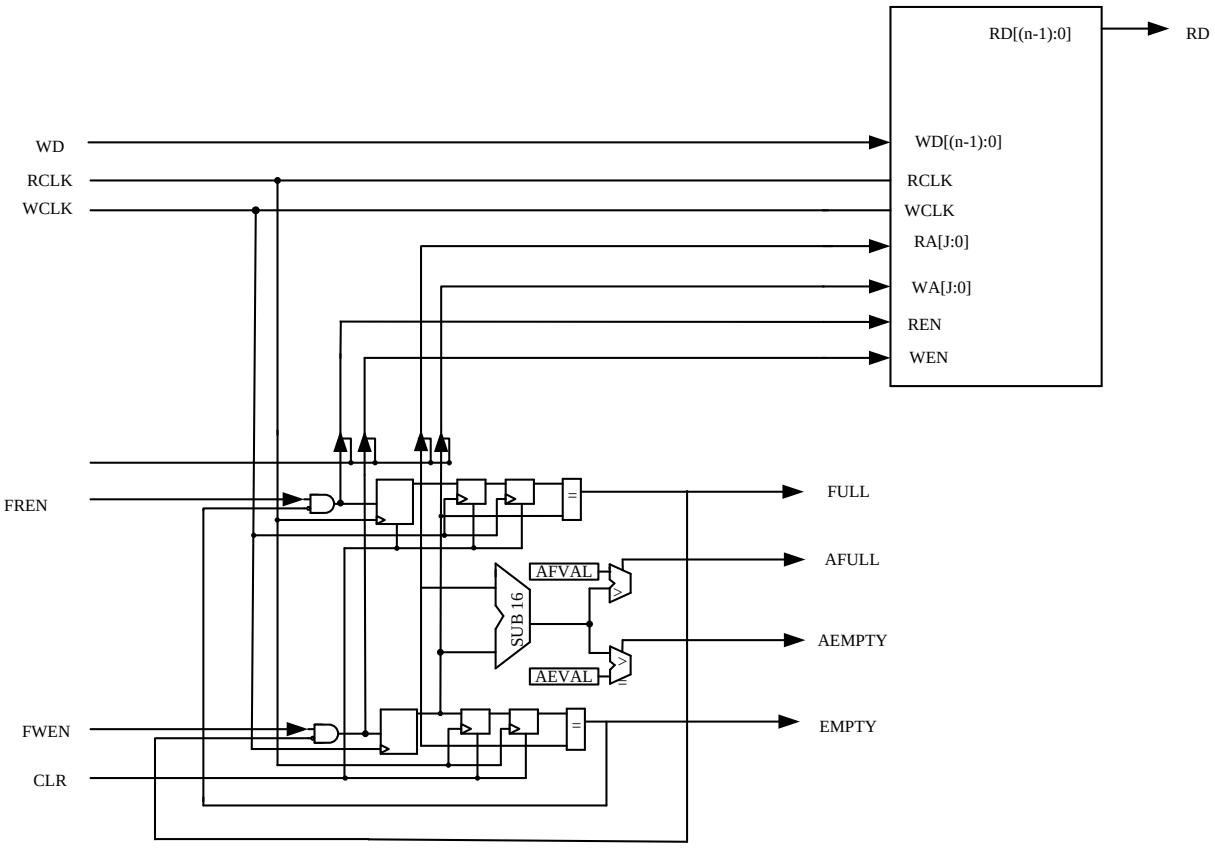


Figure 7. RAM structure with FIFO control unit

1 million gates contain a total capacity of 162K bit Block RAM, which is not hardened. It uses the EDAC IP in the Actel RT series for hardening. EDAC hardened SRAM with refresh: Domestic devices (foreign RT series devices) use EDAC hardened SRAM with

three data bit widths: 8bit,16bit and 32bit. Maximum capacity: 4096×8bit,2048×16bit,1280×32bit.

To refresh the EDAC SRAM, you can call the EDAC IP in the foreign Actel programming software Liebro, as shown in the figure below. (Regular RAM can also be called)

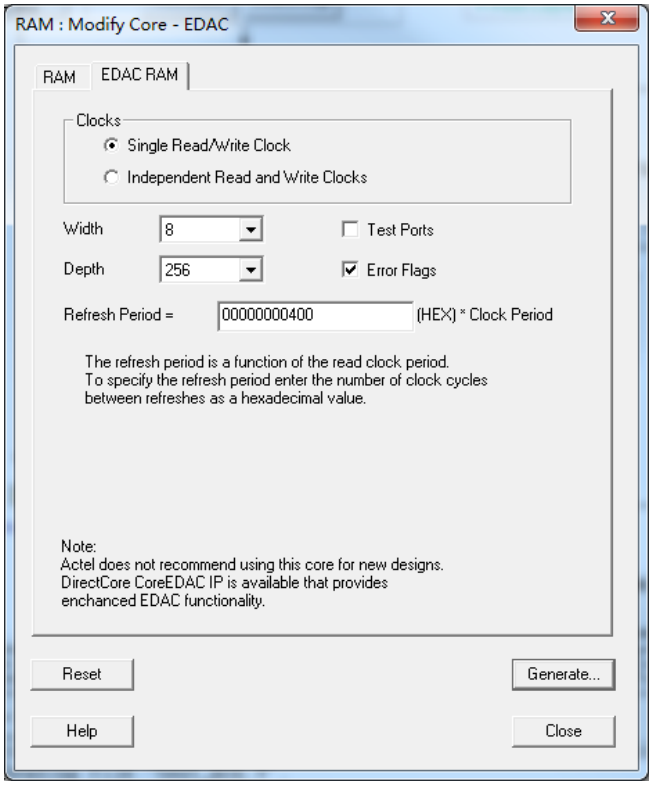


Figure 8. Calling EDAC with refresh to harden RAM

This functional module is generated by the Libero IDE software IP core, and implements the EDAC SRAM function of one-correction and two-checking. At the same time, it can be controlled by the self-refresh enable pin STOP_SCRUB to realize the self-refresh function, correct and write back 1-bit errors, and indicate 2-bit errors.

This module is the same as the foreign RTAX1000S and AX1000. Both use fixed IP.

In Libero, you can call standard RAM or EDAC RAM.

Working conditions

Absolute Maximum Ratings

Exceeding the absolute maximum ratings specified in the table below may cause permanent damage to the circuit.Absolute Maximum RatingsThe following may affect the reliability of the device.

Table 6. Absolute Maximum Ratings

Serial number	project	BSTRTAX1000-CQ352
1	Maximum junction temperature TJ	+135℃
2	Core voltage VCCA	-0.3V~+1.7V
3	I/O voltage VCCI	-0.3V~+3.75V
4	V_{PUMP}Voltage	-0.3V~+3.75V
5	V_{REF}Voltage	-0.3V~+3.75V
6	Input voltage VI	-0.5V~+4.1V
7	Output voltage VO	-0.5V~+3.75V
8	Storage temperature TSG	-60℃~+150℃
9	Differential I/O voltage VCCDA	-0.3V~+3.75V
10	Soldering temperature Brazing (10s)	+250℃

The melting point of the gold-tin solder used in the device sealing ring is 280℃To ensure the airtightness and reliability of the device sealing ring, the soldering (10s) temperature should not exceed 250℃.

Recommended operating conditions

Table 7. Recommended operating conditions

Serial number	project	BSTRTAX1000-CQ352
1	Junction temperature TJ	-55℃ ~+125℃
2	1.5V VCCA	1.425V~1.575V
3	1.5V VCCI	1.425V~1.575V
4	1.8V VCCI	1.71V~1.89V
5	2.5V VCCI	2.375V~2.625V
6	3.3V VCCI	3.0V~3.6V
7	2.5V VCCDA	2.375V~2.625V
8	3.3V VCCDA	3.0V~3.6V
9	3.3V VPUMP	3.0V~3.6V

Main technical parameters

Electrical characteristic parameters

Table 8. Basic electrical characteristics parameters

characteristic	symbol	condition Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx -55℃≤TA≤125℃	Limit value		unit
			Minimum	maximum	
Core power supply quiescent current	I_{CCA}	*f*=0, VCCA=1.575V, VCCIBx=3.6V, VCCDA=3.6V	—	450	mA
		f=0, VCCA=1.575V, VCCIBx=3.6V, VCCDA=3.6V, TA=25℃	—	30	mA
Port power quiescent current	I_{CCI}	*f*=0, VCCA=1.575V, VCCIBX=3.6V, VCCDA=3.6V	—	35	mA
Differential Supply Quiescent Current	*ICCDA*	*f*=0, VCCA=1.575V, VCCIBx=3.6V, VCCDA=3.6V	—	10	mA

Input low level leakage current	I_{IL}	*VIN=GND*	—	5	μA
Input high level leakage current	I_{IH}	*VIN=VCCI*	—	5	μA
Three-state output leakage current	*IOZ*	*VIN=VCCI*	—	5	μA
Port capacitance	*CIO*	*f = 100 kHz, V = 0 V*	—	15	pF
Functional testing	*Func*				
Binning Circuit Delay	*BIN fast*		—	7	μs
	BIN low		—	9.5	μs
Maximum operating frequency c	*Fmax*		350	—	MHz
3.3V LVTTL level (3V≤VCCIBx≤3.6V)					
Input low level	V_{IL}		-0.3	0.8	V
Input high level	V_{IH}		2.0	3.6	V
Output low level	V_{OL}	I_{OL}= 24mA	—	0.4	V
Output high level	V_{OH}	I_{OH}= 24mA	2.4	—	V
2.5V LVCMOS (2.375V≤VCCIBx≤2.625V)					
Input low level	V_{IL}		-0.3	0.7	V
Input high level	V_{IH}		1.7	3.6	V
Output low level	V_{OL}	I_{OL}= 12mA	—	0.4	V
Output high level	V_{OH}	I_{OH}= -12mA	2.0	—	V
1.8V LVCMOS (1.71V≤VCCIBx≤1.89V)					
Input low level	V_{IL}		-0.3	0.2VCCI	V
Input high level	V_{IH}		0.7VCCI	2.1	V
Output low level	V_{OL}	I_{OL}= 8mA	—	0.2	V
Output high level	V_{OH}	I_{OH}= -8mA	VCCI-0.2	—	V
1.5V LVCMOS (1.425V≤VCCIBX≤1.575V)					

Input low level	V_{IL}		-0.5	0.35VCCI	V
Input high level	V_{IH}		0.65VCCI	1.95	V
Output low level	V_{OL}	I_{OL}=8mA	—	0.4	V
Output high level	V_{OH}	I_{OH}= -8mA	VCCI-0.4	—	V
3.3V PCI (3V≤VCCIBx≤3.6V)					
Input low level	V_{IL}		-0.5	0.3VCCI	V
Input high level	V_{IH}		0.5VCCI	VCCI+0.5	V
3.3V GTL+ (3V≤VCCIBx≤3.6V)					
Input low level	V_{IL}			VREF-0.1	V
Input high level	V_{IH}		VREF+0.1		V
Output low level	V_{OL}			0.7	V
1.5V HSTL Class I (1.425V≤VCCIBx≤1.575V)					
Input low level	V_{IL}		-0.3	VREF-0.1	V
Input high level	V_{IH}		VREF+0.1	3.6	V
Output low level	V_{OL}	I_{OL}=8mA	—	0.4	V
Output high level	V_{OH}	I_{OH}= -8mA	VCCI-0.4	—	V
2.5V SSTL2 Class I (2.375V≤VCCIBx≤2.625V)					
Input low level	V_{IL}		-0.3	VREF-0.2	V
Input high level	V_{IH}		VREF+0.2	3.6	V
Output low level	V_{OL}	I_{OL}=7.6mA	—	VREF-0.57	V
Output high level	V_{OH}	I_{OH}= -7.6mA	VREF+0.57	—	V
2.5V SSTL2 Class II (2.375V≤VCCIBx≤2.625V)					
Input low level	V_{IL}		-0.3	VREF-0.2	V
Input high level	V_{IH}		VREF+0.2	3.6	V
Output low level	V_{OL}	I_{OL}=15.2mA	—	VREF-0.8	V
Output high level	V_{OH}	I_{OH}= -15.2mA	VREF+0.8	—	V
3.3V SSTL3 Class I (3V≤VCCIBx≤3.6V)					

Input low level	V_{IL}		-0.3	VREF-0.2	V
Input high level	V_{IH}		VREF+0.2	3.6	V
Output low level	V_{OL}	I_{OL}=8mA	—	VREF-0.6	V
Output high level	V_{OH}	I_{OH}= -8mA	VREF+0.6	—	V
3.3V SSTL3 Class II (3V≤VCCIBx≤3.6V)					
Input low level	V_{IL}		-0.3	VREF-0.2	V
Input high level	V_{IH}		VREF+0.2	3.6	V
Output low level	V_{OL}	I_{OL}=16mA	—	VREF-0.8	V
Output high level	V_{OH}	I_{OH}= -16mA	VREF+0.8	—	V
2.5V LVDS (2.375V≤VCCIBx≤2.625V)					
Output low level	V_{OL}			1.25	V
Output high level	V_{OH}		1.25		V
Differential output voltage	V_{ODIFF}		250	450	mV
Output common mode voltage	V_{OCM}		1.125	1.375	V
Input common mode voltage	V_{ICM}		0.2	2.2	V
3.3V GTL+ (3V≤VCCIBx≤3.6V)					
Input low level	V_{IL}		0.86	2.125	V
Input high level	V_{IH}		1.49	2.72	V
Output low level	V_{OL}		0.96	1.57	V
Output high level	V_{OH}		1.8	2.41	V

Note:

- The voltage is based on GND, GND = 0 V. The current flowing into the lead end of the device is positive.
- The "Binning circuit" is a test circuit inside the circuit, which is used to monitor whether the fluctuation of the manufacturing process is within a reasonable range. It is programmed and tested by the manufacturer before leaving the factory. After programming in the user area, this path cannot be tested.

Reliability

Circuit ESD: ≥2000V.

Radiation resistance

Total radiation dose (TID): ≥ 150k rad (Si)

Single event latch-up threshold (SEL): ≥75MeV•cm2/mg

Single event upset rate:

- -Block RAM (with EDAC turned on and timer 2MHz refresh) ≤10-10 errors/bit·day,
- -Flip-flop logic unit ≤ 10-10 errors/bit·day

Single event upset threshold (SEU): ≥ 13MeV•cm2/mg (Block RAM with EDAC turned on and timer 2MHz refresh)

Device characteristic curve

Relationship between static current, voltage and temperature

existV_{CCI}When the power supply voltage is 3.6V, 3.3V, and 3.0V respectively,The relationship between the power supply quiescent current ICCI and the temperature (range is -55℃～125℃, the initial temperature is -55℃, and the step value is 30℃). Figure 9 shows the test value and characteristic curve of the device power supply quiescent current ICCI changing with the power supply voltage and temperature.

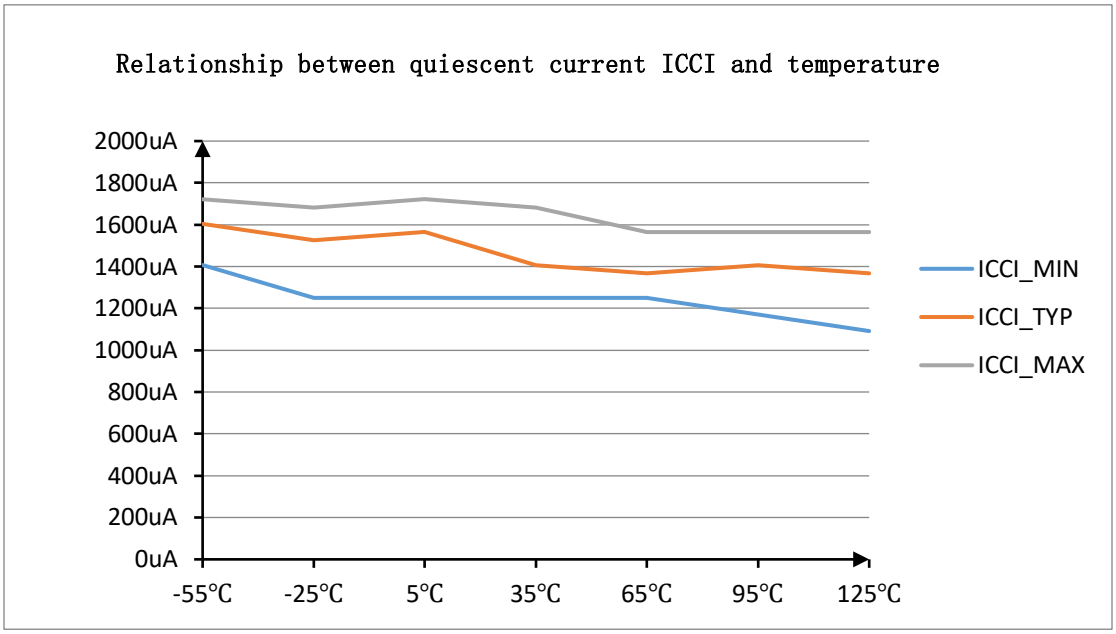


Figure 9. Device power supply current vs. power supply voltage and temperature variation characteristics

It can be seen from the characteristic curve that the power supply static current ICCI increases with the increase of the power supply voltage, does not change much within the overall temperature range, and tends to decrease with the increase of the working environment temperature. The reason for this trend is related to the MOS tube characteristics of this part of the device. Due to the positive temperature characteristics of the MOS tube threshold, when the working environment temperature decreases, the bias voltage increases, and the power supply current increases; similarly, when the power supply voltage decreases, the bias voltage decreases, and the power supply current decreases. This curve conforms to the normal law of the device.

existV_{CCDA}When the power supply voltage is 3.6V, 3.3V, and 3.0V respectively,The relationship between the power supply quiescent current ICCDA and the temperature (range is -55℃～125℃, the initial temperature is -55℃, and the step value is 30℃). Figure 10 shows the test value and characteristic curve of the device power supply quiescent current ICCDA changing with the power supply voltage and temperature.

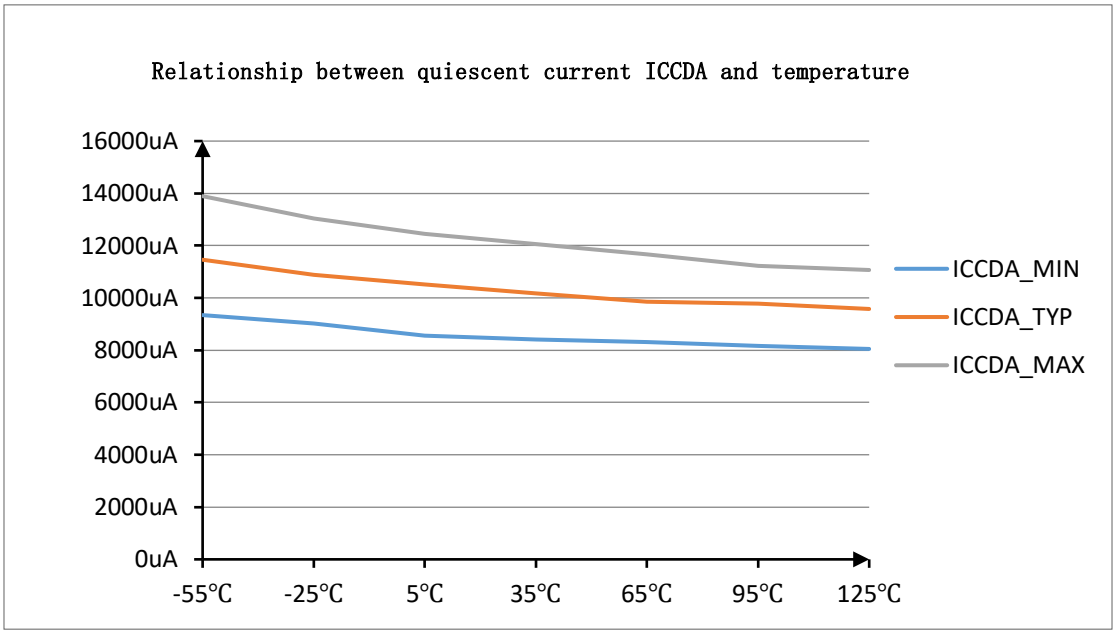


Figure 10. Device power supply current vs. power supply voltage and temperature variation characteristics

It can be seen from the characteristic curve that the power supply static current ICCDA increases with the increase of the power supply voltage, does not change much within the overall temperature range, and tends to decrease with the increase of the working environment temperature. The reason for this trend is related to the MOS tube characteristics of this part of the device. Due to the positive temperature characteristics of the MOS tube threshold, when the working environment temperature decreases, the bias voltage increases, and the power supply current increases; similarly, when the power supply voltage decreases, the bias voltage decreases, and the power supply current decreases. This curve conforms to the normal law of the device.

existV_{CCA}When the power supply voltage is 1.575V, 1.5V, and 1.425V respectively, The relationship between the power supply quiescent current ICCA and temperature (range is -55℃～125℃, initial temperature is -55℃, step value is 30℃). Figure 11 shows the test value and characteristic curve of the device power supply quiescent current ICCA changing with power supply voltage and temperature.

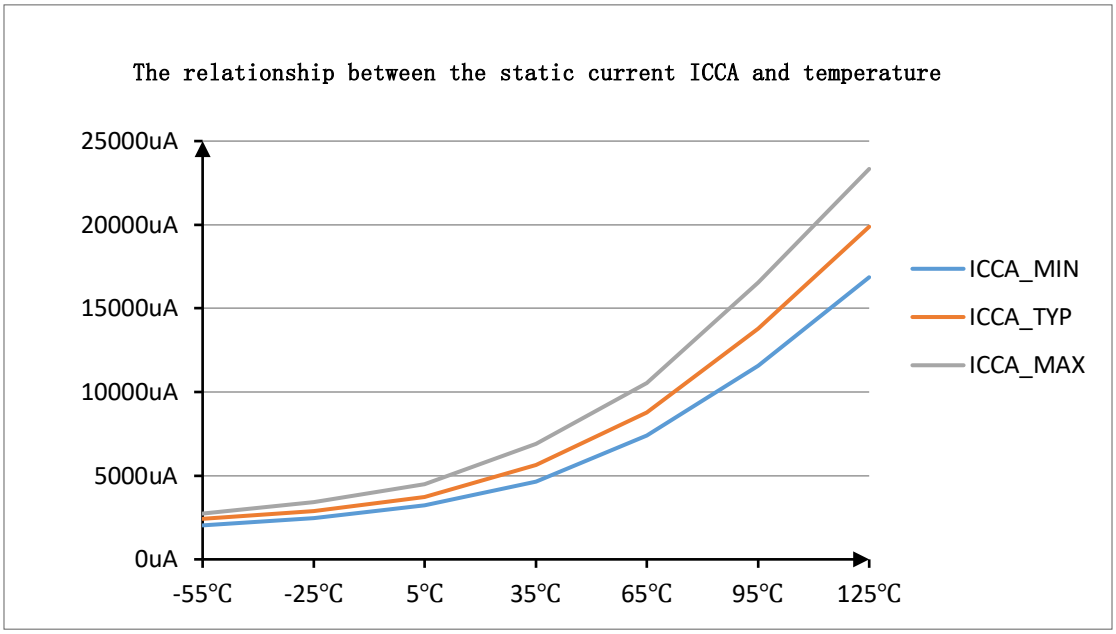


Figure 11. Device power supply current vs. power supply voltage and temperature variation characteristics

It can be seen from the characteristic curve that the power supply static current ICCA increases with the increase of power supply voltage and the increase of working environment temperature. The reason for this trend is related to the MOS tube characteristics of the internal array of the device. Due to the negative temperature characteristics of the MOS tube threshold, when the working environment temperature increases, the bias voltage increases, and the power supply current increases; similarly, when the power supply voltage decreases, the bias voltage decreases, and the power supply current decreases. This curve conforms to the normal law of the device.

Relationship between dynamic current, voltage and temperature changes

existV_{CCI}The power supply voltage is 3.6V, 3.3V, and 3.0V respectively, and the operating frequency is 10MHz.The relationship between the power supply dynamic current IOPI and the temperature (range is -55℃～125℃, the initial temperature is -55℃, and the step value is 30℃). Figure 12 shows the test value and characteristic curve of the device power supply dynamic current IOPI changing with the power supply voltage and temperature.

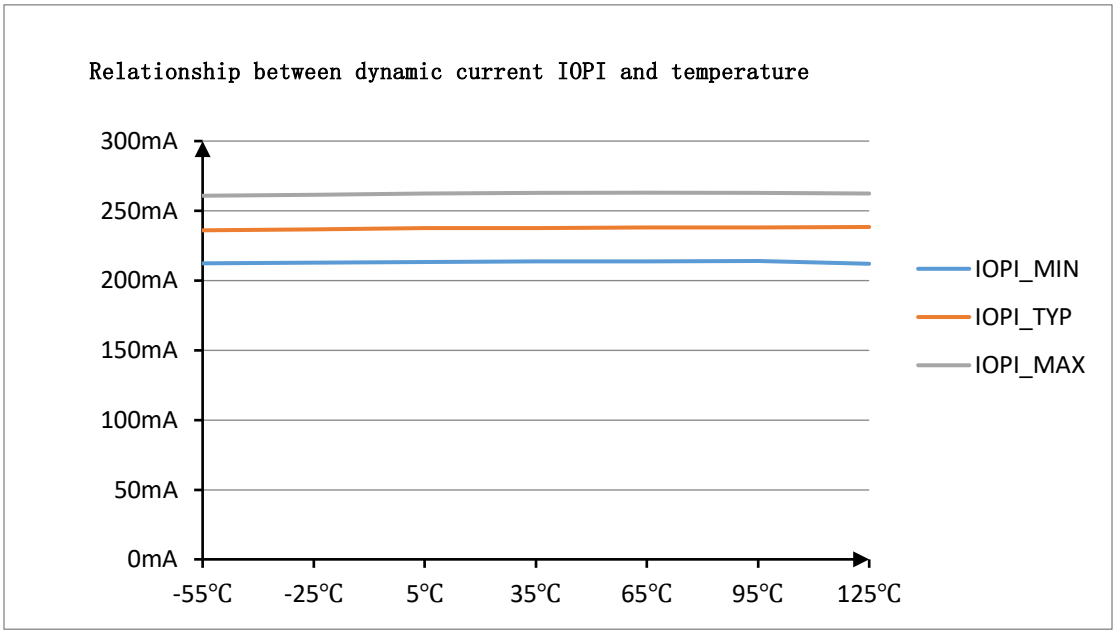


Figure 12. Device power supply current vs. power supply voltage and temperature variation characteristics

From the characteristic curve, it can be seen that the power supply dynamic current IOPI increases with the increase of power supply voltage and does not change much within the overall temperature range. The reason for this trend is related to the MOS tube characteristics of this part of the device. When the bias voltage increases, the power supply current increases; similarly, when the power supply voltage decreases, the bias voltage decreases, and the power supply current decreases. This curve conforms to the normal law of the device.

existV_{CCDA}The power supply voltage is 3.6V, 3.3V, and 3.0V respectively, and the operating frequency is 10MHz.The relationship between the power supply dynamic current IOPDA and the temperature (range is -55℃～125℃, the initial temperature is -55℃, and the step value is 30℃). Figure 13 shows the test value and characteristic curve of the device power supply dynamic current IOPDA changing with the power supply voltage and temperature.

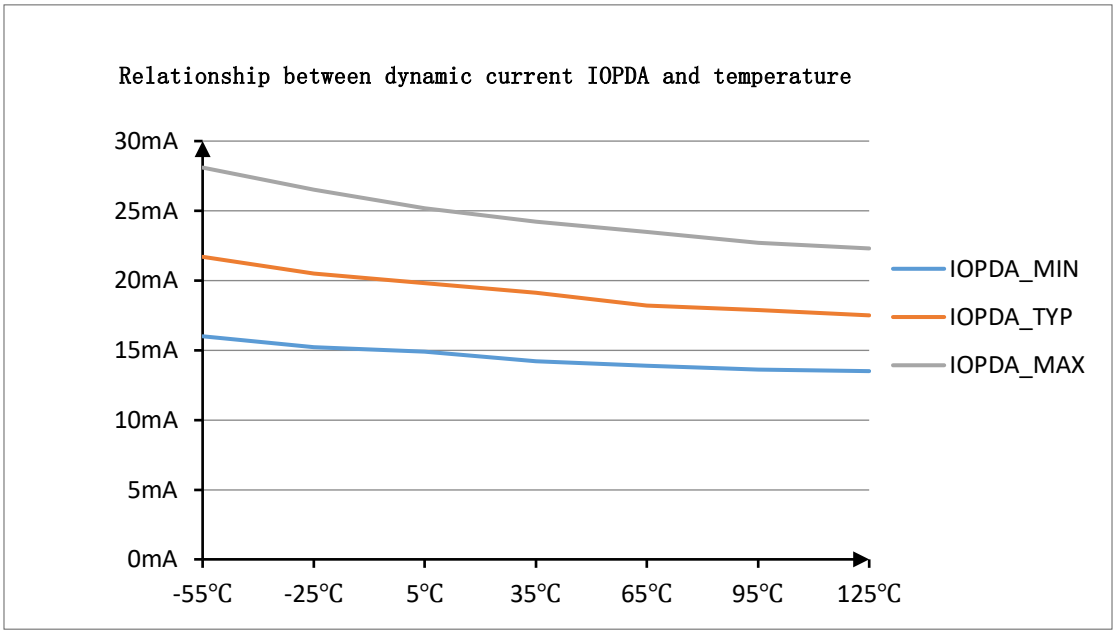


Figure 13. Device power supply current vs. power supply voltage and temperature variation characteristics

It can be seen from the characteristic curve that the power supply dynamic current IOPDA increases with the increase of the power supply voltage, does not change much within the overall temperature range, and tends to decrease with the increase of the working environment temperature. The reason for this trend is related to the MOS tube characteristics of this part of the device. Due to the positive temperature characteristics of the MOS tube threshold, when the working environment temperature decreases, the bias voltage increases, and the power supply current increases; similarly, when the power supply voltage decreases, the bias voltage decreases, and the power supply current decreases. This curve conforms to the normal law of the device.

existV_{CCA}The power supply voltage is 1.575V, 1.5V, 1.425V respectively, the operating frequency is 10MHz,The relationship between the power supply dynamic current IOPA and the temperature (range is -55℃～125℃, the initial temperature is -55℃, and the step value is 30℃). Figure 14 shows the test value and characteristic curve of the device power supply dynamic current IOPA changing with the power supply voltage and temperature.

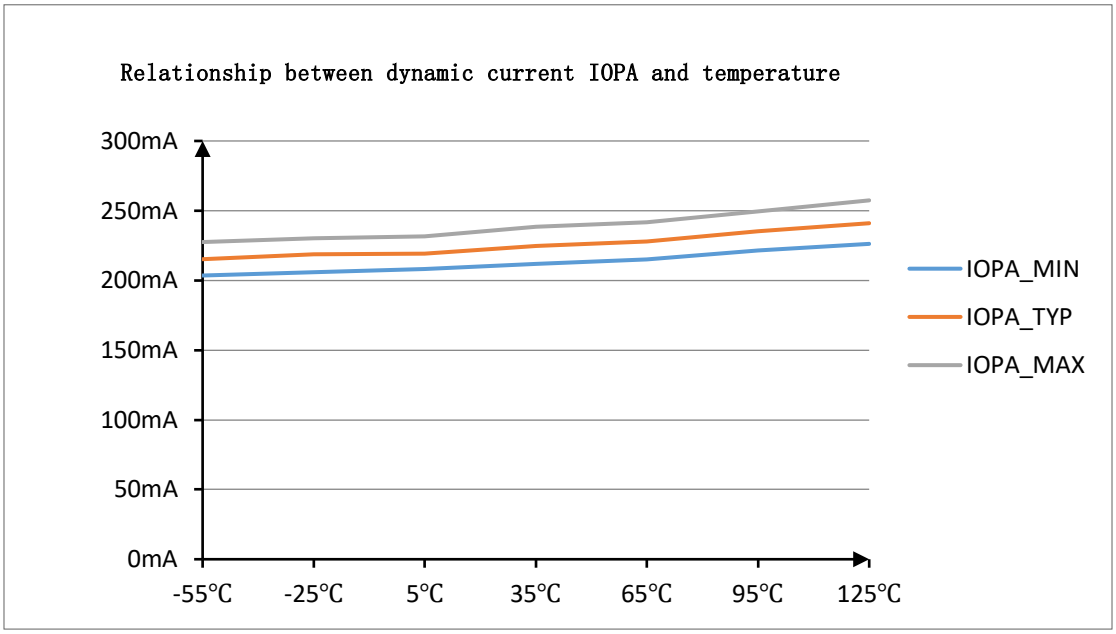


Figure 14. Device power supply current vs. power supply voltage and temperature variation characteristics

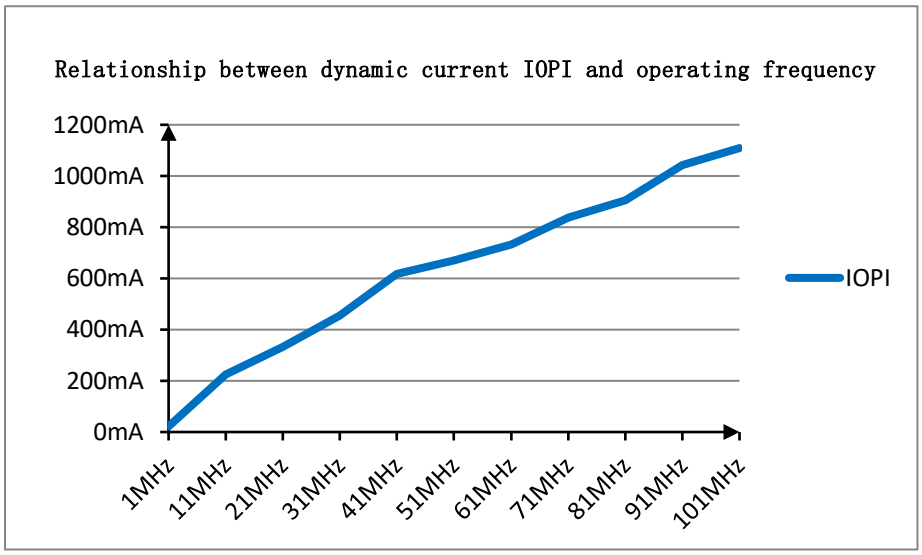
It can be seen from the characteristic curve that the power supply dynamic current IOPA increases with the increase of the power supply voltage and the increase of the working environment temperature. The reason for this trend is related to the MOS tube characteristics of the internal array of the device. Due to the negative temperature characteristics of the MOS tube threshold, when the working environment temperature increases, the bias voltage increases, and the power supply current increases; similarly, when the power supply voltage decreases, the bias voltage decreases, and the power supply current decreases. This curve conforms to the normal law of the device.

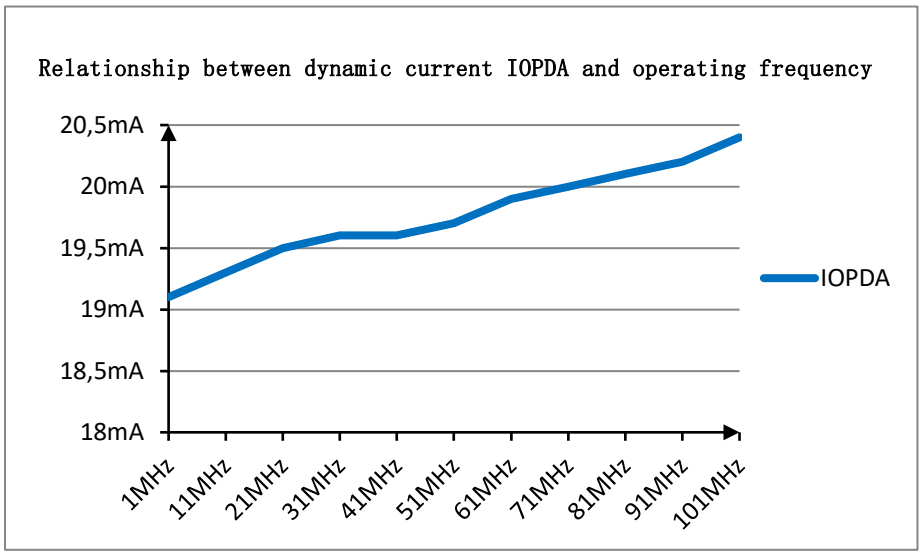
Relationship between dynamic current and operating frequency

At the power supply voltageVCCI=3.3V,VCCDA=3.3V,VCCA=Under the condition of 1.5V and temperature of 25℃,The relationship between the power supply dynamic

current IOPI/IOPDA/IOPA and the operating frequency (the frequency range is 1MHz to 101MHz, the initial frequency is 1MHz, and the step value is 10MHz).

As shown in Figure 15, the deviceTest values and characteristic curves of power supply dynamic current varying with power supply voltage and temperature.





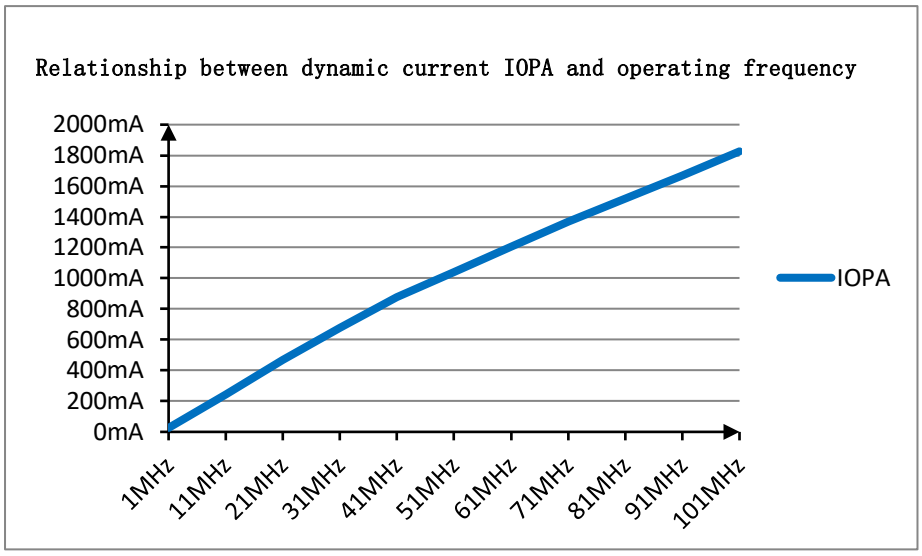


Figure 15. Device power supply dynamic current
and operating frequency change characteristic curve

It can be seen from the characteristic curve that the dynamic current of the power supply increases to varying degrees with the increase of the operating frequency.

The VCCI port power dynamic currentIOPIIt is necessary to consider that the load of each port includes the load capacitance of the test machine port and the board, which is about 20pF; the VCCDA power supply is used to power the differential pins, and the dynamic currentIOPDAThe actual number of differential pins used needs to be considered. This logic uses a total of 5 pairs of differential pins. The VCCA power supply current of this test case is the dynamic current when the utilization rate of the logic resources exceeds 99%. This curve conforms to the normal law of the device.

OutputVoltage and load current relationship

When the power supply voltage is VCCI=3.3V, VCCDA=3.3V, CCA=1.5V,temperatureAt 25℃, the test outputRelationship between voltage and load current, outputRelationship between high level and load currentlikepicture16 shownThe relationship between the output low level and the load current is shown in the figure17 Shown.becausebyDevice restrictions,Port pullCurrent,Sink CurrentMaximumallis 100mA, atThe pull current isAt

100 mA,at this timeOutputhighLevelaboutfor1.8V.existSink CurrentforAt 100 mA,At this time the outputofLow level approx.for0.8V.

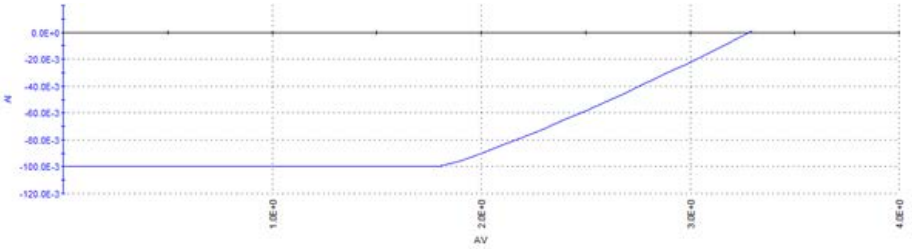


Fig.16. Device output high level and load current characteristic curve

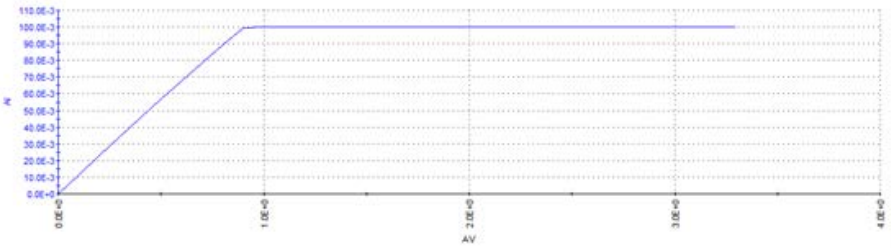


Figure 17. Device output low level and load current characteristic curve

Environmental Limits

Table 9. Environmental Limits

Classification	project	result
Step electrical stress	Rated power supply voltage limit	(1) In the 1-minute stress step test, there is no device failure in the range of VCCA to 3.3V, VCCIBx to 8.25V, VCCDA to 7.75V, Vpump to 7.75V, and VREF to 7.75V. (2) In the 168h stress retention test: VCCDA, VCCI, VPUMP, VREF and VCCA were kept at the maximum operating voltage for 168h without any device failure, which has a large margin compared to the device specification value.
	Rated input voltage limit	(1) In the 1-minute stress step test, there is no device failure when the input voltage VI is in the range of -3.7V to 7.5V. (2) In the 168h stress retention test: there is no failure when the input voltage is in the range of -3.6V to 7.4V, which has a large margin compared to the specification value.
	Rated ESD voltage limit	The device ESD is 2000V.
	Recommended power supply voltage limit	The device can operate normally when the core power supply voltage (VCCA) is in the range of 1.225V~2.275V, which has a large margin compared to the specified value of 1.425V~1.575V. The device can operate normally when the 1.5V port level power supply voltage (VCCIBx) is in the range of 1.125V~1.975V, which has a large margin compared to the specification value of 1.425V~1.575V. The device can operate normally when the 1.8V port level power supply voltage (VCCIBx) is in the range of 1.61V~2.19V, which has a large margin compared to the specification value of 1.71V~1.89V. The device can operate normally when the 2.5V port level power supply voltage (VCCIBx) is in the range of 2.125V~3.025V, which has a large margin compared to the specified value of 2.375V~2.625V. The device can work normally when the 3.3V port level power supply voltage (VCCIBx) is in the range of 2.6V~4.9V, which has a large margin compared to the specification value of 3V~3.6V. The device can operate normally when the 2.5V differential power supply voltage (VCCDA) is in the range of 2.075V to 5V, which

		has a large margin compared to the specified value of 2.375V to 2.625V. The device can operate normally when the 3.3V level differential power supply voltage (VCCDA) is in the range of 2.075V to 5V, which has a large margin compared to the specification value of 3V to 3.6V.
Step temperature stress	Operating temperature limit	The minimum operating temperature is -75℃ (the equipment can reach a minimum of -75℃), and the maximum operating temperature is 160℃, which has a large margin compared to the standard value of -55℃~125℃.
	Temperature shock limit	The test was carried out in accordance with GJB548B-2005 method 1011 condition C. The device passed the inspection without failure after 100 temperature shocks.
Step Mechanical Stress	Mechanical shock limit	The test results show that the step mechanical shock test results show that the device fails under test condition C, so the maximum mechanical shock level that can be withstood is condition B (conditions specified in group D4 of the detailed specification).
	Random vibration limit	The test results show that the device did not fail after random vibration according to GJB548B-2005 method 2026 conditions 1D, 1E and 1F, and passed the inspection.
	Constant acceleration limit	The results of the constant acceleration test show that the device did not fail after constant acceleration was performed according to GJB548B-2005 method 2001 conditions C, D and E, and the inspection was qualified.

Application Guide

Device Development and Programming Process

The device development environment uses Actel's Libero Integrated Design Environment (IDE). It is recommended to use Libero9.2 SP4 version. The Synplify tool recommends using the 2019ME version that comes with Libero9.2 SP4. The software can be downloaded from the Microsemi official website, or you can contact us for more information.

Device programming requires the use of BPM's "Universal Device Programmer" or Actel's "Actel Device Programmer" (also produced by BPM). The recommended programmer hardware model is Silicon Sculptor 3.

The supporting software for the programmer is BPWin or sculptw. The preferred software version is BPWin V6.4.0, which can be downloaded from the Microsemi official website, or contact us to provide the software CD.

The development and programming process is shown in the figure below. Please refer to Appendix B and Appendix D for detailed process.

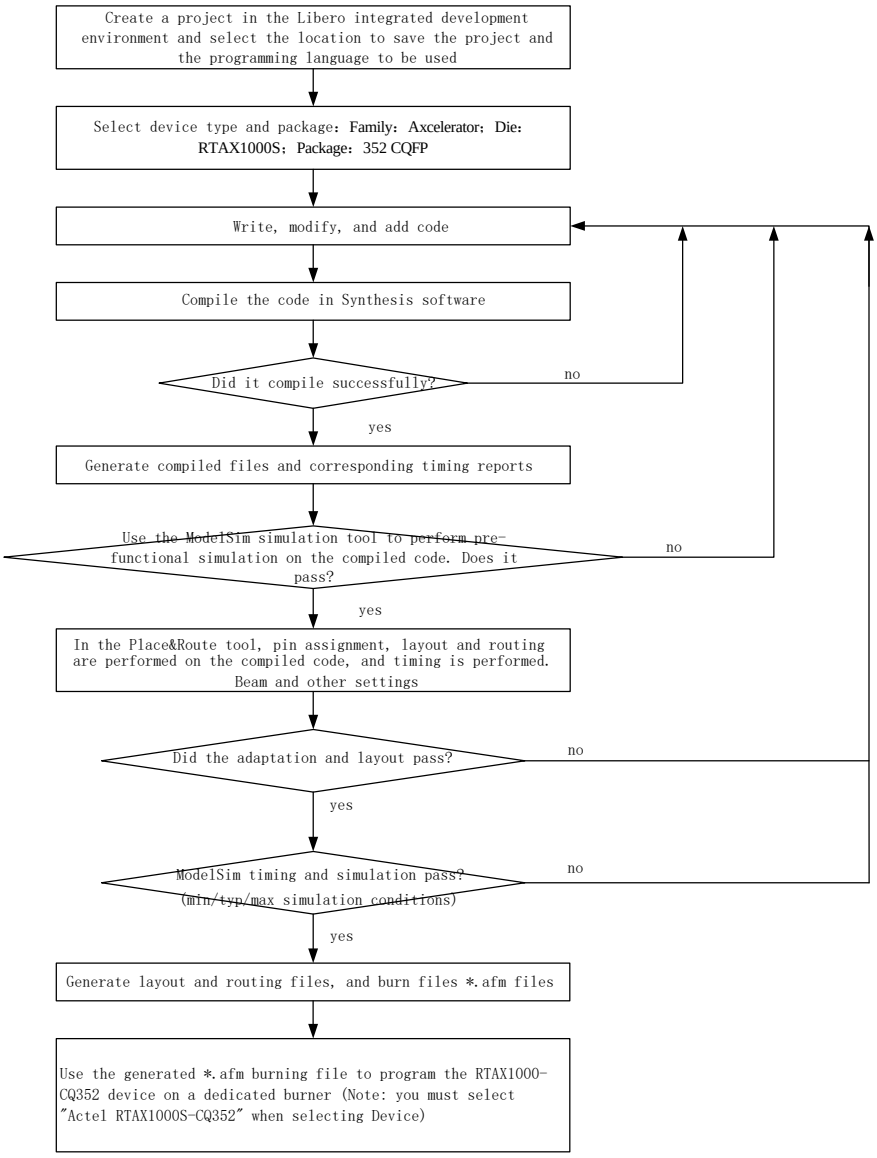


Fig.16. Device Development and Programming Flowchart

It should be noted that RTAX1000S should be selected when selecting the device in the second and last step of the above figure, as shown in the figure below.

In addition, the device can only be programmed once, and the programming process cannot be stopped or powered off. After programming is completed, the device cannot be programmed again.

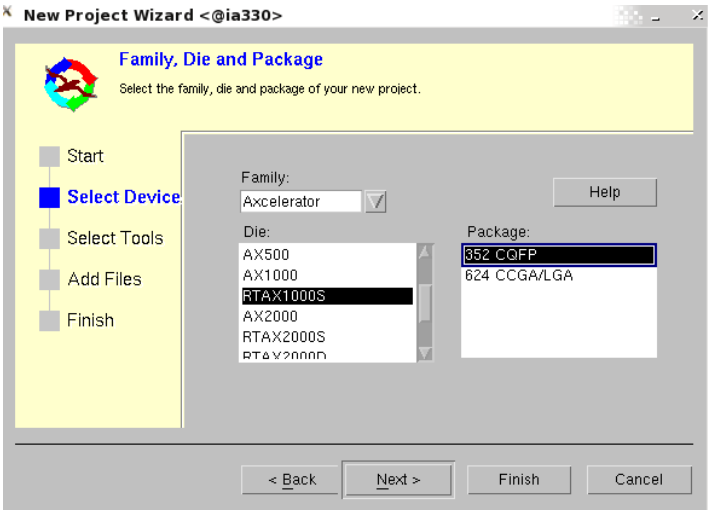


Fig.17. Libero development environment device selection interface

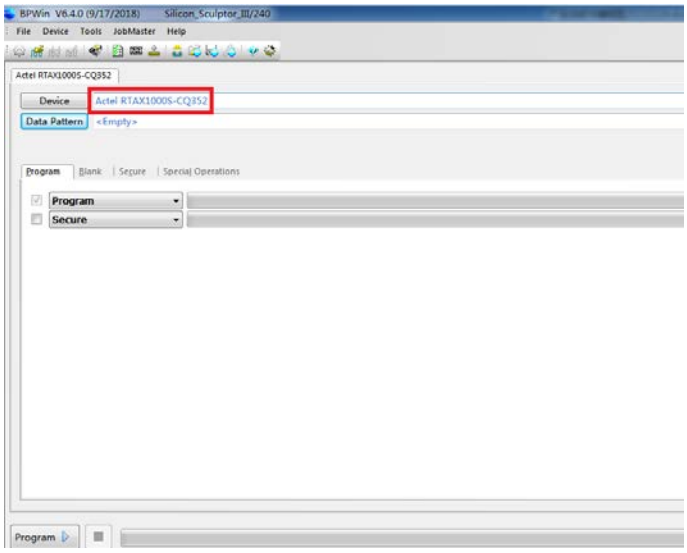


Fig.18. Programmer host computer software interface

Application Guidance Suggestions

- The user should consider the heat dissipation of the device when derating the operating frequency and power consumption. The power consumption evaluation is based on the power consumption calculator instructions in Appendix E.

- Timing constraints and analysis are the basis for ensuring the correct implementation of functions. When designing, you should ensure that the signal setup time, hold time, maximum and minimum delay parameters have sufficient margins. For information related to timing constraints, please refer to "Advanced Static Timing Analysis Using SmartTime" and "Source-Synchronous Clock Designs: Timing Constraints and Analysis".
- HCLKA/B/C/D has the smallest network transmission delay and clock offset, providing a high-speed channel for the clock signal, but it cannot be connected to combinational logic or directly output. HCLKA/B/C/D cannot be used in applications where the clock is directly connected to combinational logic or the clock is directly output at the original frequency through the I/O port. Please useCLKE/F/G/H.
- Clock skew may cause functional errors, so it is recommended that users give priority to using global clocks to reduce clock skew, and pay attention to the impact of clock skew in the design. Recommended clock priority order: HCLKA/B/C/D→CLKE/F/G/H.
- The TRST pin must be grounded after the device is soldered to prevent the JTAG circuit from affecting the normal operation of the user logic in an irradiated environment.
- Unused clock pins should be connected to power or ground. Unused I/O pins are in high impedance state internally, and it is recommended to leave them floating, connected to power or ground.
- When the R unit resources are insufficient, two C units can be used to construct one R unit, but the R unit constructed in this way has a low ability to resist SEU, so it should be used with caution. In addition, when the R unit resources are insufficient, the software will not automatically use this

structure, and it must be manually specified in the code to be called (macro unit name: DF1_CC, DFC1B_CC, DFP1B_CC).

- When multiple output ports flip in the same direction at the same time, it is easy to generate large power bounce and ground bounce noise. During the design, you should take certain measures, such as using "low slope mode" or using delay units to stagger the flipping time of different output ports.
- When developing software code, you need to consider: Since the state of the register unit in the anti-fuse FPGA is uncertain after power-on, it needs to be assigned an initial value.
- The melting point of the gold-tin solder used in the device sealing ring is 280°C. To ensure the airtightness and reliability of the device sealing ring, the soldering (10s) temperature should not exceed 250°C. In addition, since the device is a one-time programmable device, users generally manually solder it in the final stage of the whole board, and the manual soldering (non-hot air gun) temperature should not exceed 300°C.
- The weight of BSTRTAX1000-CQ352 after molding is about 22g, which is heavy, so vibration reinforcement measures should be taken. In addition to the conventional four-corner glue dispensing process, it is recommended to use bottom glue dispensing for reinforcement, and epoxy resin adhesive materials are preferred. Bottom glue dispensing can be selected after mechanical simulation according to the user's application.
- The device does not require a specific power-up sequence.At power-on, all I/Os are in high-impedance state until they reach a set state. At power-off, all I/Os are in high-impedance state.
- Compared with the foreign AX1000-CQ352, the domestic device BSTRTAX1000-CQ352 has deleted the PLL function inside, which is consistent with the foreign anti-addition product BSTRTAX1000-CQ352.

The ports of BSTRTAX1000-CQ352 are exactly the same as those of foreign RTAX1000-CQ352. Compared with foreign AX1000-CQ352, it does not have 8 PLLs. Therefore, the 16 ports corresponding to 8 PLLs are different, as shown in the following table:

Table 10. Port differences between CQ352 package and foreign AX1000 products

PIN Number	AX1000-CQ352	BSTRTAX1000-CQ352	the difference
317	VCCPLA	NC	These are analog power supplies for 8 PLLs in AX1000. When PLL is not used in AX1000, the corresponding port is connected to VCCA.
315	VCCPLB	NC	
303	VCCPLC	NC	
301	VCCPLD	NC	
140	VCCPLE	NC	
138	VCCPLF	NC	
126	VCCPLG	NC	
124	VCCPL	NC	
318	VCOMPLA	NC	These are the compensation reference signals for the eight PLLs in AX1000. When the PLL in AX1000 is not in use, the corresponding port is left floating.
316	VCOMPLB	NC	
304	VCOMPLC	NC	
302	VCOMPLD	NC	
141	VCOMPLE	NC	
139	VCOMPLF	NC	
127	VCOMPLG	NC	
125	VCOMPLH	NC	

When replacing AX1000-CQ352 with BSTRTAX1000-CQ352, the 16 NC ports related to PLL can be left floating and connected to GND or VCCA, so it can be directly replaced without changing the connection. Except for these 16 ports, the other ports are in the same position as the foreign AX1000-CQ352 products, and the bank number is also the same.

For a detailed comparison with foreign circuits, see Appendix G.

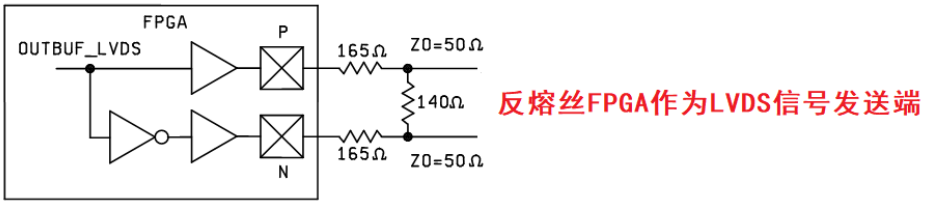
- Input Delay: The input delay of the clock port of the domestic device BSTRTAX1000-CQ352 (consistent with the foreign RT series RTAX1000-CQ352) is not available. The input delay of other ports is available and can be set by the user. It is consistent with the foreign anti-addition product RTAX1000-CQ352.
- Radiation hardening:
  - BSTRTAX1000-CQ352 has triple-module redundancy reinforcement for sequential logic resources (flip-flop R units), which uses a self-refresh correction mechanism for immediate correction. The reinforcement scheme is the same as that of foreign RTAX1000, but different from foreign circuit AX1000-CQ352, which does not have SEU reinforcement.
  - The input and output registers of I/O are also reinforced with triple-module redundancy, and a self-refresh correction mechanism is adopted to make corrections in real time. The reinforcement scheme is the same as that of the foreign RTAX1000, but different from the foreign circuit AX1000-CQ352, which does not have SEU reinforcement.
  - Both clock signals and global signals have been hardened against radiation. Hardening has also been done for SET.

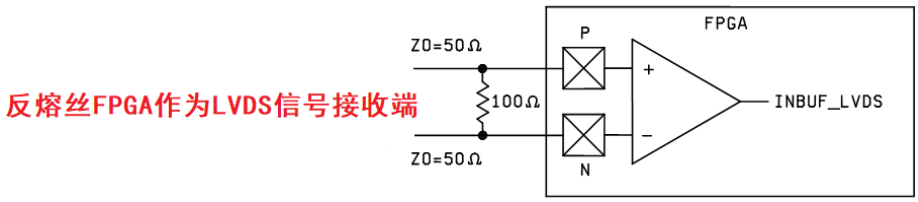
- The reinforcement scheme is the same as that of the foreign RTAX1000, but different from the foreign circuit AX1000-CQ352, the foreign AX1000 is not reinforced.
- The combinational logic resource C unit uses a MUX-based LUT structure without SEU reinforcement, which is consistent with foreign RTAX1000 and AX1000.

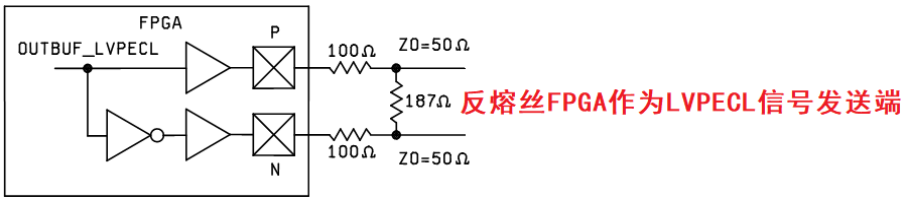
- Maximum power consumption calculation
  - BSTRTAX1000-CQ352 uses the same single-particle hardening technology as the foreign RTAX1000-CQ352. The sequential logic R unit and the registers in the I/O are hardened with triple-module redundancy. Therefore, compared with AX1000-CQ352, the power consumption is higher.
  - The power consumption of BSTRTAX1000-CQ352 is comparable to that of the foreign RTAX1000-CQ352. For the specific power consumption evaluation method, see Appendix E.
  - VCCDA. In BSTRTAX1000, the VCCDA port supplies power to differential ports and ports with reference levels. With each additional pair of differential ports or ports with reference levels, the static power consumption of VCCDA increases. This needs to be noted when evaluating power consumption.
  - See ICCDA and ICCDIFFA in the specification. ICCDA is the static current when differential ports and ports with reference levels are not used; ICCDIFFA is the additional static current for each additional pair of differential ports or ports with reference levels.
  - There are several principles for the VCCDA level:
    - VCCDA must be higher than or equal to the maximum level of all VCCI in BSTRTAX1000.

- When the differential port is not used or with reference voltage, VCCDA can use 2.5V. However, condition (1) must also be met.
- Whenever a differential port or reference level is used, VCCDA must use 3.3V.
- In addition, in the AX series and AX1000, for the sake of simplicity, the manual requires that VCCDA can only use 3.3V. The circuits for VCCDA in BSTRTAX1000 and AX1000 are the same and there is no difference.

- BSTRTAX1000-CQ352 does not use a heat sink.
- If you want to use LVDS or LVPECL differential signals, you need to connect the corresponding termination resistors (the specific connection method is the same as that of foreign AX1000-CQ352 circuit), as shown in the figure below.







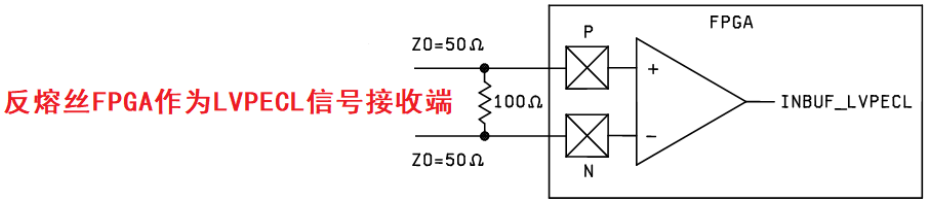


Fig.19. Termination resistor connection method

Precautions

Product transportation and storage precautions

The chip storage environment temperature is: -65℃ To +150℃ Use the designated anti-static packaging box to package and transport the product. During transportation, ensure that the chip does not collide with foreign objects.This productIt should be placed in an air-conditioned environment with temperature and humidity control to prevent the pins from oxidizing due to long-term storage, which will affect solderability.

Product unpacking and inspection

The product storage environment temperature is: -65℃To +150℃. Use the designated anti-static packaging box to package and transport the product. During transportation, ensure that the product does not collide with foreign objects. This product should be placed in an air-conditioned environment with temperature and humidity control to prevent the pins from oxidizing due to long-term storage, which will affect solderability.

Circuit Operation Notes

This product is an electrostatic sensitive device and should be installed and operated in strict accordance with the operating requirements for electrostatic sensitive devices specified in relevant national standards.

During the installation of this product, it is forbidden to touch or weld this type of product without anti-static wrist straps and other tools, and bare hands are not allowed to touch the external leads of the product. Installation and use must be carried out in an anti-static work area (equipped with anti-static work tables, tables and chairs, etc.), equipped with an ion fan, and operated within the effective range of the ion fan.

Operators must receive anti-static training, wear anti-static work clothes (including anti-static gloves or finger cots, hats, work shoes and anti-static wrist straps), and avoid actions or operations that are likely to generate static electricity.

The anti-static equipment (such as wrist straps and finger cots, etc.) should be tested regularly to ensure that qualified anti-static equipment is used before each use.

Devices should be stored in containers made of static dissipative materials (e.g., special boxes for integrated circuits). Plastics, rubber, or silk fabrics that cause static electricity should be avoided during production, testing, use, and transportation.

Ensure the relative temperature and humidity of the anti-static work area. Ensure the relative temperature and humidity of the anti-static work area.

Use this product strictly in accordance with the recommended operating conditions. Using this product beyond the absolute maximum ratings may cause permanent damage to the product.

If the system is used in situations with high temperature changes and vibration requirements, it is recommended to take reinforcement measures for the circuit to improve its ability to resist mechanical vibration and thermal stress.

Illustrate

Version and Disclaimer

Version Number	Release time	Revisions
A0	2022.6	Pre-release
A1	2023.3	• Corrected some editorial errors in the first draft; • Modify the device number in "Standard Implementation"; • The Chinese description of Table 2 has been modified; • Improve the description of device radiation resistance indicators; • Improve the special pin connection method in Section 4.3.1; • Added content 6.4 and 6.5; • Modify the recommended versions of IDE software and Synplify software in Section 7.1, as well as the device development and programming flow chart; • In 7.2 Application Guidance Suggestions, add "When developing software code, you need to consider: because the state of the register unit in the anti-fuse FPGA is uncertain after power-on, it needs to be assigned an initial value"; • Replaced Figure B-8 in Appendix B and added relevant instructions; Added relevant instructions for Libero software to call its own Modelsim software for post-simulation verification in Appendix B; • The order of pictures D-2, D-3, and D-4 in Appendix D has been adjusted, and the text descriptions have been adjusted accordingly.
A2	2023.12	• Cover instruction manual number: (SHM/FC 50156-A1) to (SHM/FC 5015)6-A2); • The title of Section 5.1, Absolute Maximum Ratings, was changed to Absolute Maximum Ratings; • Added 17) LVDS and LVPECL differential signal impedance network in Section 7.2; • Added product identification information to Section 9.1;

		• Added relevant description text in Figure B-10 of Appendix B; added relevant description text in Figure B-12 to remind users not to select 3.3V PCI level; • Figure B-28 and related text descriptions are added to Appendix B. The original Figure B-28 becomes Figure B-29, and the naming order of other figures is similar; • Added Section 3 of Appendix C (note that this temperature refers to the junction temperature of the device, that is, the internal temperature of the device after operation, not the external ambient temperature); • 8) Appendix G deletes BSTRTAX1000-LG624 and foreign RTAX1000S-LG624 comparison description, only BSTRTAX is retained1000-CQ352 and foreign RTAX1000-CQ352 comparative description.

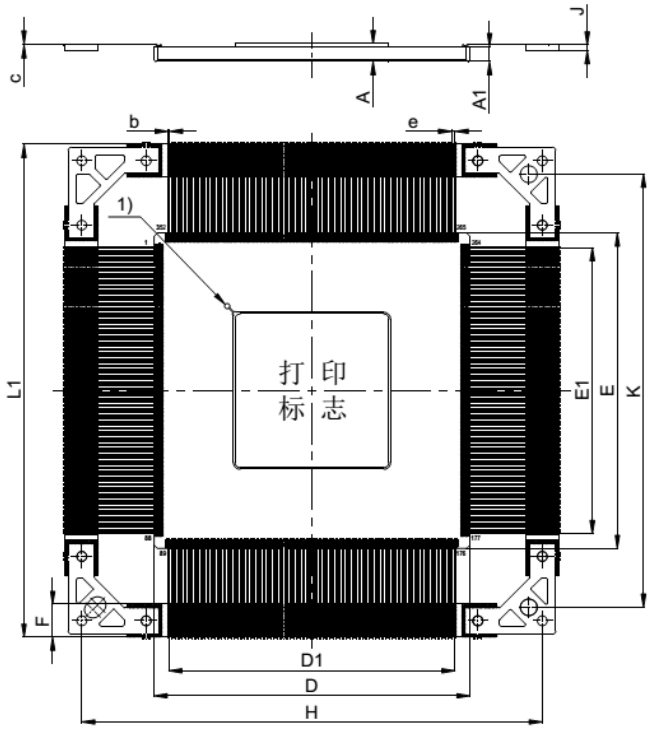
Disclaimer:

Our institute is only responsible for the current validity of this product manual at the time of issuance, and will not notify you of version updates. If you need to know the latest information about this product, please consult us according to the contact information in Article 9.2.

All technical information contained in this product manual is only for users to have a preliminary understanding of this product. If there is any discrepancy with the detailed product specifications, the detailed product specifications shall prevail.

Appendix A Package Dimensions and Pin Description

The device shape is in accordance with GB/T7092-1993, using 0.50mm pitch 352 lead ceramic quad flat (CQFP352) package, the specific dimensions are shown in the figure below:



Dimension symbols	Value, unit: mm		
	Minimum	Nominal	maximum
A	2.47	2.75	3.03
A1	2.07	2.30	2.53
b	0.15	0.20	0.25
c	0.10	0.15	0.20
D (E)	47.80	48.00	48.20
D1 (E1)	-	43.51	-
e	-	0.50	-
F	4.87	5.00	5.13
H	69.80	70.00	70.20
J	0.77	0.90	1.03
K	65.70	65.90	66.10
L1	74.70	75.00	75.30

Figure A-1. Dimensions

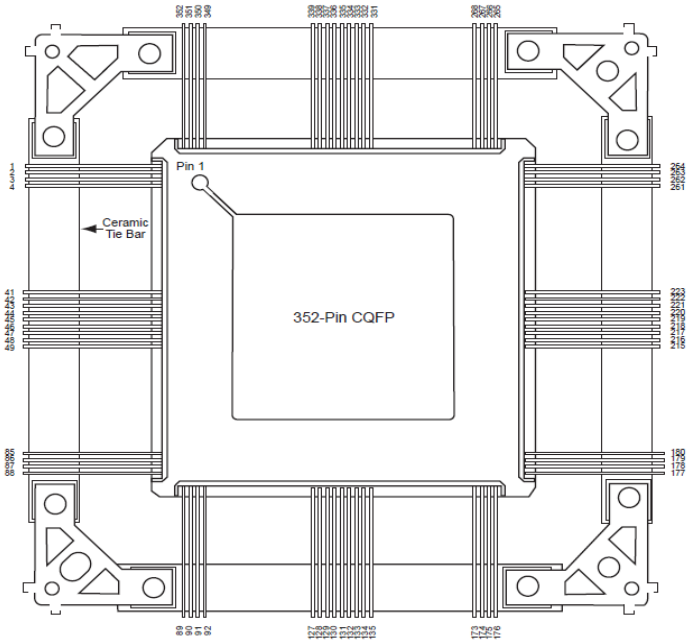


Figure A-2. CQFP352 pinout

Table A-1. Pin Assignment Table

Name	CQFP352 package pinout		Name	CQFP352 package pinout		Name	CQFP352 package pinout
Bank0			IO159P/CLKEP	143		GND	222
IO02N	341		IO160N/CLKFN	136		GND	228
IO02P	342		IO160P/CLKFP	137		GND	234
IO03P (single-ended only)	343		Bank5			GND	240
IO04N	337		IO161N/CLKGN	128		GND	246
IO04P	338		IO161P/CLKGP	129		GND	252
IO08N	331		IO162N/CLKHN	122		GND	258
IO08P	332		IO162P/CLKHP	123		GND	264
IO09N	335		IO167N	118		GND	265
IO09P	336		IO167P	119		GND	274
IO24N	325		IO183N	110		GND	280
IO24P	326		IO183P	111		GND	286
IO25N	323		IO184N	112		GND	292
IO25P	324		IO184P	113		GND	298
IO30N/HCLKAN	319		IO185N	104		GND	310

IO30P/HCLKAP	320		IO185P	105		GND	322
IO31N/HCLKBN	313		IO186N	106		GND	330
IO31P/HCLKBP	314		IO186P	107		GND	334
Bank1			IO187N	98		GND	340
IO32N/HCLKCN	305		IO187P	99		GND	345
IO32P/HCLKCP	306		IO188N	100		GND	352
IO33N/HCLKDN	299		IO188P	101		NC	91
IO33P/HCLKDP	300		IO190N	94		NC	124
IO38N	295		IO190P	95		NC	125
IO38P	296		IO192N	92		NC	126
IO54N	287		IO192P	93		NC	127
IO54P	288		Bank6			NC	130
IO55N	289		IO193P (single-ended only)	86		NC	131
IO55P	290		IO194N	84		NC	138
IO56N	281		IO194P	85		NC	139
IO56P	282		IO196N	78		NC	140
IO57N	283		IO196P	79		NC	141
IO57P	284		IO197N	82		NC	174
IO59N	277		IO197P	83		NC	268
IO59P	278		IO198N	76		NC	301
IO60N	275		IO198P	77		NC	302
IO60P	276		IO203N	72		NC	303
IO61N	271		IO203P	73		NC	304
IO61P	272		IO204N	70		NC	307
IO63N	269		IO204P	71		NC	308
IO63P	270		IO205N	66		NC	315
Bank2			IO205P	67		NC	316
IO64N	259		IO206N	64		NC	317
IO64P	260		IO206P	65		NC	318
IO67N	261		IO207N	60		PRA	312
IO67P	262		IO207P	61		PRB	311
IO68N	255		IO208N	58		PRC	135
IO68P	256		IO208P	59		PRD	134
IO69N	253		IO211N	54		TCK	349
IO69P	254		IO211P	55		TDI	348
IO74N	249		IO212N	52		TDO	347
IO74P	250		IO212P	53		TMS	350

IO75N	247		IO223N	48		TRST	351
IO75P	248		IO223P	49		VCCA	3
IO76N	243		IO224N	46		VCCA	14
IO76P	244		IO224P	47		VCCA	32
IO77N	241		Bank7			VCCA	56
IO77P	242		IO225N	40		VCCA	74
IO78N	237		IO225P	41		VCCA	87
IO78P	238		IO226N	42		VCCA	102
IO79N	235		IO226P	43		VCCA	114
IO79P	236		IO237N	34		VCCA	150
IO82N	231		IO237P	35		VCCA	162
IO82P	232		IO238N	36		VCCA	175
IO83N	229		IO238P	37		VCCA	191
IO83P	230		IO240N	30		VCCA	209
IO94N	225		IO240P	31		VCCA	233
IO94P	226		IO241N	28		VCCA	251
IO95N	223		IO241P	29		VCCA	263
IO95P	224		IO242N	24		VCCA	279
Bank3			IO242P	25		VCCA	291
IO96N	217		IO244N	22		VCCA	329
IO96P	218		IO244P	23		VCCA	339
IO97N	219		IO245N	18		VCCDA	2
IO97P	220		IO245P	19		VCCDA	44
IO99N	213		IO246N	16		VCCDA	90
IO99P	214		IO246P	17		VCCDA	116
IO108N	211		IO249N	12		VCCDA	117
IO108P	212		IO249P	13		VCCDA	132
IO109N	207		IO250N	10		VCCDA	148
IO109P	208		IO250P	11		VCCDA	149
IO111N	205		IO256N	4		VCCDA	178
IO111P	206		IO256P	5		VCCDA	221
IO112N	199		IO257N	6		VCCDA	266
IO112P	200		IO257P	7		VCCDA	293
IO113N	201		Shared I/O			VCCDA	294
IO113P	202		GND	1		VCCDA	309
IO115N	195		GND	9		VCCDA	327

IO115P	196		GND	15		VCCDA	328
IO116N	193		GND	21		VCCDA	346
IO116P	194		GND	27		VCCIB0	321
IO117N	189		GND	33		VCCIB0	333
IO117P	190		GND	39		VCCIB0	344
IO124N	183		GND	45		VCCIB1	273
IO124P	184		GND	51		VCCIB1	285
IO125N	187		GND	57		VCCIB1	297
IO125P	188		GND	63		VCCIB2	227
IO127N	181		GND	69		VCCIB2	239
IO127P	182		GND	75		VCCIB2	245
IO128N	179		GND	81		VCCIB2	257
IO128P	180		GND	88		VCCIB3	185
Bank4			GND	89		VCCIB3	197
IO130N	172		GND	97		VCCIB3	203
IO130P	173		GND	103		VCCIB3	215
IO131N	170		GND	109		VCCIB4	144
IO131P	171		GND	115		VCCIB4	156
IO132N	166		GND	121		VCCIB4	168
IO132P	167		GND	133		VCCIB5	96
IO133N	164		GND	145		VCCIB5	108
IO133P	165		GND	151		VCCIB5	120
IO134N	160		GND	157		VCCIB6	50
IO134P	161		GND	163		VCCIB6	62
IO136N	158		GND	169		VCCIB6	68
IO136P	159		GND	176		VCCIB6	80
IO137N	154		GND	177		VCCIB7	8
IO137P	155		GND	186		VCCIB7	20
IO138N	152		GND	192		VCCIB7	26
IO138P	153		GND	198		VCCIB7	38
IO153N	146		GND	204		VPUMP	267
IO153P	147		GND	210			
IO159N/CLKEN	142		GND	216			

Port Description:

- IOxN, IOxP, ordinary IO ports, when used as differential ports, IOxN and IOxP form a differential pair.
- HCLKAP, HCLKAN, HCLKBP, HCLKBN, HCLKCP, HCLKCN, HCLKDP, HCLKDN, global hard clock, provide 4 global clocks. When single-ended clock, HCLKA/B/C/DP is available, HCLKA/B/C/DN is not available. When used for differential clock, HCLKxP and HCLKxN are used as a differential clock pair.
- CLKEP, CLKEN, CLKFP, CLKFN, CLKGP, CLKGN, CLKHP, CLKHN, global routing clocks, provide 4 global clocks. When single-ended clock, CLKE/F/G/HP are available, CLKE/F/G/HN are not available. When used for differential clock, CLKxP and CLKxN are used as a differential clock pair.
- PRA/B/C/D, internal monitoring port.
- NC, unused port.
- TDI/TMS/TCK/TDO/TRST, JTAG port.
- VCCA, core power port; GND, ground port; VCCIx, I/O power port; VCCDA, differential I/O port;
- VPUMP, isolated charge pump power supply;

Appendix B Development Environment and Development Process

The software development environment for the BSTRTAX1000-CQ352 device is Actel's Libero IDE. The main development process is as follows. For detailed process and usage instructions, please refer to the "Libero IDE Use'Guide".

Taking the v9.2 version of Libero as an example, its main interface is shown in the figure below.

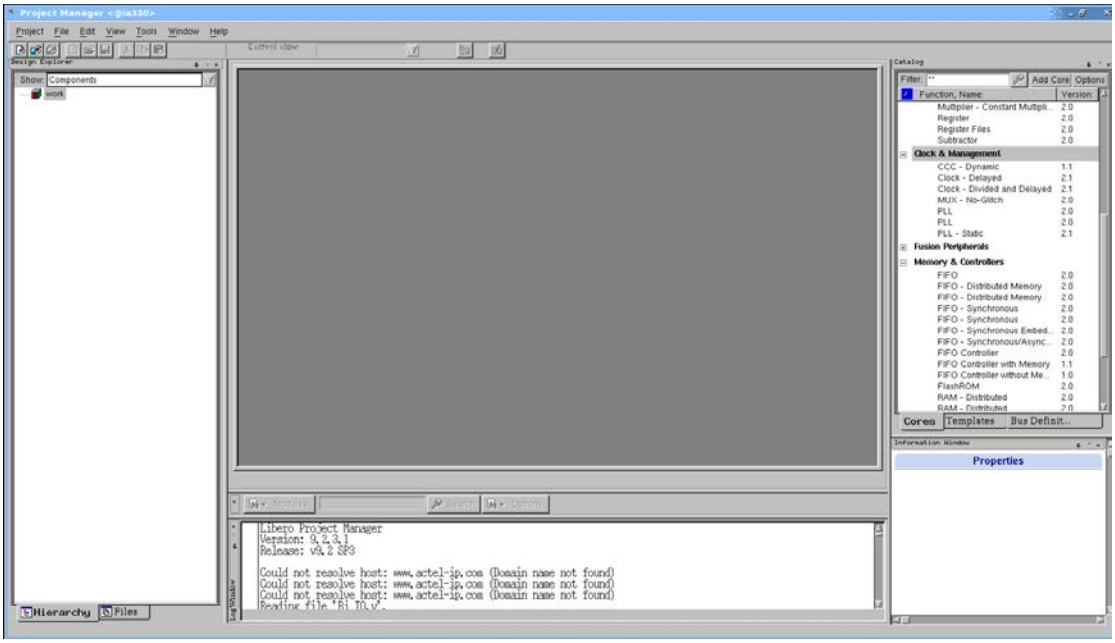


Figure B-1. Libero main interface (version: v9.2)

Click the [Project] option in the upper left corner of the stand-alone toolbar, select [New Project…], and create a new project file. As shown in the figure below, add the project file name, select the project save location, and the programming language.

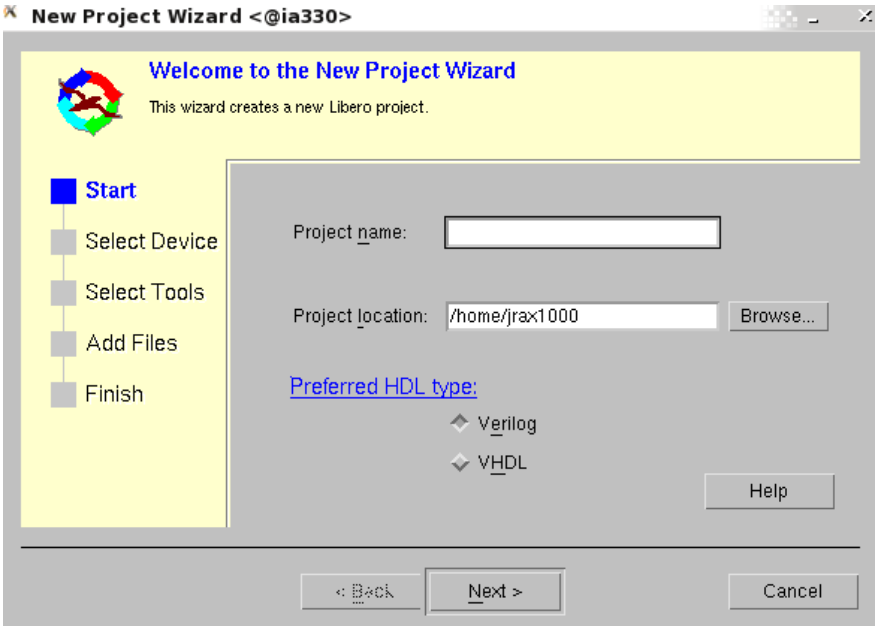


Figure B-2. New Construction Project

Select the device type and package: Family: Axcelerator - Die: RTAX1000S - Package: 352CQFP, then click Finish, as shown in the figure below.

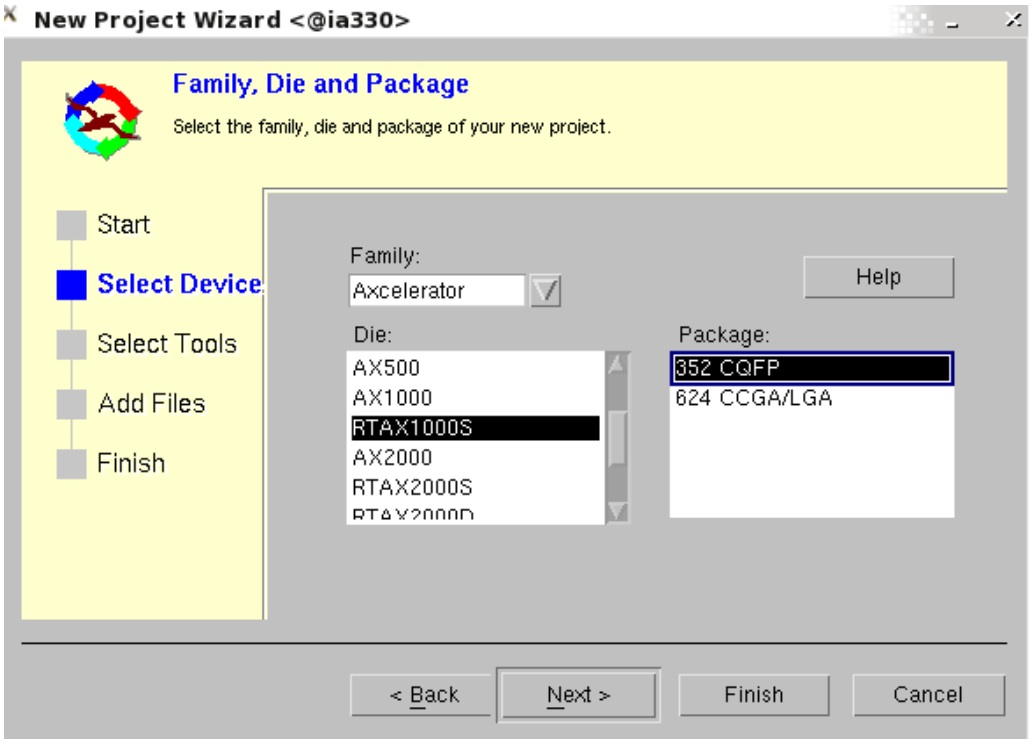


Figure B-3. Select device type and package

The following interface will then appear:

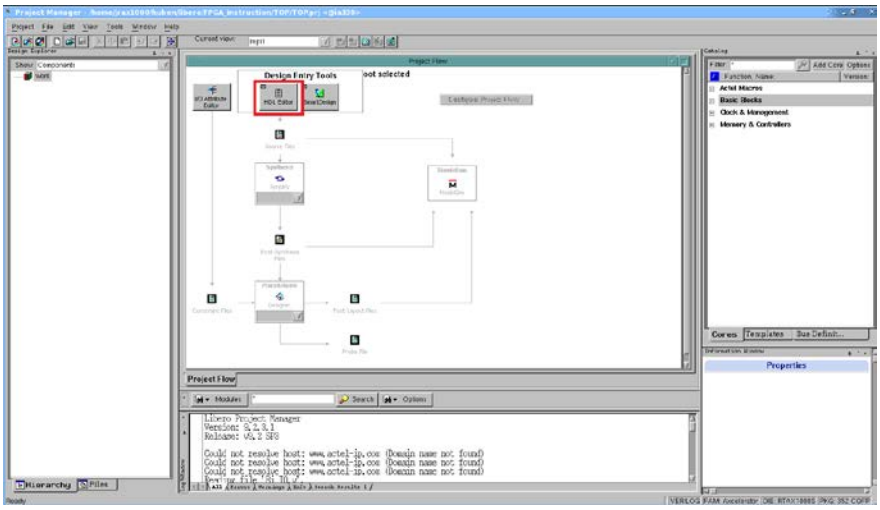


Figure B-4. IDE development environment main interface

Click [HDL Editor] (the red box in the above picture) to pop up the following interface. In this interface, select Create a New Verilog Source or VHDL Source file, write the code you need and save it.

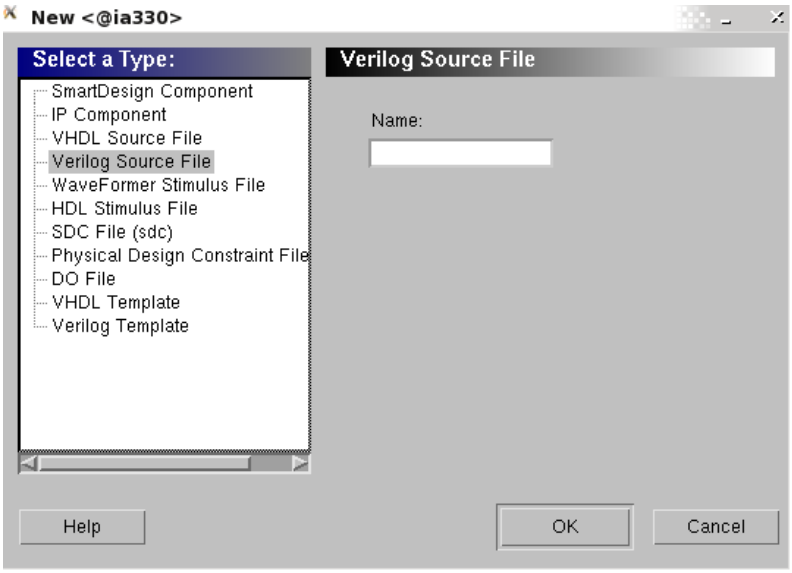


Figure B-5. New file interface

At the bottom of the software interface (as shown in the red box in the figure below), click different buttons to switch between the Source file and the main interface.

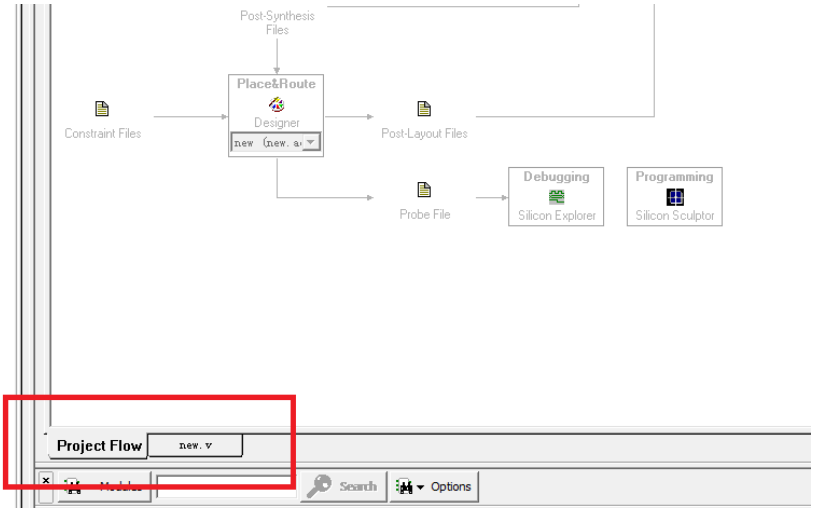


Figure B-6. IDE tab interface

If there are multiple Source files, there is no need to manually set one as the top-level file (the software automatically sets it).

After writing the program, click the [Synthesis] button in the main interface (the red box in the figure below):

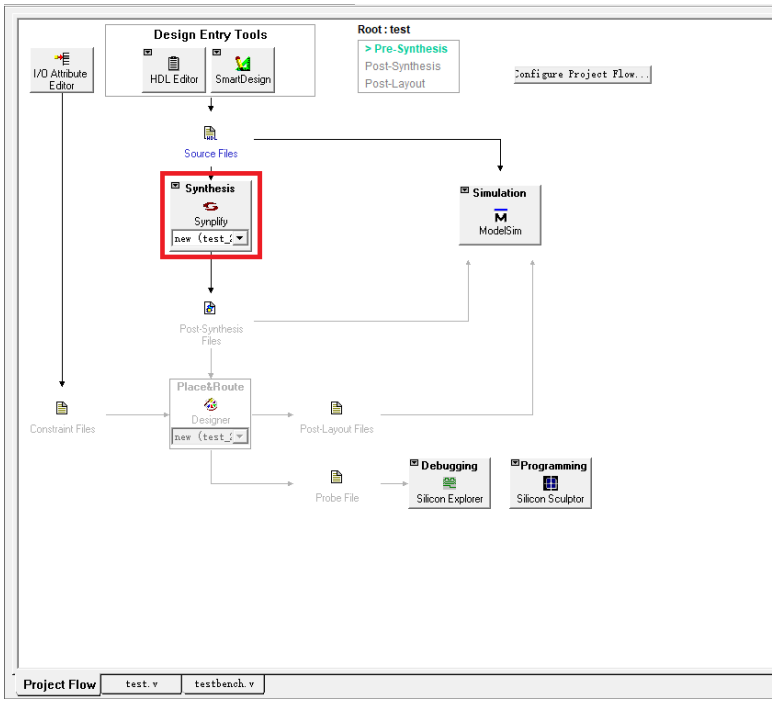


Figure B-7. Libero synthesis tool

In the pop-up interface, first confirm the device model and speed grade. If they are incorrect, you can click the red box with the number 1 in the figure below (choose one of the two), and select the RTAX1000S-CQFP352 device in the pop-up interface (the red box with the number 2), and select STD for the speed grade.

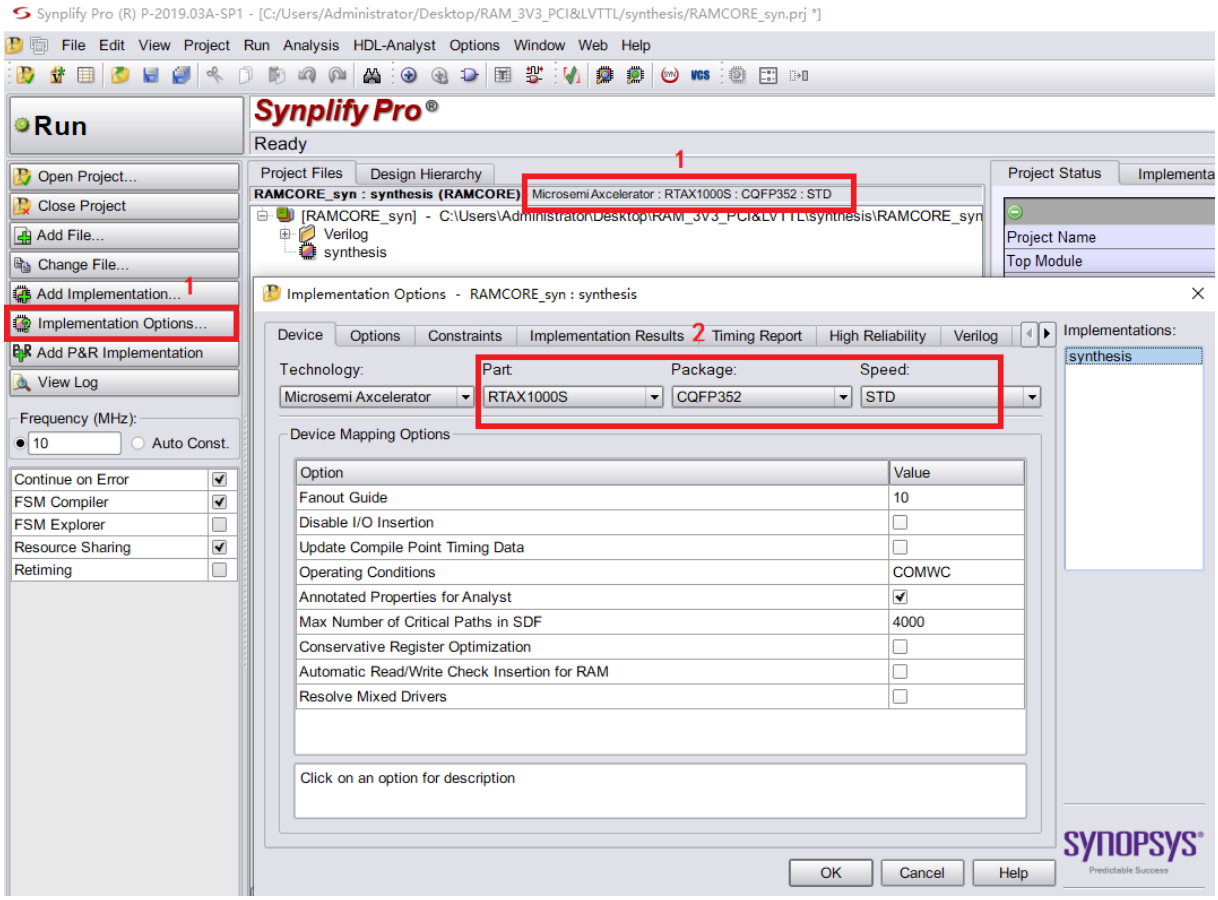


Figure B-8. (a) Synplify synthesis tool interface

Then fill in the actual running frequency of the program in [Frequency] (fill in the frequency according to the actual running frequency, do not fill it higher). Then click [Run] to run.

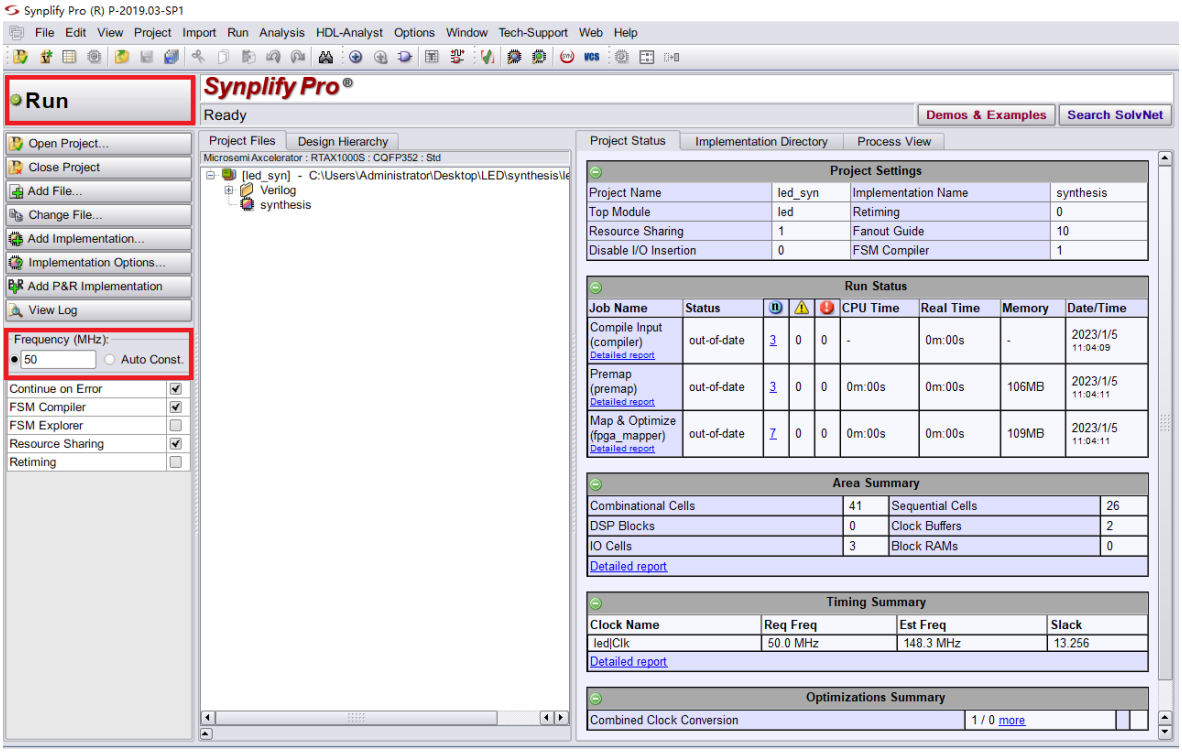


Figure B-8. (b) Synplify synthesis tool interface

If there are no errors after running, return to the main interface of the Libero software and click [Place&Route] (as shown in the red box in the figure below).

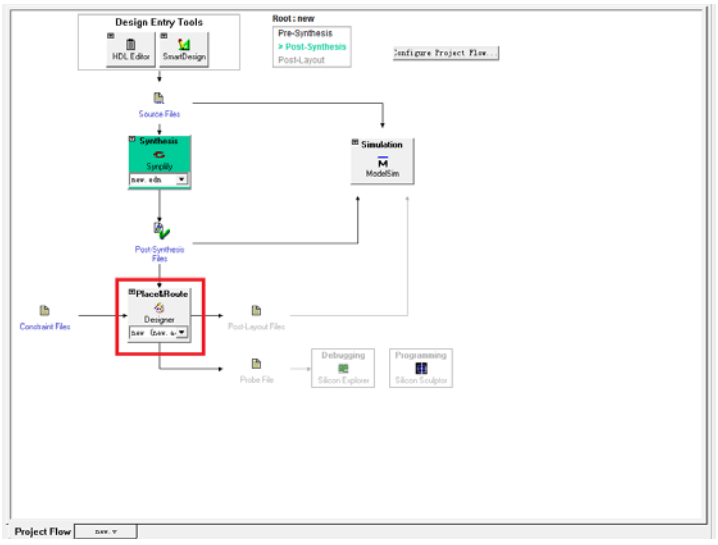


Figure B-9. Libero placement and routing tool

After clicking, the following interface will pop up (if it does not pop up, you can click the [Constraint Files] interface on the left of [Place&Route]),If no related constraint files need to be added,Click [OK] to skip.

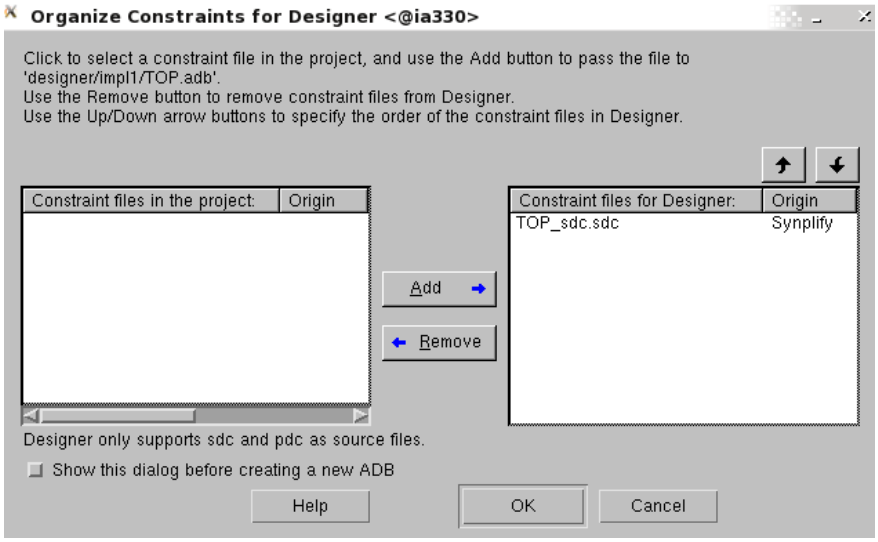


Figure B-10. Adding a timing constraint file

The following interface will appear next. [Speed] uses the default setting STD, and the [Die voltage] option is the default 1.5V.

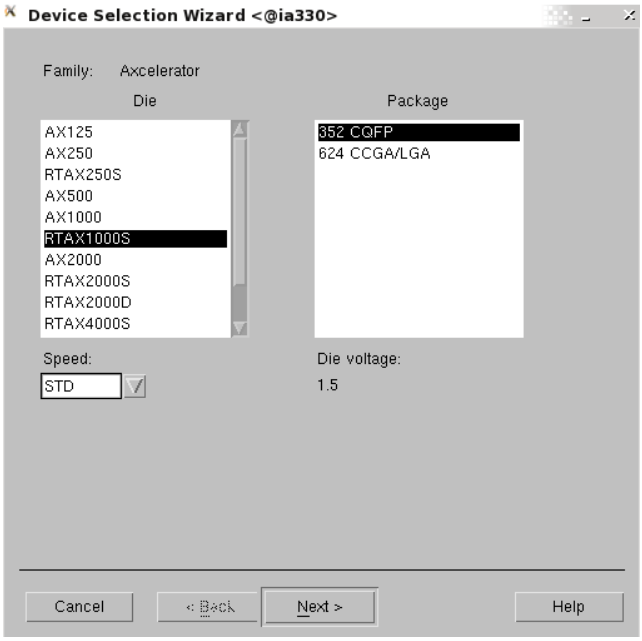


Figure B-11. Select device speed grade and operating voltage

Then click [Next] and the following interface will appear. In this interface, select the level standard of the I/O port.Note that since the 3.3V PCI level does not support hot-swap cold backup (see the relevant instructions below Table 3 in 4.3), do not select 3.3V PCI when the port needs to be burned to 3.3V level.

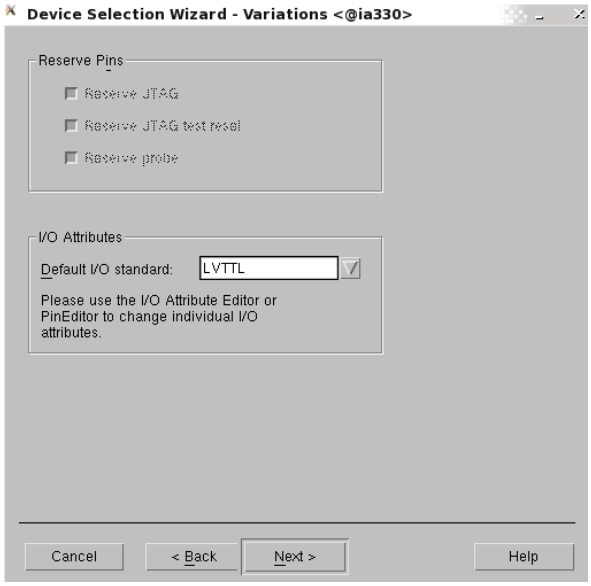


Figure B-12. I/O port level standard selection

Click [Next] and set the operating temperature and voltage range in the interface that appears. (In fact, you don’t need to set it, just click [Finish]), then just click [Finish].

Figure B-13. Operating temperature and voltage range settings

An Error window may appear afterwards (as shown in the figure below). Ignore it and just click [OK].

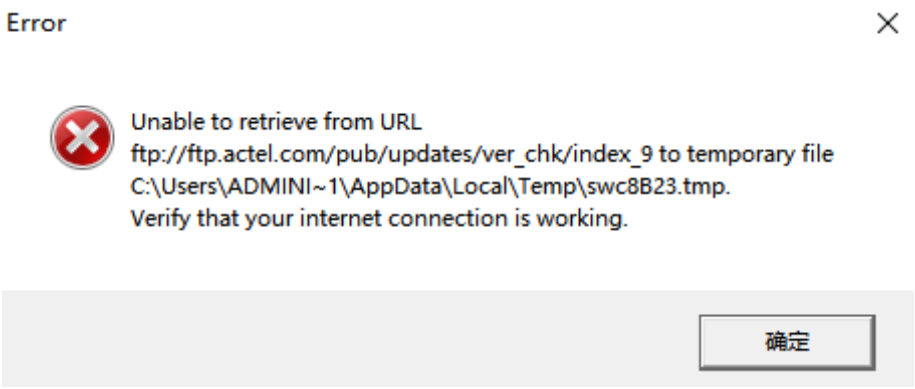


Figure B-14. Error window

In the next interface, select [Compile] (the red box in the figure below) to compile.

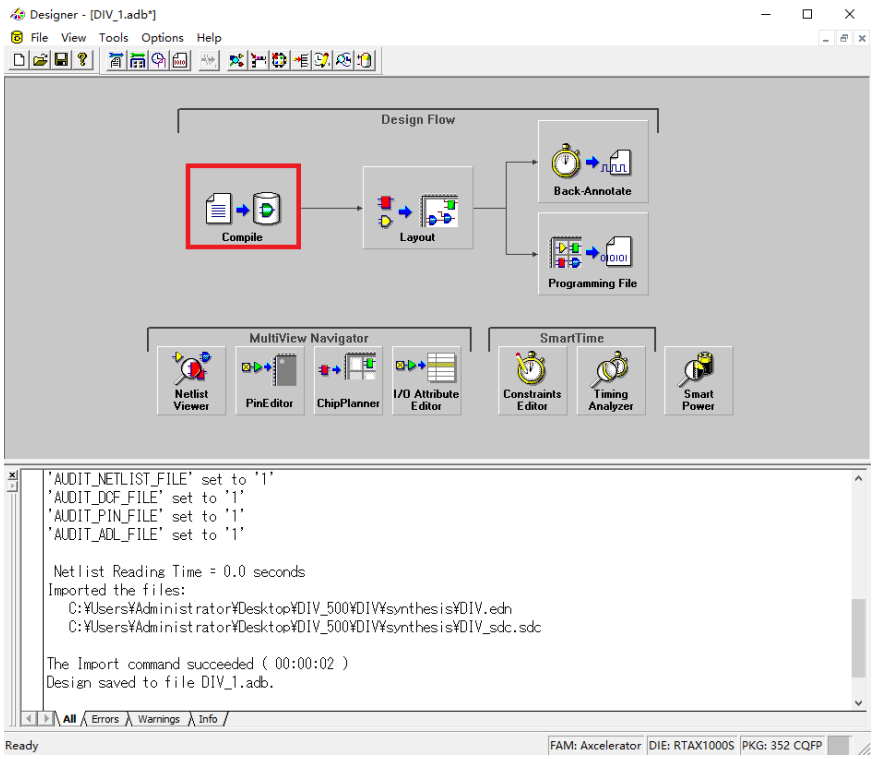


Figure B-15. Compilation interface

After clicking [Compile], the following dialog box will pop up, just click OK.

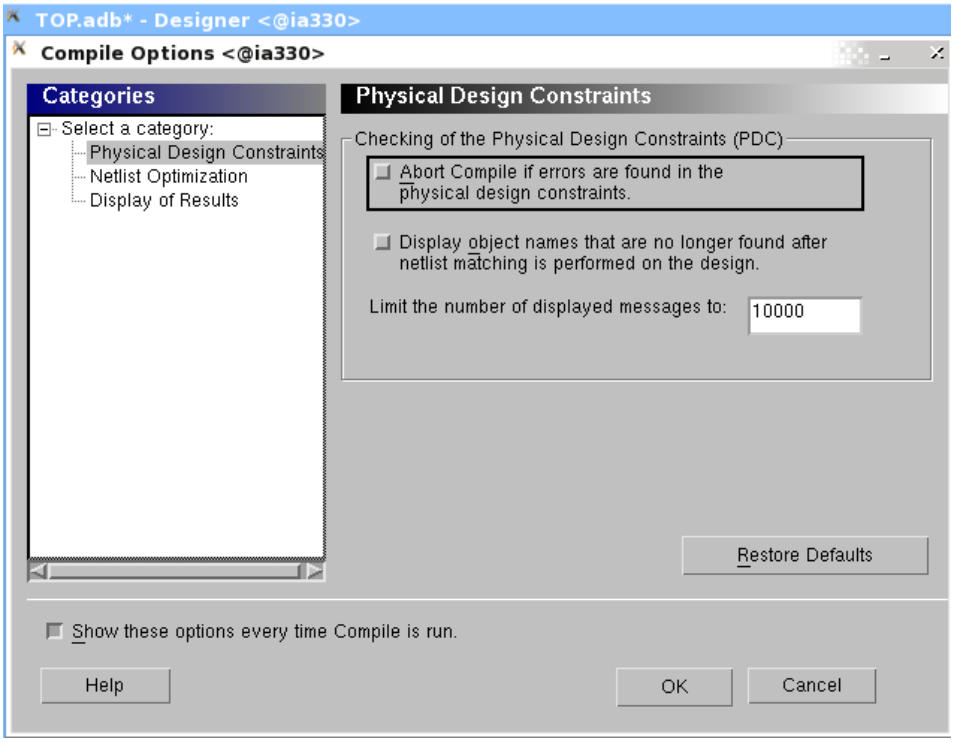


Figure B-16. Compile options

If there are no compilation errors, click [I/O Attribute Editor] to set the pin attributes:

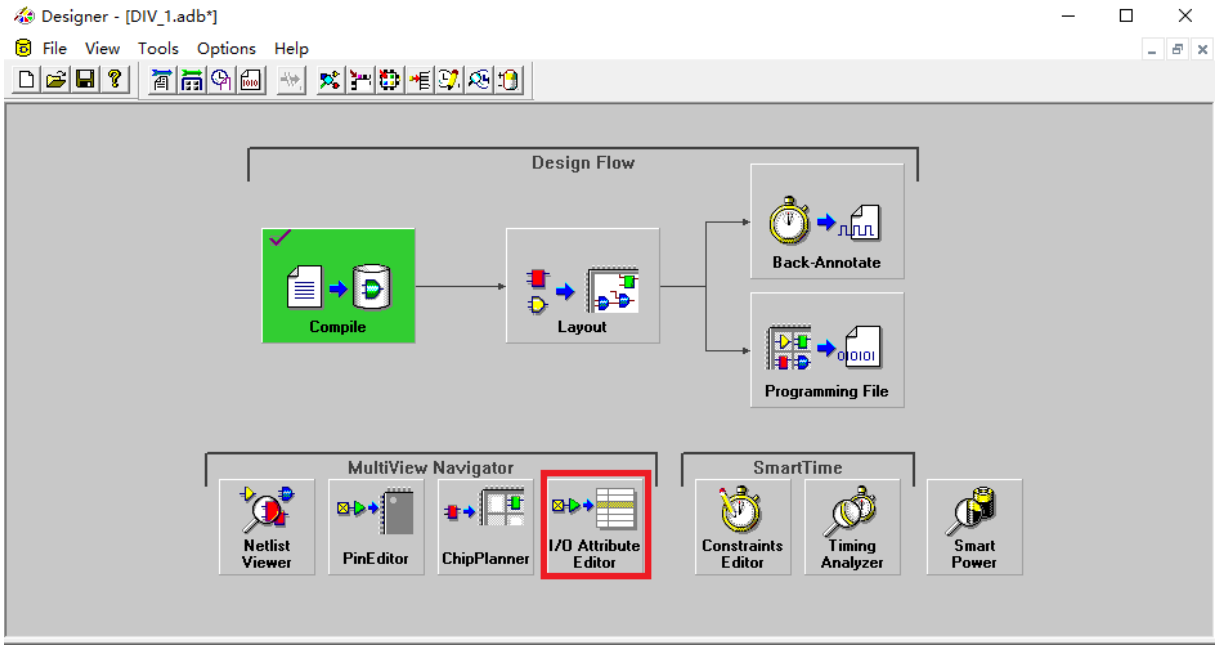


Figure B-17. Pin attribute definition

Then the following interface will pop up, where [Port Name] is the port name defined by the user, [Pin Number] is the pin number of the BSTRTAX1000-CQ352 circuit, [I/O Standard] is the level standard of the I/O port, [Slew] is the output falling edge slope, [Resistor Pull] is the pull-up and pull-down status after the port is powered on, which can be set to high impedance, weak pull-up or weak pull-down, and [Hot Swappable] indicates whether it is compatible with the hot swap function (3.3V PCI does not support it).

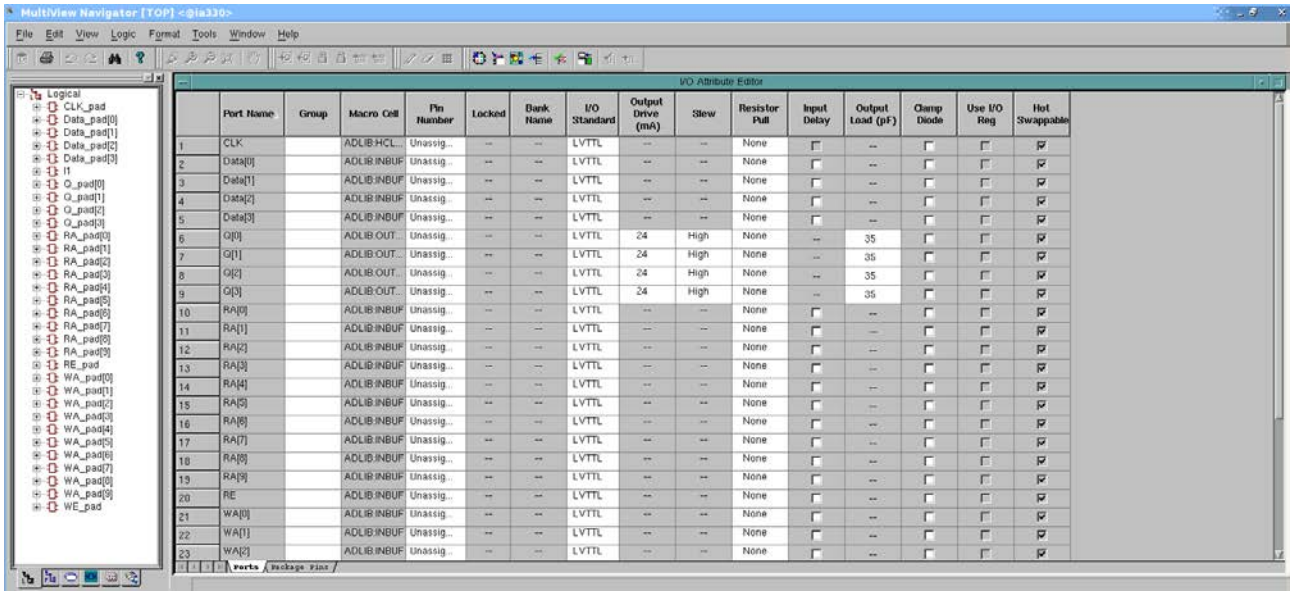


Figure B-18. Pin property settings

If you need to modify the level standard of a certain BANK, click [ChipPlanner] in the interface below.

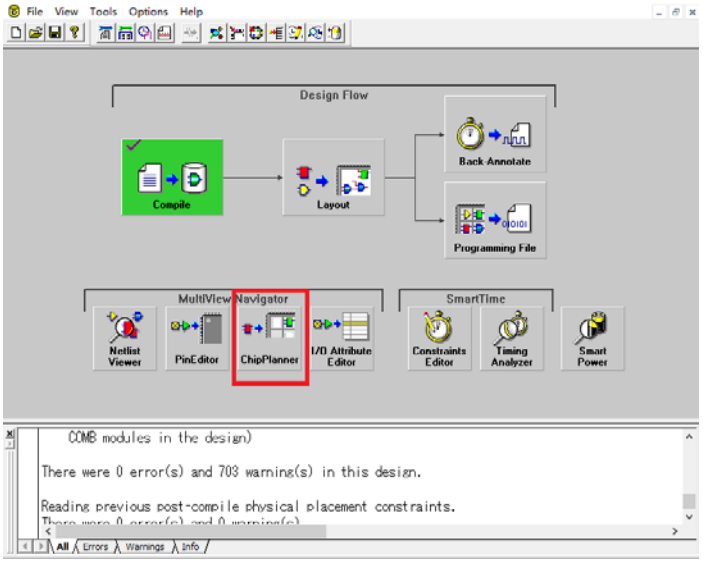


Figure B-19. ChipPlanner button

Then the following interface will pop up, which is equivalent to the internal layout of the circuit. Then place the mouse outside the chip layout (the red box in the figure), right-click the mouse, and select [I/O bank settings] in the pop-up menu..

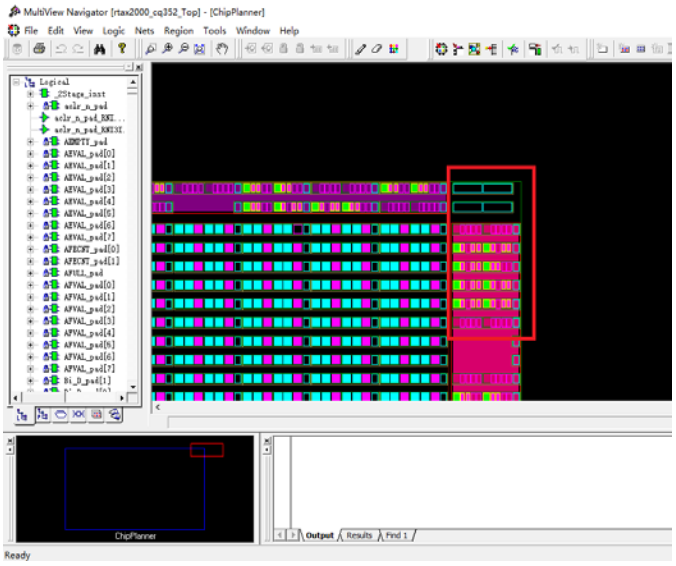


Figure B-20. ChipPlanner interface

After clicking [I/O bank settings], the dialog box shown in the figure below pops up. In the [Choose Bank] option, you can select the bank number, and in the [Select all

technologies that the bank should support] interface, check or uncheck a certain level standard to achieve the purpose of modifying a certain bank level standard.

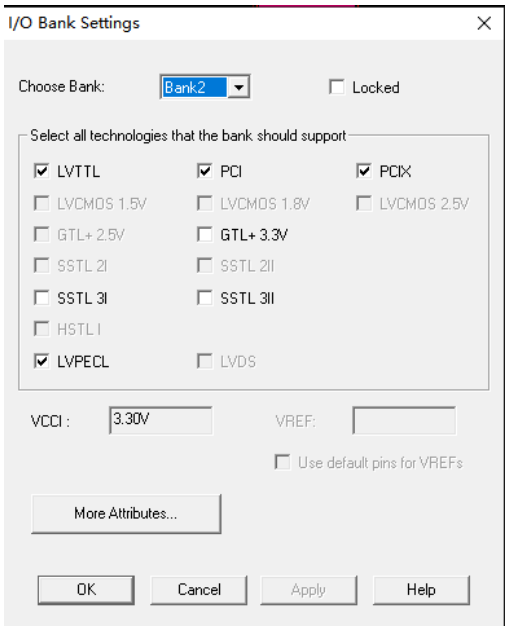


Figure B-21. I/O bank settings interface

After the configuration is completed, return to the previous interface and click [Layout] to perform layout and routing.

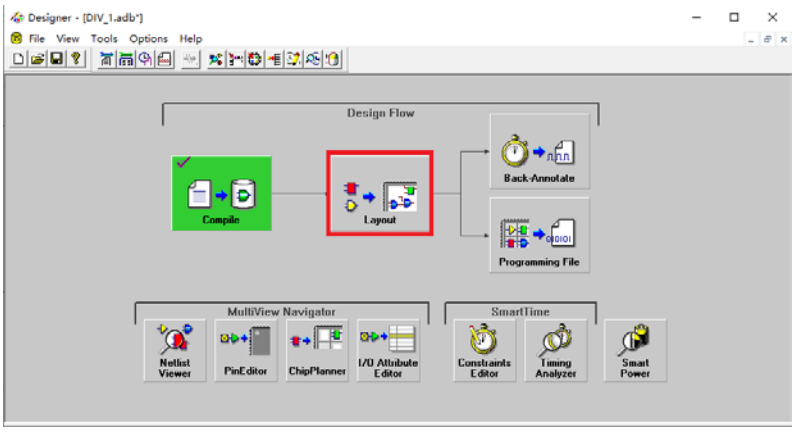


Figure B-22. Logical resource layout

In the pop-up interface (as shown below), select [OK] (the settings are generally left as default).

Figure B-23. Layout and routing options

Then click the [Timing Analyzer] button to observe the timing analysis results after layout and routing.

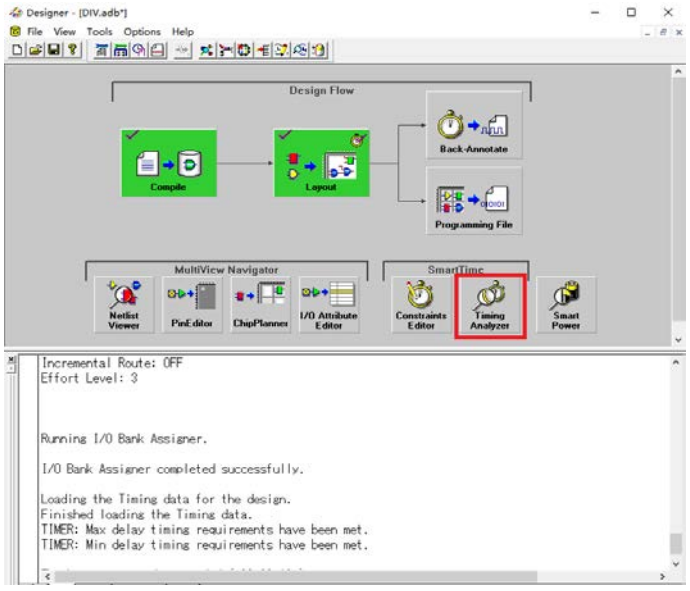


Figure B-24. Timing Analyzer Buttons

After clicking, the following interface pops up, where you can see information including device model, speed grade, operating temperature range, etc.:

From the simulation results in the figure below, we can see that the required speed [Required Frequency (MHz)] is 20MHz, and the actual maximum speed [Frequency (MHz)] is 22.482MHz. In addition, all the green √s appear on the left side of the interface, and there is no red ×, indicating that the timing of the program meets the requirements.

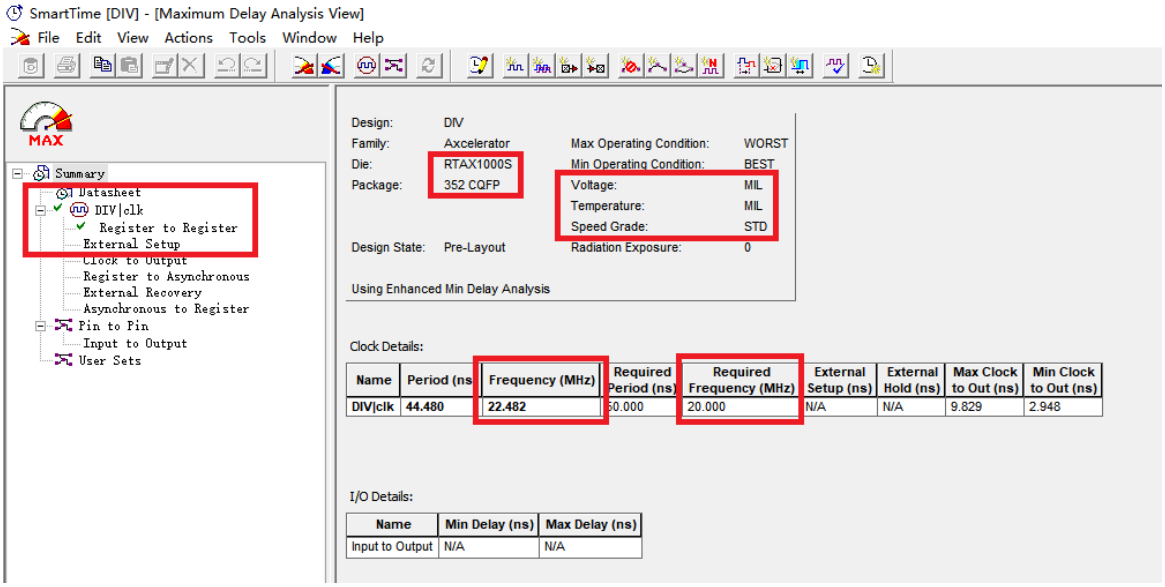


Figure B-25. Timing Analysis Pass Interface

If the timing analysis results do not meet expectations, a red × will appear on the left side of the interface, and the actual maximum rate that can be achieved [Frequency (MHz)] will also be lower than the required speed [Required Frequency (MHz)].

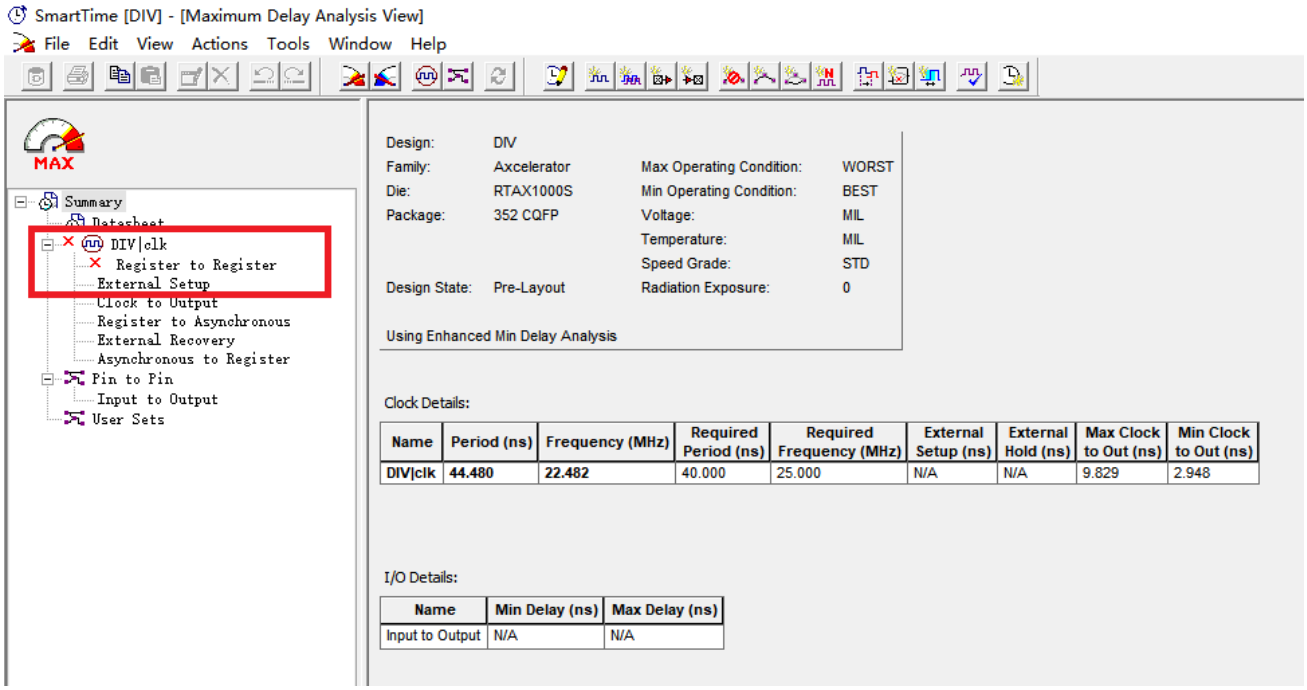


Figure B-26. Timing Analysis Failed Interface

At this time, click the red × on the left side of the interface, and the following interface will pop up. The red part is the code that does not meet the timing requirements, usually some counters with too large bit width. Optimize the corresponding code in the program until the timing requirements are met.

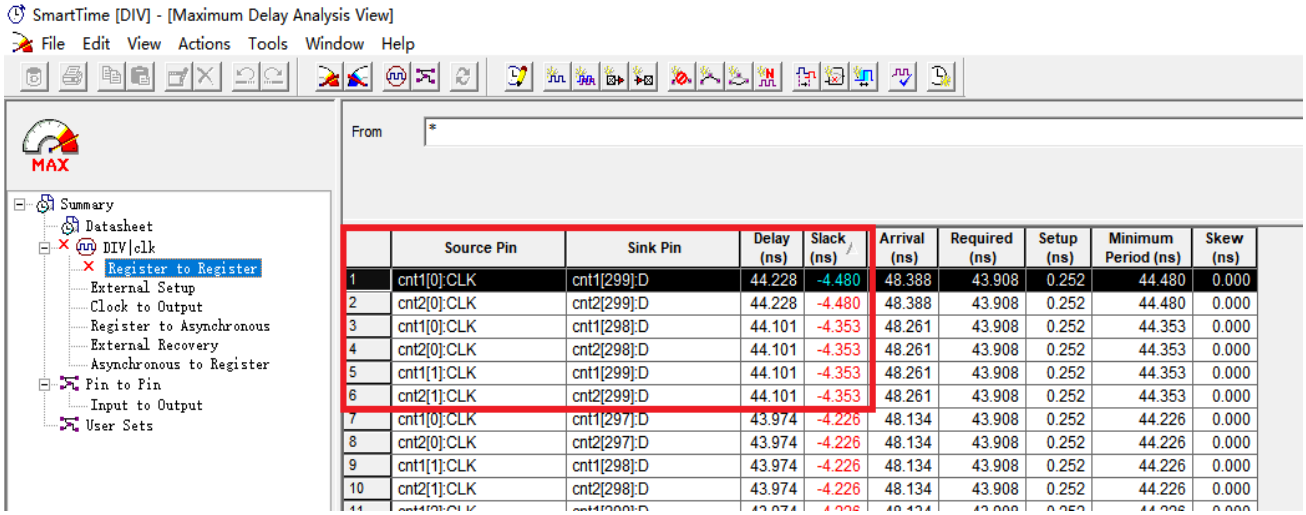


Figure B-27. Timing Analysis Failed Interface

In addition, the default pop-up interface of the timing analysis is the result under the MAX condition. We can click the button shown in the figure below to observe the timing analysis results under the Min condition. Similarly, the green √ appears on the left side of the interface, and there is no red ×, which means that the timing of the program meets the requirements.

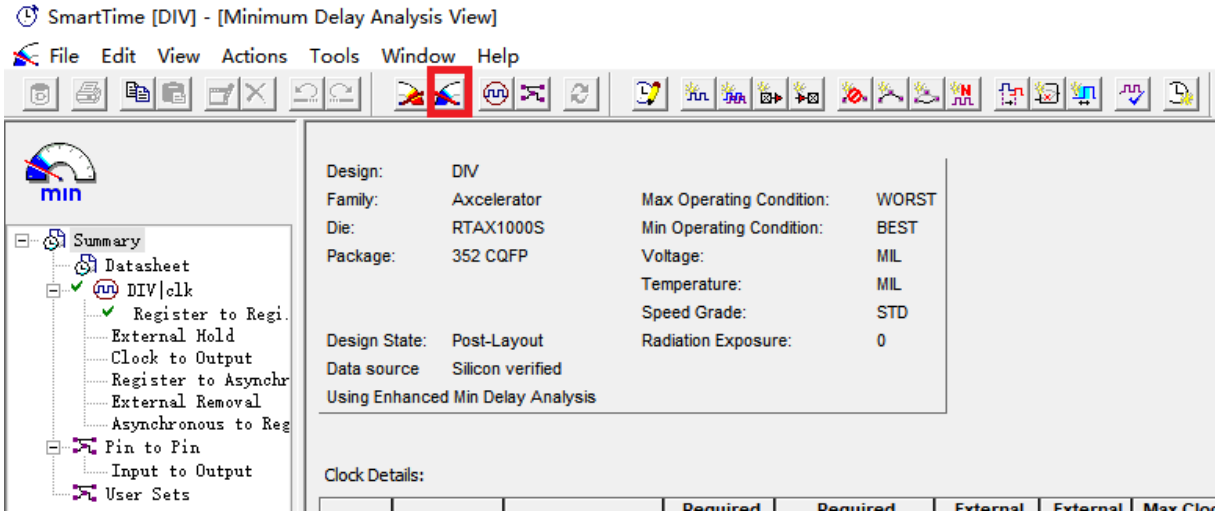


Figure B-28. Enter the Min condition timing analysis interface button

Max and MinTiming AnalysisallAfter passing, call the Modelsim software that comes with Libero (you can also call other simulation software for verification after Libero generates the post-simulation netlist data) for post-simulation verification.

Before post-simulation verification, you need to complete the writing of the testbench file. Then enter the [Files] interface in the lower left corner of the software:

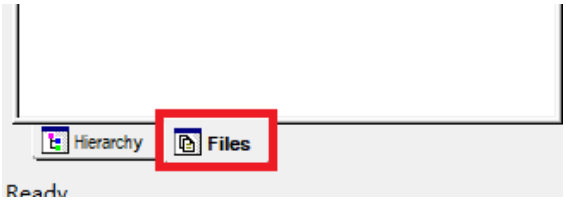


Figure B-29.【Files】Interface

Then load the testbench file into the [Stimulus Files] directory:

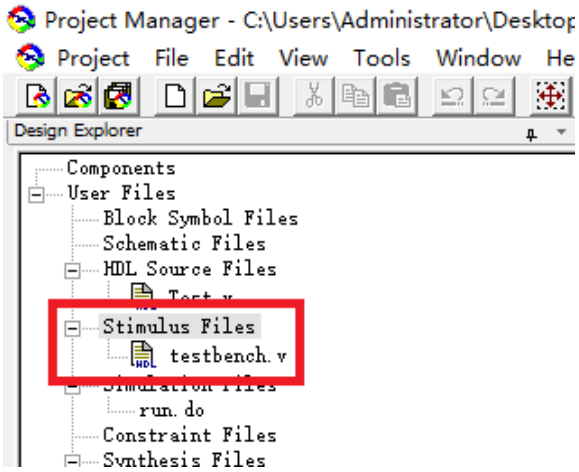


Figure B-30. Stimulus Files】Directory

Then click Back-Annotate to generate the post-simulation netlist data. Click “OK” in the pop-up window to confirm.

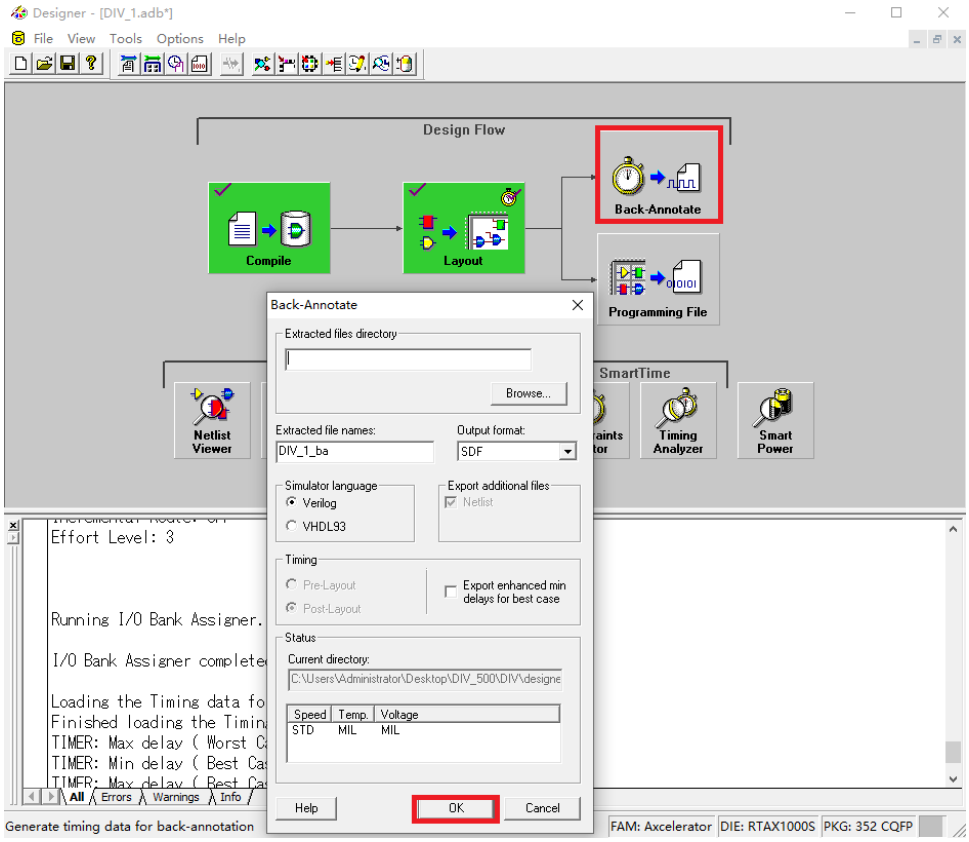


Figure B-31. Back-Annotate interface

At this point, the Back-Annotate icon is green, indicating that the post-simulation netlist has been generated.

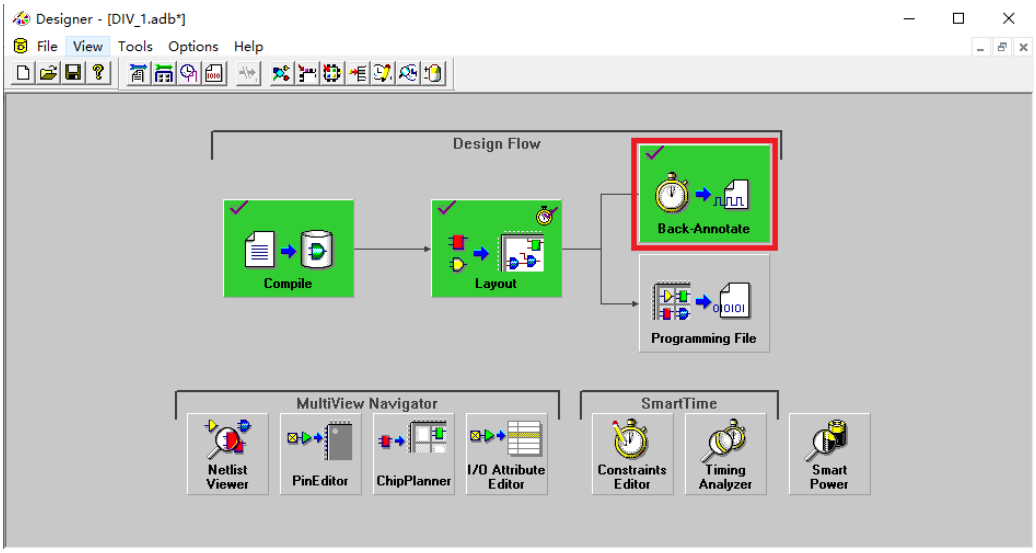


Figure B-32.Back-Annotate interface

Then, save and exit the interface.

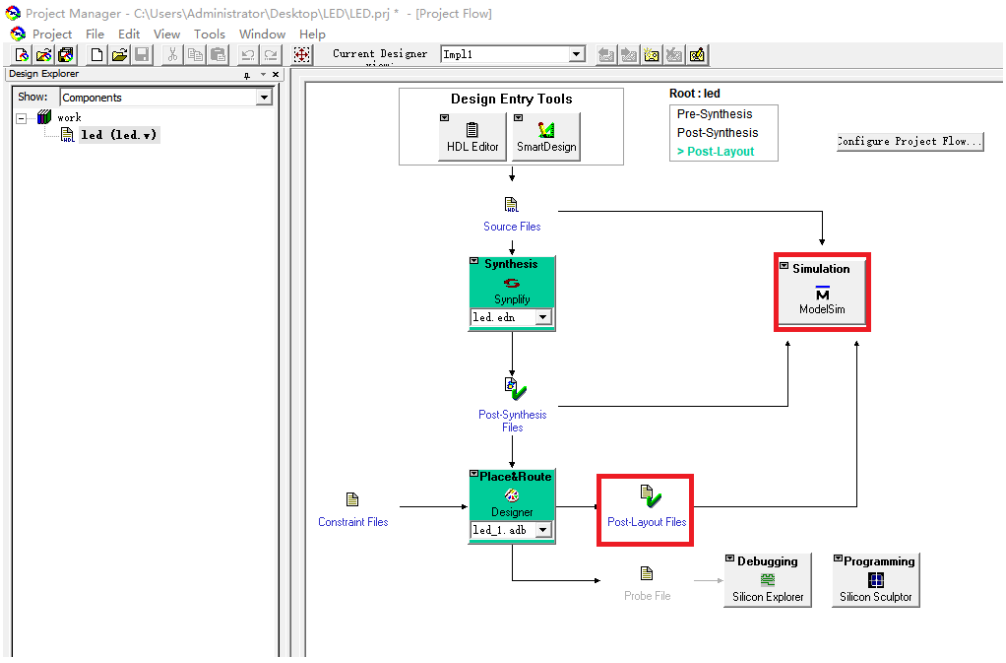


Figure B-33. Modelsim Interface

In the interface above, we can see a green check mark in the middle of Post-Layout Files. At this time, when we call the Modelsim software that comes with Libero, we get the "post-simulation" waveform.

If we did not click Back-Annotate in the previous step to generate the post-simulation netlist data, then Post-Layout Files will display a yellow exclamation mark. At this time, if we call the Modelsim software that comes with Libero, we will get the waveform of the "pre-simulation".

Next, right-click on Simulation and select Options.... The following interface pops up:

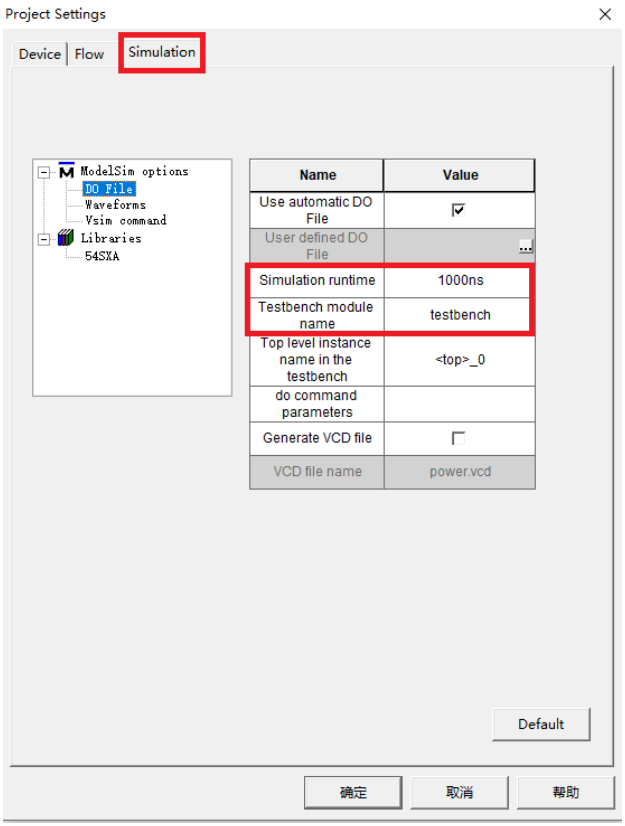


Figure B-34. [Options...] interface

The red box in the figure above shows the default name of the testbench file and the top-level module instantiated in the testbench file. If it does not match the name of the actual code, it needs to be modified, otherwise an error will be reported during

simulation - the default name of the testbench file is "testbench"; the default name of the top-level module after instantiation is "top-level module name_0".

After the settings are completed, click Figure B-33The [Simulation] button in the interface will call the Modelsim tool and display the corresponding waveform.

In addition, when performing post-simulation operations, you can select three conditions: Min, Typ, and Max, as shown in the figure below. Under the three conditions, the post-simulation passes, indicating that the program functions normally.

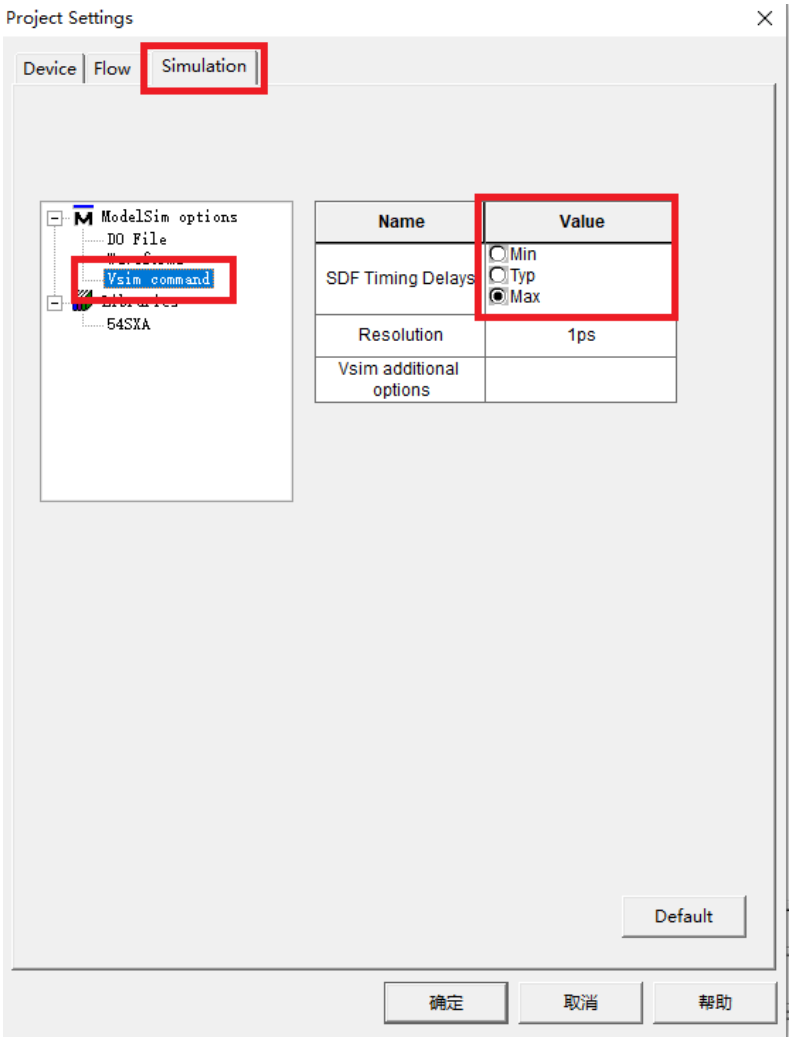


Figure B-35. [Options...] interface

After the timing analysis and post-simulation verification are passed, click [Programming file] to generate the .afm file for burning.

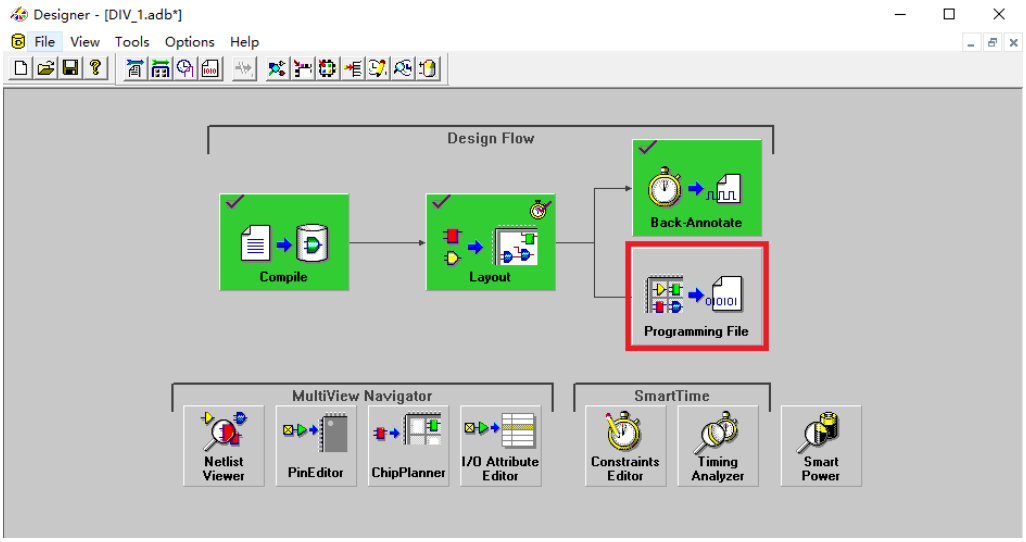


Figure B-36. Generate flash file

In the pop-up dialog box, set the save location and name of the .afm file.

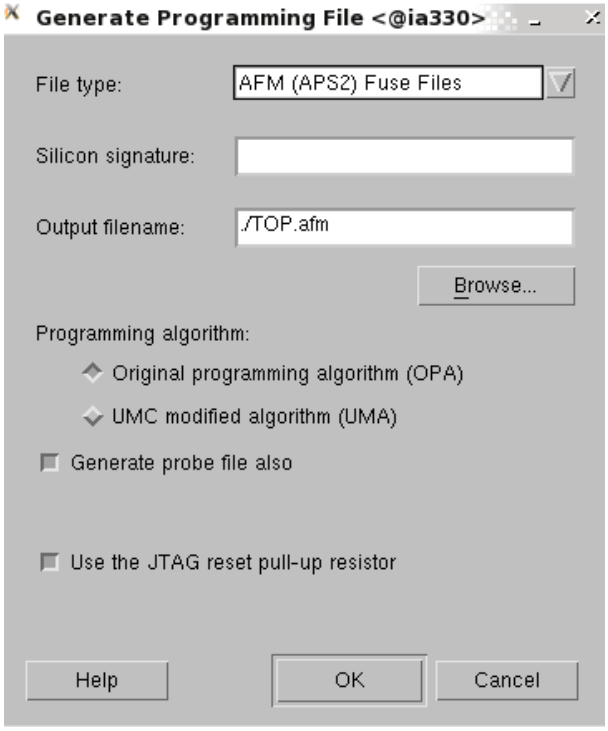


Figure B-37. Burn file save location and name

Appendix C Improving Device Speed

If after timing analysis, it is found that the device cannot run at the required target frequency, there are several ways to increase the device's operating speed without modifying the code.

Check Timing-driven:

When Layout is in the Compile interface, check Timing-driven in the pop-up interface.

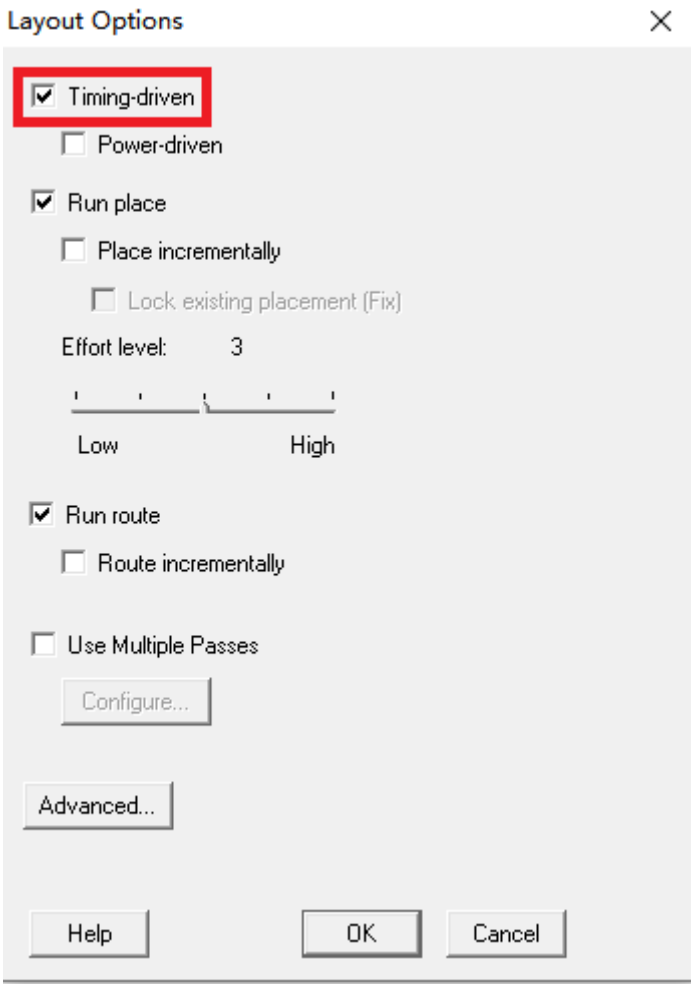


Figure C-1. Layout Options

Check Use Multiple Passes

After Layout, when the following interface pops up, check [Use Multiple Passes] and click [Configure] to set it.

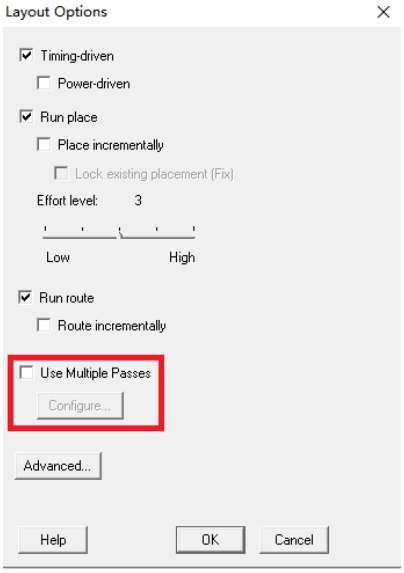


Figure C-2. Use Multiple Passes check box

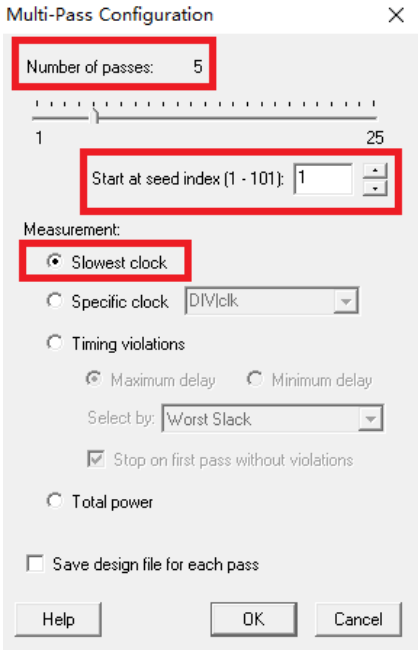


Figure C-3. Multi-Pass Configuration interface

Use Multiple Passes means using multi-channel layout mode, and the software selects an optimal solution from multiple layout and routing results.

In the configuration interface above, [Number of passes] refers to the number of iterations, which can be selected from 1 to 25 times. Software defaultIt is recommended to select 5 times. The more iterations you run, the longer it takes.

[Start at seed index] is to set the seed index, usually the default value is sufficient. This option means that there are 101 layout and routing algorithms, and you choose which algorithm to start layout and routing from.

[Slowest clock] means using the slowest clock frequency as a performance reference for layout and routing, that is, optimizing the slowest clock. The default is to select [Slowest clock] Users can also select options such as [Timing violations]. For specific instructions, click [Help] in the dialog box to see detailed instructions.

After checking Use Multiple Passes, the program placement and routing takes a very long time.

Modify the temperature range

In Libero software, the default operating temperature range of the device is -55℃~+125℃(Note that this temperature refers to the junction temperature of the device, that is, the internal temperature of the device after it is working, not the external ambient temperature).If the maximum junction temperature of the device is only 70℃,Then we can modify the deviceJunction temperaturerange, the highestJunction temperatureReduce in order to increase the device operating speed. In the Compile interface, click [Tools] - [Device Selection] in the menu bar.

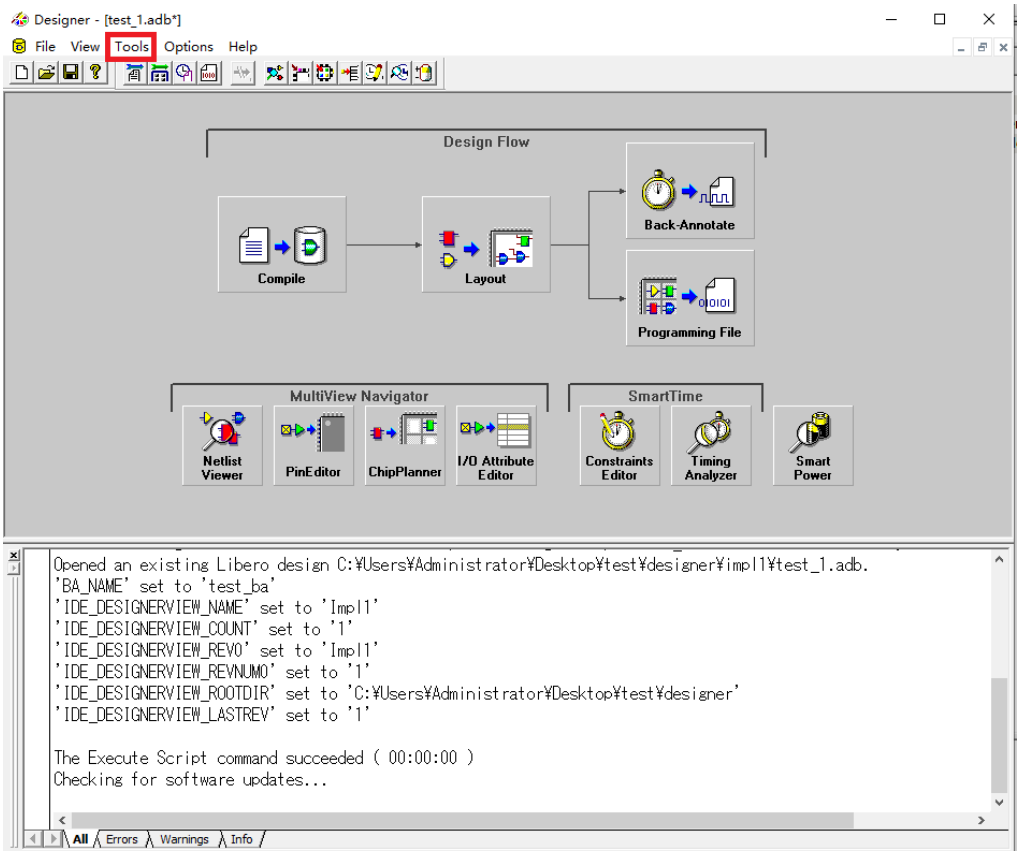


Figure C-4. Compile interface

Click [Next] in the pop-up interface until the interface shown in Figure C-5 appears. Select [Custom] in [Range], and then you can set the junction temperature range yourself, for example, you can set the junction temperature to -55℃~+100℃. After compiling, perform timing analysis and you can see that the device's operating speed has increased.

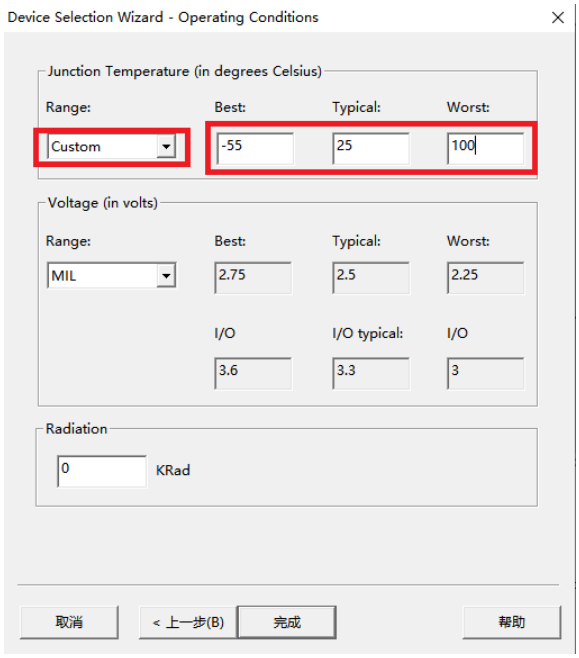


Figure C-5 .Device junction temperatureSettings interface

Appendix D Programmer and Programming Process

Programmer selection: BP's "Universal Device Programmer" or Actel's "Actel Device Programmer" (produced by BP). The recommended programmer model is Silicon Sculptor 3, and the recommended software is BPWin V6.4.0, or other newer versions of software. The software can be downloaded from the Microsemi official website, or contact us to provide software CDs.

The programming process is as follows (taking V6.4.0 as an example):

The BPWin V6.4.0 interface is shown in the figure below. Click the [Device] option in the figure below and select the circuit model: Actel BSTRTAX1000-CQ352.

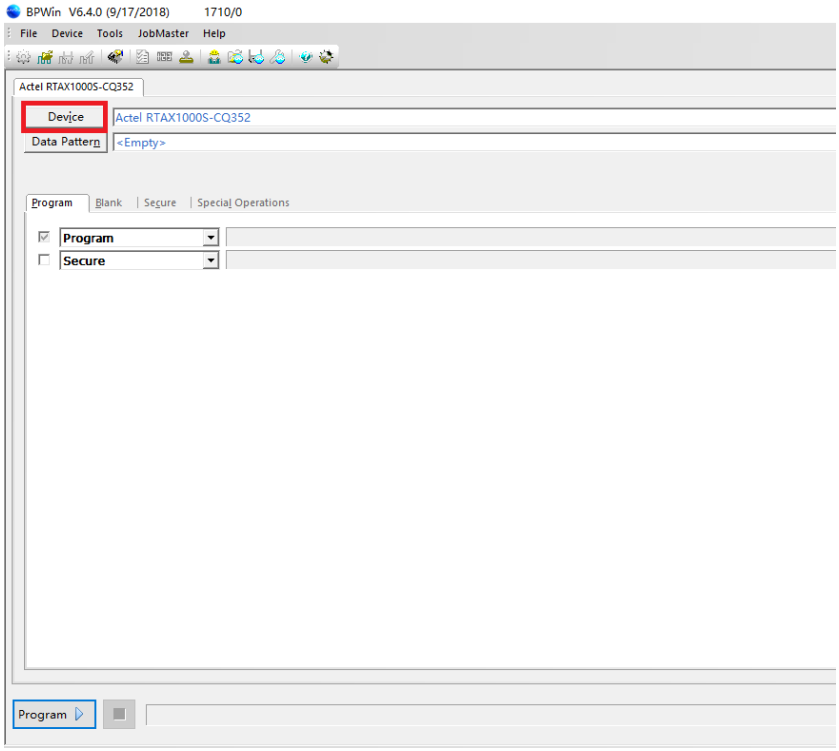


Figure D-1. BPWin V6.4.0 main interface

After the programmer passes the power-on self-test, select [Data Pattern] and click [Open] in the pop-up interface.

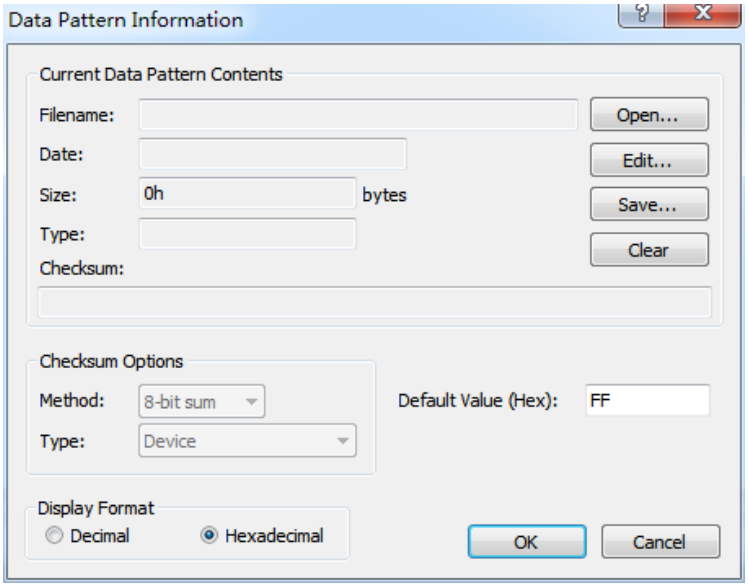


Figure D-2. Data Pattern Information

Then select [Browse] in the pop-up interface to import the .afm file compiled in the Libero software.

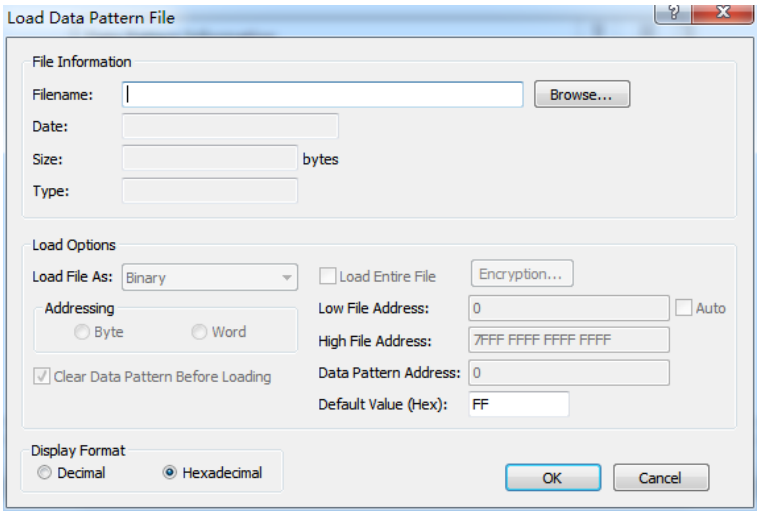


Figure D-3. Loading .afm files

Then place the circuit on the programmer, select the [Blank] tab, and perform contact test and air check test in this tab.

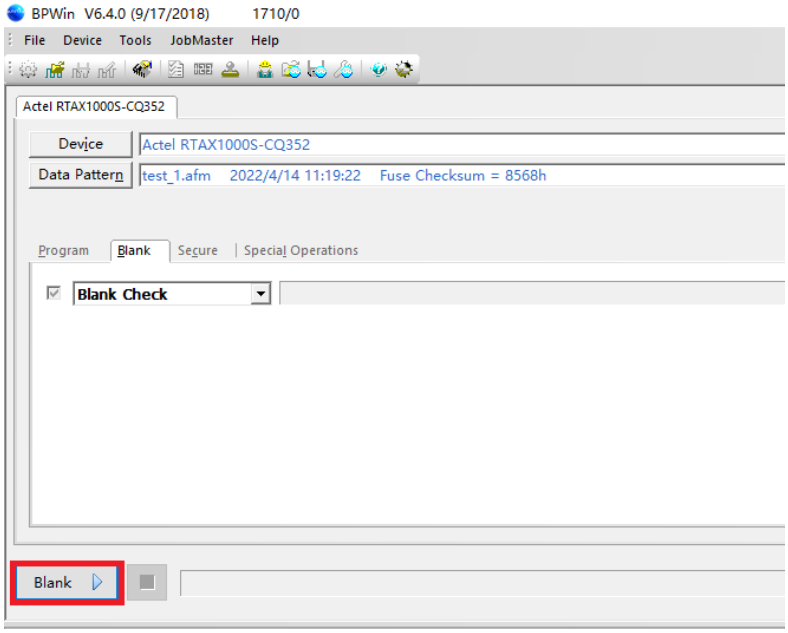


Figure D-4. [Blank] Blank check tab interface

After the contact test and air check test are passed, click [Program] to start burning. Determine whether the burning is successful according to the burning progress bar and the prompt information at the bottom of the interface.

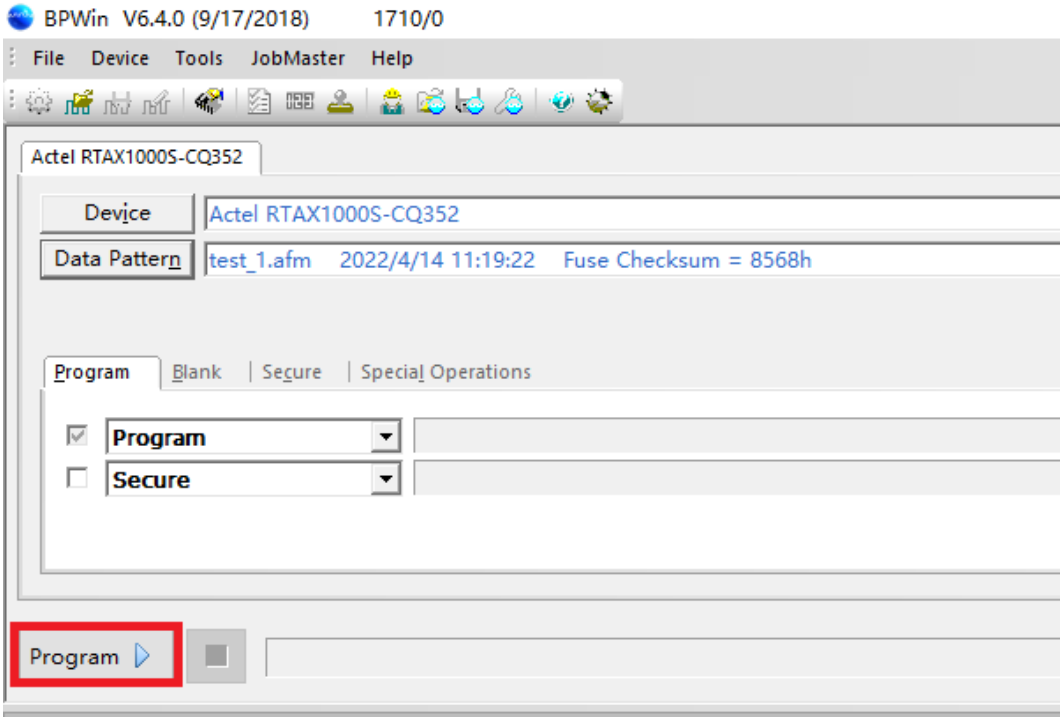


Figure D-5 Burning interface

Appendix E Power Consumption Evaluation Instructions

The BSTRTAX1000-CQ352 power consumption evaluation software is in the Smart Power of the Place&Route interface in the Libero IDE, as shown in the red box in the figure below.

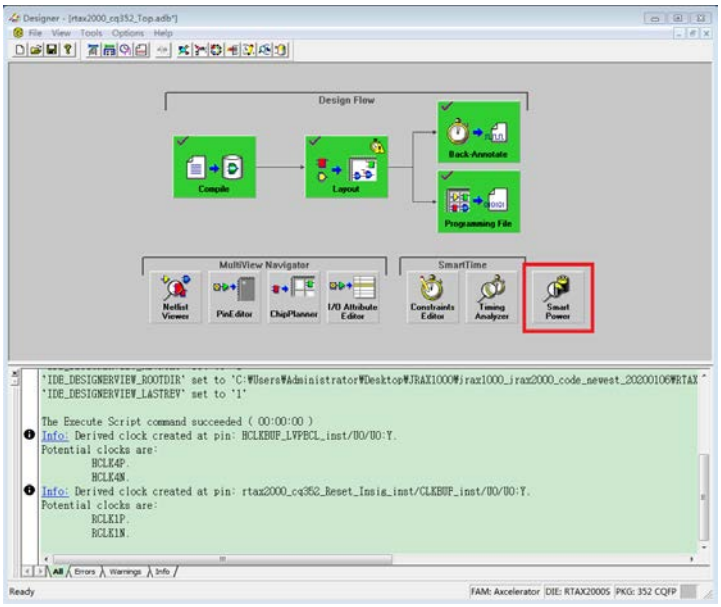


Figure E-1. Power consumption evaluation software

When the entire project design is completed, you can click to open the Smart Power software to perform power consumption evaluation. When you open the Smart Power software for the first time, the software will perform power consumption evaluation on the current project by default based on the constraints and configurations in the Constrains Editor. The software interface and power consumption evaluation results are shown in the figure below.

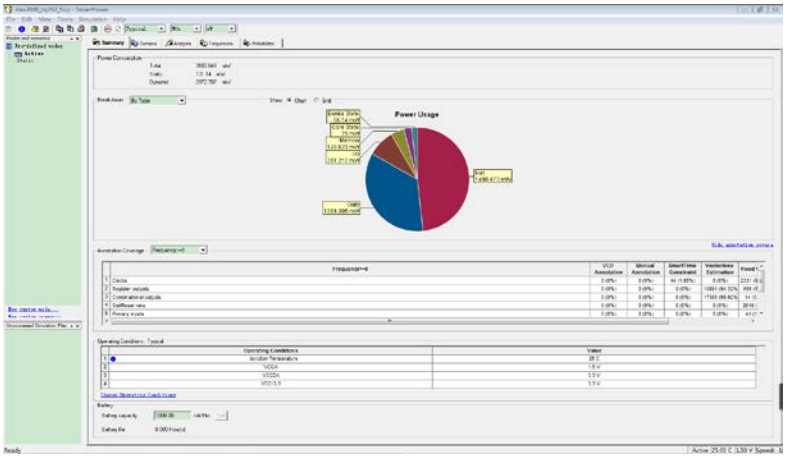


Figure E-2. Power consumption evaluation software interface

The top of the software interface is the toolbar of the software. As shown in the figure below, several commonly used tools are marked. In the condition setting, you can set the parameters of power consumption evaluation such as temperature, thermal resistance, and voltage. Users can set the corresponding settings according to the tool requirements, and generally the default values are sufficient. Generate a report to export the detailed results of the current project power consumption evaluation in the form of TXT or CSV files. Initialization configuration is used to quickly set condition parameters such as frequency and probability of power consumption evaluation. Update is used to re-evaluate power consumption. After the user changes some settings on the main interface, you can click this tool to recalculate. The condition selection can drop down to select Worst, Typical, and Best conditions, which correspond to different voltage and temperature settings. The unit selection can drop down to select the calculation units of Hz, KHz, MHz, W, mW, and μW.

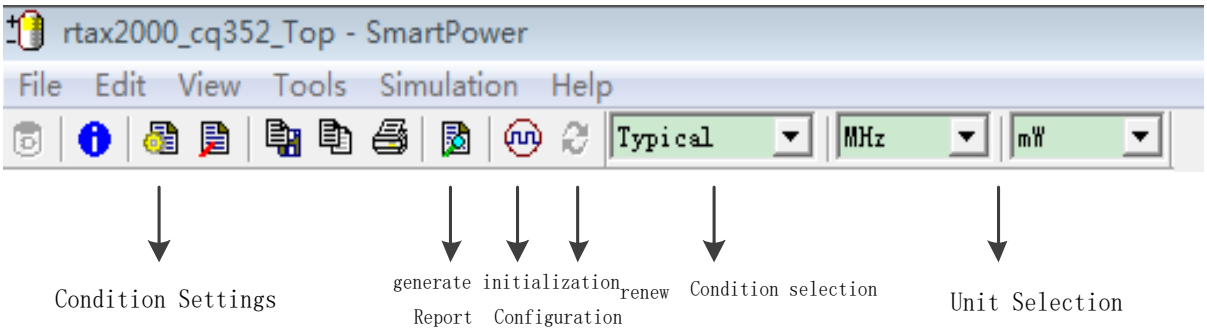


Figure E-3. Power consumption evaluation software toolbar

Normally, you only need to initialize the configuration to complete the power consumption evaluation under normal conditions. The following figure shows the initialization configuration interface, where you can configure General, Clocks, and Set of pins. In General, you can choose the evaluation method for unannotated pins: non-vector analysis or fixed value.

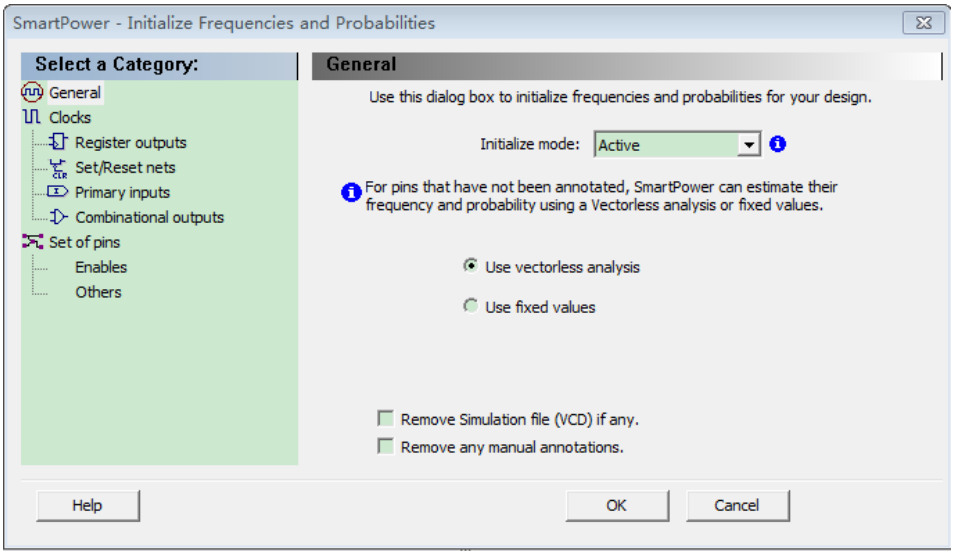


Figure E-4. Initialization configuration interface

In Clocks, you can configure the clock frequency and period. As shown in the figure below, you can choose to configure according to the clock constraint file or manually input the frequency setting. For Register outputs, Set/Reset nets, Primary inputs, and Combinational outputs, users can also choose non-vector analysis or fixed values, and set the trigger rate and probability. The configuration in Set of pins is the same as the Clocks configuration.

After setting the above items, click OK and the software will re-evaluate the power consumption according to the set conditions. This initial configuration power consumption evaluation is convenient and quick. In addition, users can also use Import VCD file under Simulation to import the simulation file VCD file of modelsim for quick configuration. After the file is imported, all configuration parameters in the software evaluate the power consumption according to the frequency and conditions of the simulation signal.

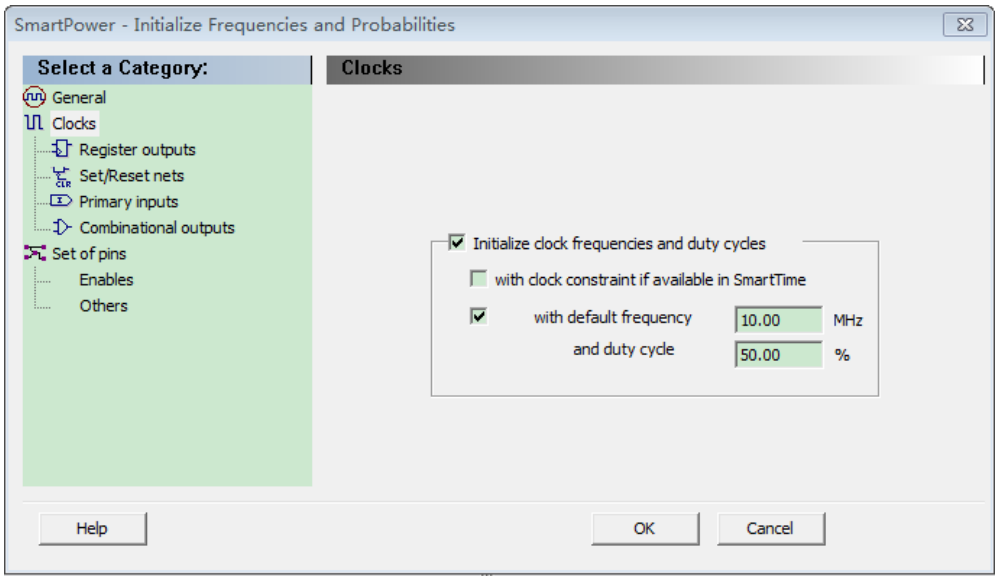


Figure E-5. Initialization configuration clock

Below the toolbar in the power consumption assessment software interface are the detailed results of the power consumption assessment, which are divided into five sub-interfaces: Summary, Domains, Analysis, Frequencies, and Probabilites. The Summary interface displays the total power consumption, static power consumption, dynamic power consumption, power consumption decomposition diagram, and assessment conditions.

The figure below is the Domains interface, which shows the frequency and probability of the clock domain signal and the data rate of the pin. These values are the default values after initialization configuration. Users can modify them according to their own needs. After modification, click Update and the software will re-evaluate the power consumption.

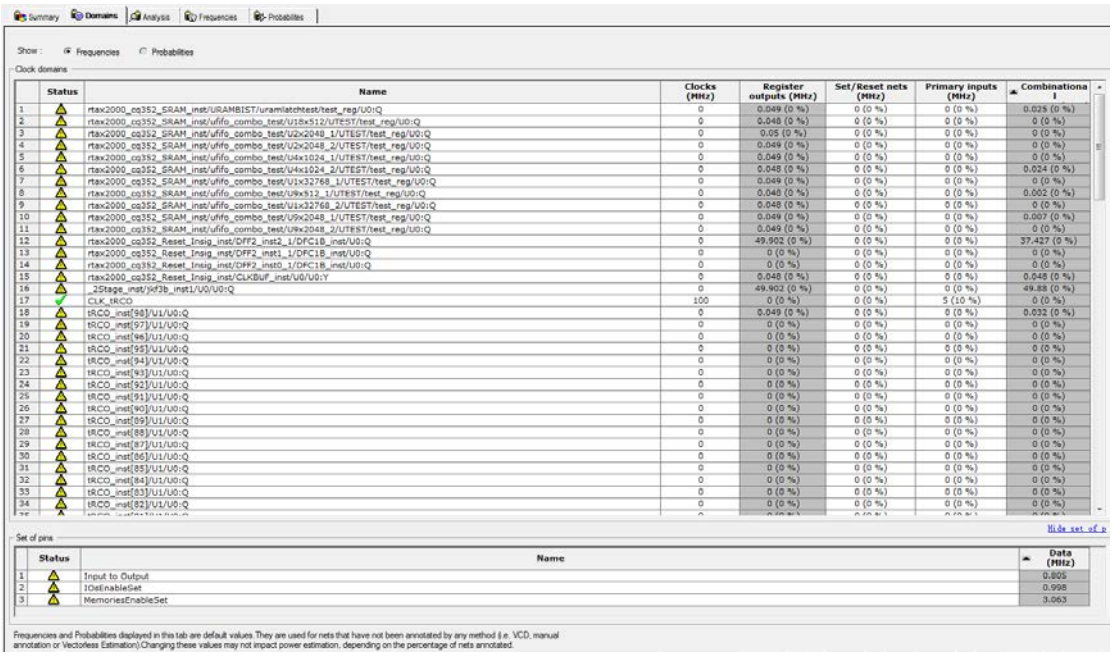


Figure E-6. Domains interface

The figure below is the Analysis interface, which shows the specific power consumption and proportion of each program module, making it easier for users to analyze the power consumption of each program module.

Figure E-7. Analysis interface

The figure below is the Frequencies interface, which shows the frequency information of each signal in the program. Users can filter the signal frequency information to be viewed by Domain and Source. All frequency information is the default value after initialization configuration. Users can select single or multiple signals to modify

according to their own needs. After modification, click Update, and the software will re-evaluate the power consumption based on the modified value.

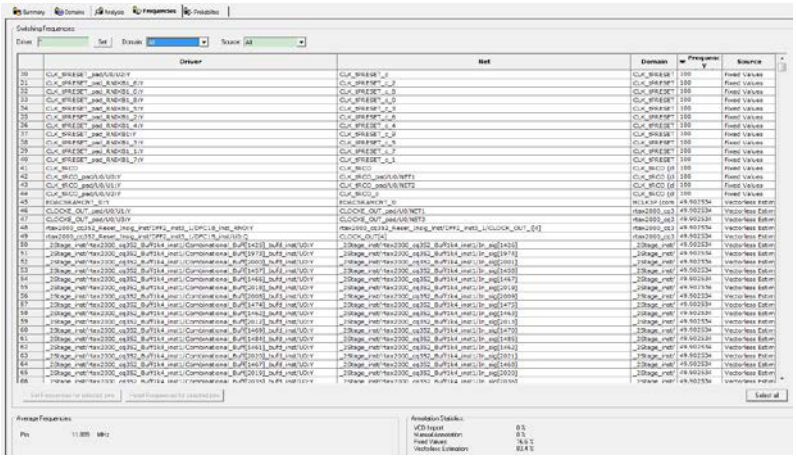


Figure E-8. Frequencies interface

The figure below is the Probabilites interface. Similar to the figure above, it shows the probability information of each signal in the program. Users can filter the signal probability information to be viewed by Type, Polarity, and Source. All probability information is the default value after initialization configuration. Users can select single or multiple signals to modify according to their own needs. After modification, click Update, and the software will re-evaluate the power consumption according to the modified value.

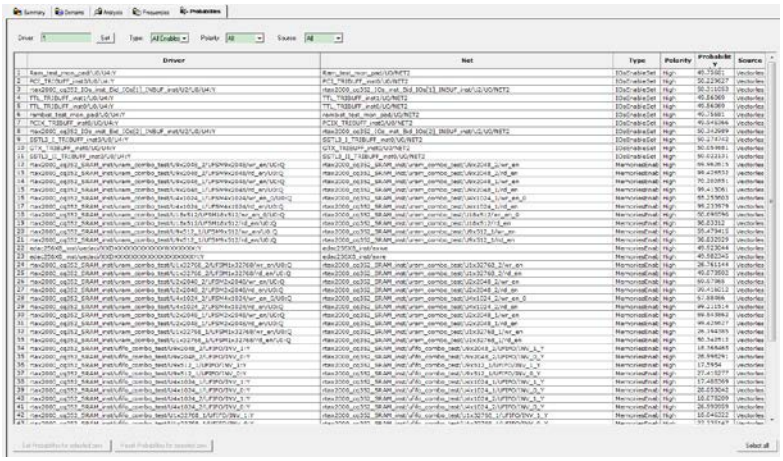


Figure E-9. Probabilites interface

Appendix F Compatibility Design of BSTRTAX1000-CQ352 and BSTRTAX1000-CQ35252

The BSTRTAX1000-CQ352 device and the BSTRTAX1000-CQ35252 device have the same package dimensions except for the height of the ceramic body, the same number of ports, and the same operating voltage conditions. The only difference is the scale of resources. Users can design compatibility when making PCB boards.

F.1. Differences in ports

Comparing the ports of BSTRTAX1000-CQ352 and BSTRTAX1000-CQ35252, there are mainly 7 different ports, as shown in the following table.

Table F-1. Differences in ports between BSTRTAX1000-CQ352 and BSTRTAX1000-CQ35252

Port number	BSTRTAX1000-CQ352	BSTRTAX1000-CQ35252	Recommended connection method
91	NC	VCCDA	VCCDA
130	NC	VCCDA	VCCDA
131	NC	VCCDA	VCCDA
174	NC	VCCDA	VCCDA
268	NC	VCCDA	VCCDA
307	NC	VCCDA	VCCDA
308	NC	VCCDA	VCCDA

As shown in the table above, there are 7 ports that are different between BSTRTAX1000-CQ352 and BSTRTAX1000-CQ35252, but they have the same serial

number and position. These 7 ports are VCCDA ports in BSTRTAX1000-CQ35252 and NC ports in BSTRTAX1000-CQ352.

When designing for compatibility, it is recommended to connect the above pins to VCCDA on the PCB board.

F.2 Differential Ports

There are two ports on BSTRTAX1000-CQ352 and BSTRTAX1000-CQ35252 that cannot be used as differential ports. The port numbers are 86 and 343. The port numbers are the same on BSTRTAX1000-CQ352 and BSTRTAX1000-CQ35252.

When in use, these two ports cannot be used as differential ports.

The other I/O ports can be used as single-ended or differential ports as required, see the pin list in Appendix A.

F.3. Replacement process and precautions for BSTRTAX1000-CQ352 and BSTRTAX1000-CQ35252

In addition to the full compatibility of the external dimensions and the difference in the connection methods of the 7 ports, the replacement of BSTRTAX1000-CQ352 and BSTRTAX1000-CQ35252 mainly lies in the programming projects and programming files.

Since they are two different devices, the programming files and AFM files of BSTRTAX1000-CQ352 and BSTRTAX1000-CQ35252 cannot be directly interchanged. For example, BSTRTAX1000-CQ35252 cannot be directly programmed with the AFM of BSTRTAX1000-CQ352. Conversely, BSTRTAX1000-CQ352 cannot be directly programmed with the AFM of BSTRTAX1000-CQ35252.

All of them need to be re-synthesized, laid out and routed, and the I/O ports allocated according to the development process in Appendix B.

When replacing BSTRTAX1000-CQ352 with BSTRTAX1000-CQ35252, the synthesis, simulation, and layout and routing are the same as before, mainly the allocation of I/O ports.

For single-ended and differential level standards, BSTRTAX1000-CQ352 and BSTRTAX1000-CQ35252 are fully compatible. However, for level standards with reference level, HSTL CLASS I, SSTL2 and SSTL3, there are restrictions on the allocation of reference level pin VREF and input and output pins with reference level inside the device. In conventional allocation, it is generally automatically allocated by Libero software, or manually adjusted and tried, and finally the allocation of ports with reference level is completed.

In BSTRTAX1000-CQ352 and BSTRTAX1000-CQ35252, the differences in internal scale, number and distribution of I/O PADs, etc., lead to different internal allocation restrictions on reference level pin VREF and input and output pins with reference level. As a result, when using ports with reference level standards, these ports with reference level are incompatible.

I/O allocation is shown in the figure below. There are two ways:

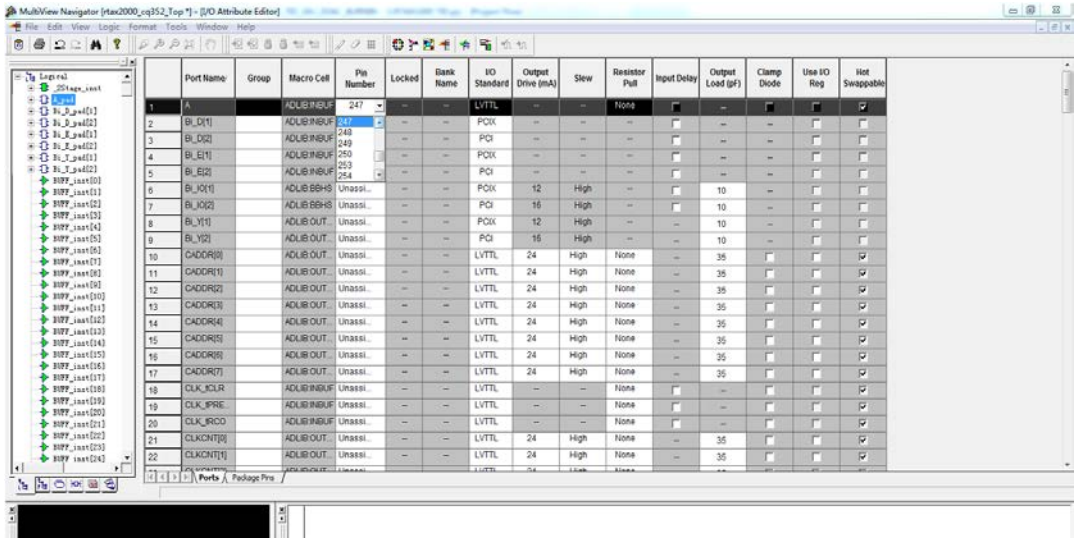


Figure F-1. Assign FPGA PIN Numbers based on the signal ports of the functions

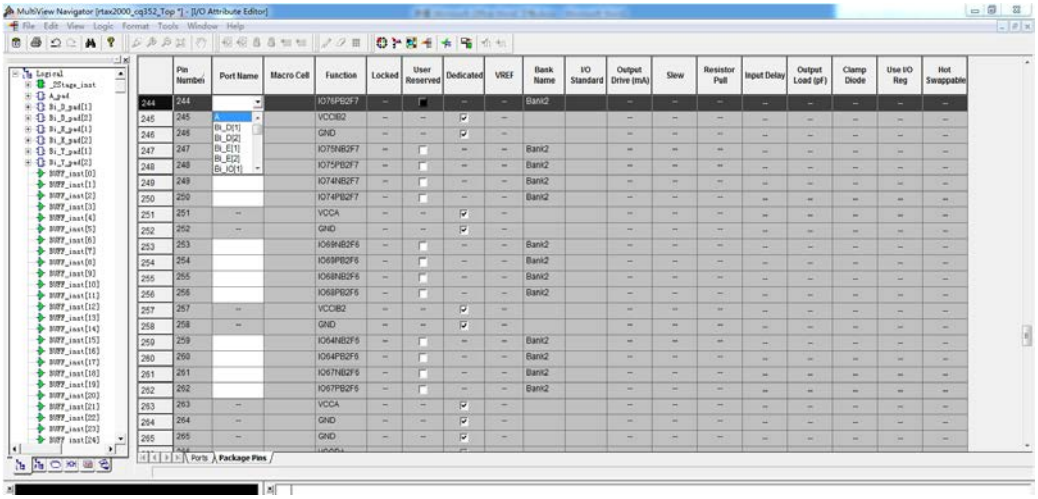


Figure F-2. Assigning function signal ports according to FPGA PIN Number

Through the above two methods, the FPGA I/O port is configured for the functional signal port.

When replacing from BSTRTAX1000-CQ352 to BSTRTAX1000-CQ35252 (or vice versa), you need to first obtain the port allocation information table of BSTRTAX1000-CQ352. Then, when allocating I/O after the BSTRTAX1000-CQ35252 is integrated, allocate according to the port allocation information table of BSTRTAX1000-CQ352. This ensures that the I/O ports are fully compatible after replacing with BSTRTAX1000-CQ35252.

For ports with reference levels that are not fully compatible, it is necessary to consider the compatibility of BSTRTAX1000-CQ35252 port allocation when initially designing BSTRTAX1000-CQ352 port allocation. Currently, there is no effective and efficient way to solve this problem, and it can only be solved through repeated attempts.

When the same I/O port configuration can be deployed in both BSTRTAX1000-CQ352 and BSTRTAX1000-CQ35252, full compatibility can be achieved.

If the port configuration in BSTRTAX1000-CQ352 cannot be routed in BSTRTAX1000-CQ35252, you need to adjust the configuration of the port with

reference level in BSTRTAX1000-CQ352 and then verify it in BSTRTAX1000-CQ35252 until it can be routed in both BSTRTAX1000-CQ352 and BSTRTAX1000-CQ35252.

F.4. Timing differences after replacement between BSTRTAX1000-CQ352 and BSTRTAX1000-CQ35252

The electrical characteristics of the internal components of BSTRTAX1000-CQ352 and BSTRTAX1000-CQ35252 are exactly the same. The main difference is the size and area, which leads to the difference in overall timing characteristics.

The main differences in the electrical characteristics of the overall circuits of BSTRTAX1000-CQ352 and BSTRTAX1000-CQ35252 before programming are: the minimum high pulse width and the minimum low pulse width of the clock.

However, after the functions are integrated, laid out and routed, there will be some differences in timing due to the layout, routing and scale differences. The maximum operating speed of the programmed functions will be different between BSTRTAX1000-CQ352 and BSTRTAX1000-CQ35252.

The extent of the difference is related to the specific functions and I/O configurations, and a definite assessment cannot be made at present.

Appendix G Comparison report with Actel AX1000

Description

- The main content of this report is the parameter comparison between the domestic BSTRTAX1000-CQ352 and the foreign RTAX1000-CQ352, so that users can replace the foreign RTAX1000-CQ352 and AX1000-CQ352 with domestic products.

- BSTRTAX1000 devices imitate foreign RTAX1000. They can replace foreign RTAX1000, AX1000, and also replace foreign AX500 series.
- The 1 million gate anti-fuse FPGAs currently used by users are all imported A series devices: AX1000, and the A series does not have radiation resistance. The foreign RT series device RTAX1000 is a device that has been reinforced and improved on the basis of the A series. It has radiation resistance and is compatible with the A series devices, but the chip area is increased by about 30%-50%, the speed is equivalent, and the power consumption is increased by 2-3 times (the main reason is that the R unit uses triple-mode redundancy). However, due to the embargo, the RT series cannot be purchased.
- The parameters and test conditions of the circuit refer to Actel's RTAX1000S and AX1000 US military standards and manuals.
- The "-1" in the name of foreign devices represents the speed grade (as shown in Figure 1), which means 15% faster than the standard grade. In this report, only the standard speed grade is compared.

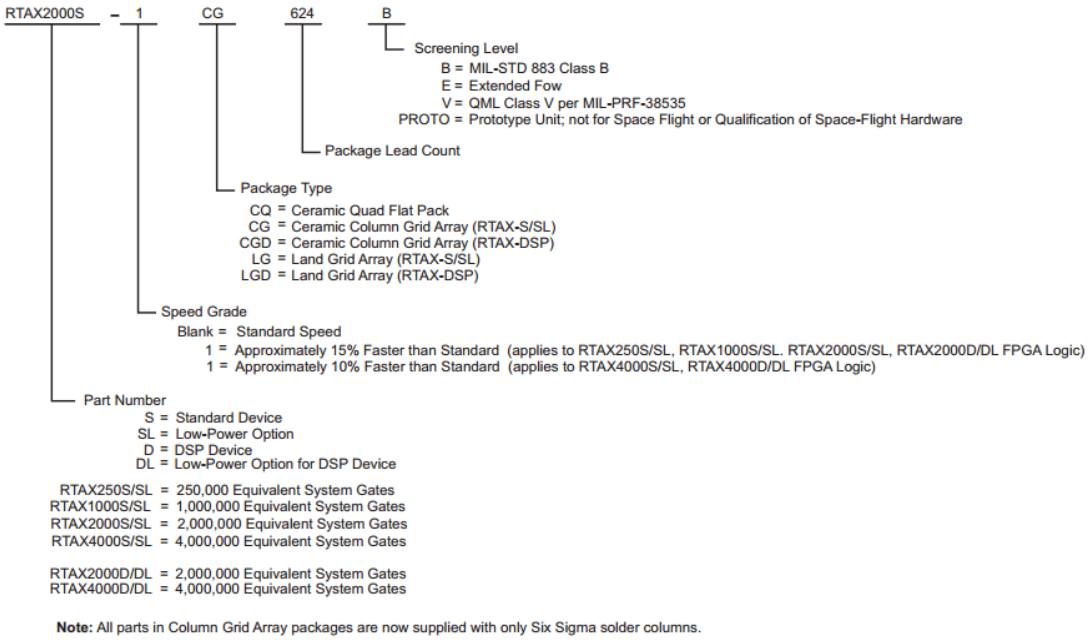


Figure G-1. Meaning of the names of imported RTAX1000 devices

Overview

BSTRTAX1000 is a radiation-hardened MTM (Metal-To-Metal) anti-fuse FPGA with a system gate count of 1,000,000 gates and a typical gate count of 125,000 gates. There are two types of logic cells inside the device: register cells (R-cell, triple-mode redundancy) and combinational logic cells (C-cell). Users interconnect and configure the logic cells by programming anti-fuses to achieve specific logic functions. There are 198 user-configurable I/O ports distributed around the CQ352 packaged device. All I/O ports can be configured as input, output, high-impedance, and bidirectional modes. At the same time, the device contains rich clock resources, a large amount of test logic, and specific encryption logic. Users can test the circuit through JTAG test logic, and can also encrypt the circuit by burning encryption anti-fuses.

Key Features:

- Port operating voltage VCCI = 3.3V ± 0.3V or 2.5V ± 0.25V or 1.8V ± 0.18V or 1.5V ± 0.075V
- Core operating voltage VCCA = 1.5V ± 0.075V
- System gate count 1,000,000 gates, typical gate count 125,000 gates
- Maximum operating frequency 320MHz
- C units: 12,096; R units: 6,048
- On-chip RAM: 162Kbit
- 8 global clocks
- Maximum quiescent current: 450mA
- 8 global clocks
- CQ352 package user configurable I/O ports 198

- Support 3.3V PCI/TTL, HSTL, SSTL and other level standards
- Adjustable output slew rate (except PCI level)
- Output port status can be configured at power-on: weak pull-up, weak pull-down, high impedance
- Support hot swap and cold backup

- MTM anti-fuse is used for function configuration and logic interconnection, without chip configuration, effectively preventing reverse engineering and design theft, ensuring data security
- Adopt radiation-resistant 0.13μm MTM anti-fuse 1P7M CMOS process
- Anti-radiation properties:
  - Total dose ≥150krad(Si)
  - Single event latch-up threshold (SEL): ≥75MeV•cm2/mg
  - Single event upset rate:
- Block RAM (EDAC on and timer 2MHz refresh) ≤10-10 errors/bit·day,
- Trigger logic unit ≤ 10-10 errors/bit·day
  - Single event upset threshold (SEU): ≥ 13MeV•cm2/mg (Block RAM with EDAC turned on and timer 2MHz refresh)
- ESD≥2000V
- Working temperature: -55℃~125℃
- Package: CQFP352

Parameter comparison

Comparison of main performance indicators of products

Table G-1. Comparison of main technical indicators with foreign countries

Serial number	index	Foreign RTAX1000S	Foreign AX1000	BSTRTAX1000	Comparison conclusion
1	Port voltage	VCCI=3.3V±0.3V or 2.5V±0.125V or 1.8V±0.09V or 1.5V±0.075V	VCCI=3.3V±0.3V or 2.5V±0.125V or 1.8V±0.09V or 1.5V±0.075V	VCCI=3.3V±0.3V or 2.5V±0.125V or 1.8V±0.09V or 1.5V±0.075V	Consistency
2	Differential port voltage	VCCDA=3.3V±0.3V or 2.5V±0.125V	VCCDA=3.3V±0.3V or 2.5V±0.125V	VCCDA=3.3V±0.3V or 2.5V±0.125V	Consistency
3	Core voltage	1.5V±0.075V	1.5V±0.075V	1.5V±0.075V	Consistency
4	System Gate Count	1,000,000 doors	1,000,000 doors	1,000,000 doors	Consistency
5	Typical gate count	125,000 doors	125,000 doors	125,000 doors	Consistency
6	Logical Unit	C units: 12096; R units: 6048	C units: 12096; R units: 6048	C units: 12096; R units: 6048	Consistency
7	On-chip RAM	162Kbit	162Kbit	162Kbit	Consistency
8	Global clock	8	8	8	Consistency
9	Maximum operating frequency	350MHz	350MHz	320MHz	Inconsistency
10	CQ352 package user I/O number	198	198	198	Consistency
11	I/O Port Characteristics	Output slew rate is adjustable; port status is configurable at power-on; supports hot swap and cold backup	Output slew rate is adjustable; port status is configurable at power-on; supports hot swap and cold backup	Output slew rate is adjustable; port status is configurable at power-on; supports hot swap and cold backup	Consistency
12	Total dose	≥100k rad(Si)	-	≥150k rad(Si)	Inconsistency
13	Single Event Latchup	immunity	-	≥90MeV·cm2/mg	

14	Single Event Upset	≥37MeV·cm2/mg	-	Flip rate: ≤1E-10 Error/bit.day	
15	ESD Specifications	≥2000V	≥2000V	≥2000V	Consistency
16	Programming pass rate	30(6)	30(6)	30(6)	Consistency
17	Operating temperature	-55℃~+125℃	-55℃~+125℃	-55℃~+125℃	Consistency

Comparison conclusion:

- Comparison between domestic devices and imported AX1000: domestic devices are resistant to radiation, while foreign devices are not.
- Comparison between domestic devices and imported RTAX1000: There are differences in radiation resistance indicators.

Comparison of Absolute Maximum Ratings and Recommended Operating Conditions

Table G-2. Absolute maximum ratings compared with foreign countries

	project	Foreign RTAX1000S	Foreign AX1000	BSTRTAX1000	Comparison conclusion
1	Junction temperature TJ	-55℃~+135℃	--	-55℃~+135℃	Consistency
2	Core voltage VCCA	-0.3V~+1.7V	-0.3V~+1.6V	-0.3V~+1.7V	NoConsistency
3	I/O voltage VCCI	-0.3V~+3.75V	-0.3V~+3.75V	-0.3V~+3.75V	Consistency
4	V_{PUMP}Voltage	-0.3V~+3.75V	--	-0.3V~+3.75V	Consistency
5	V_{REF}Voltage	-0.3V~+3.75V	-0.3V~+3.75V	-0.3V~+3.75V	Consistency
6	Input voltage VI	-0.5V~+4.1V	-0.5V~+4.1V	-0.5V~+4.1V	Consistency
7	Output voltage VO	-0.5V~+3.75V	-0.5V~+3.75V	-0.5V~+3.75V	Consistency

8	Storage temperature TSG	-60℃~+150℃	-60℃~+150℃	-60℃~+150℃	Consistency
9	Differential I/O voltage VCCDA	-0.3V~+3.75V	-0.3V~+3.75V	-0.3V~+3.75V	Consistency

Table G-3 Comparison of recommended working conditions with foreign countries

	project	Foreign RTAX1000S	Foreign AX1000	BSTRTAX1000	Comparison conclusion
1	Junction temperature TJ	-55℃~+125℃	-55℃~+125℃	-55℃~+125℃	Consistency
2	1.5V VCCA	1.425V~1.575V	1.425V~1.575V	1.425V~1.575V	Consistency
3	1.5V VCCI	1.425V~1.575V	1.425V~1.575V	1.425V~1.575V	Consistency
4	1.8V VCCI	1.71V~1.89V	1.71V~1.89V	1.71V~1.89V	Consistency
5	2.5V VCCI	2.375V~2.625V	2.375V~2.625V	2.375V~2.625V	Consistency
6	3.3V VCCI	3.0V~3.6V	3.0V~3.6V	3.0V~3.6V	Consistency
7	2.5V VCCDA	2.375V~2.625V	none	2.375V~2.625V	Consistency
8	3.3V VCCDA	3.0V~3.6V	3.0V~3.6V	3.0V~3.6V	Consistency
9	3.3V VPUMP	3.0V~3.6V	3.0V~3.6V	3.0V~3.6V	Consistency

Comparison conclusion:

- Comparison between domestic devices and imported AX1000: Four parameters are not specified, and the rest are the same.
- Comparison between domestic devices and imported RTAX1000: the working conditions are the same.

Comparison of packaging related parameters

Table G-4. Comparison of relevant parameters of CQFP352 package (with lead frame)

Parameter	Foreign RTAX1000S	Foreign AX1000	BSTRTAX1000	Comparison conclusion
Package	CQ352	CQ352	CQ352	Consistency
Package size (typical value, mm)	75×75×2.66	75×75×2.66	75×75×2.75	Inconsistency
Pin width (typical value, mm)	0.19	0.19	0.19	Consistency
Pin spacing (typical value, mm)	0.5	0.5	0.5	Consistency
Logo	First foot mark	First foot mark	First foot mark	Consistency
Thermal resistance θJC	0.4℃/W	2.0℃/W	0.53℃/W	Inconsistency

Comparison conclusion:

CQ352 package: Comparison between domestic devices and imported AX1000: The domestic package size is slightly thicker than that of foreign devices, the other dimensions are consistent with those of foreign devices, and the thermal resistance is inconsistent with that of foreign devices; Comparison between domestic devices and imported RTAX1000: The package dimensions are basically the same, and the thermal resistance is inconsistent with that of foreign devices.

3.4 Port Definition Comparison

The port differences are shown in the following table:

Table G-5. Port differences between CQ352 packaging and foreign AX1000 products

PIN Number	AX1000-CQ352	BSTRTAX1000-CQ352	the difference
317	VCCPLA	NC	These are analog power supplies for 8 PLLs in AX1000. When PLL is not used in AX1000, the corresponding port is connected to VCCA.
315	VCCPLB	NC	
303	VCCPLC	NC	
301	VCCPLD	NC	
140	VCCPLE	NC	
138	VCCPLF	NC	
126	VCCPLG	NC	
124	VCCPL	NC	
318	VCOMPLA	NC	These are the compensation reference signals for the eight PLLs in AX1000. When the PLL in AX1000 is not in use, the corresponding port is left floating.
316	VCOMPLB	NC	
304	VCOMPLC	NC	
302	VCOMPLD	NC	
141	VCOMPLE	NC	
139	VCOMPLF	NC	
127	VCOMPLG	NC	
125	VCOMPLH	NC	

When replacing AX1000-CQ352 with BSTRTAX1000-CQ352, the 16 NC ports related to PLL can be left floating and connected to GND or VCCA, so it can be directly replaced without changing the connection. Except for these 16 ports, the other ports are in the same position as the foreign AX1000-CQ352 products, and the bank number is also the same.

3.5 Comparison of product specification indicators

Table G-6. Comparison of specifications and foreign product indicators

characteristic	symbol	condition Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx -55℃≤TA≤125℃	Foreign RTAX1000S		Foreign AX1000		BSTRTAX1000		unit	contrast
							Minimum	maximum		
Core power supply quiescent current	I_{CCA}	f=0, VCCA=1.575V, VCCIBx=3.6V, VCCDA=3.6V, TA=25℃	—	30	—	7.5	—	30	mA	Inconsistency
		f=0, VCCA=1.575V, VCCIBx=3.6V, VCCDA=3.6V, TA=-55℃,125℃	—	450	—	200	—	450	mA	Inconsistency
Port power quiescent current	I_{CCI}	f=0, VCCA=1.575V, VCCIBX=3.6V, VCCDA=3.6V, TA=25℃	—	10	—	10	—	10	mA	Consistency

		f=0, VCCA=1.575V, VCCIBX=3.6V, VCCDA=3.6V, TA=-55℃,125℃	—	35	—	32	—	35	mA	Inconsistency
Differential Supply Quiescent Current	ICCDA	f=0, VCCA=1.575V, VCCIBx=3.6V, VCCDA=3.6V, TA=25℃	—	7	—	1.5	—	7	mA	Inconsistency
		f=0, VCCA=1.575V, VCCIBx=3.6V, VCCDA=3.6V, TA=-55℃,125℃	—	10	—	10	—	10	mA	Consistency
Core power supply dynamic current	I_{OPA}	f=10MHz, VCCA=1.575V, VCCIBx=3.6V, VCCDA=3.6V	—	—	—	—	—	350	mA	No overseas
Port power dynamic current	I_{OPI}	f=10MHz, VCCA=1.575V, VCCIBx=3.6V, VCCDA=3.6V	—	—	—	—	—	350	mA	No overseas
Differential Supply Dynamic Current	IOPDA	f=10MHz, VCCA=1.575V, VCCIBx=3.6V, VCCDA=3.6V	—	—	—	—	—	50	mA	No overseas

Input low level leakage current	I_{IL}	VIN=GND,TA=25℃	—	1	—	10	—	1	μA	Inconsistency
		VIN=GND,TA=-55℃,125℃	—	5	—	10	—	5	μA	Inconsistency
Input high level leakage current	I_{IH}	VIN = V_{CCIB},TA=25℃	—	1	—	10	—	1	μA	Inconsistency
		VIN = V_{CCIB},TA=-55℃,125℃	—	5	—	10	—	5	μA	Inconsistency
Three-state output leakage current	IOZ	VIN = V_{CCIB},TA=25℃	—	1	—	10	—	1	μA	Inconsistency
		VIN = V_{CCIB},TA=-55℃,125℃	—	5	—	10	—	5	μA	Inconsistency
Differential Pair	ICCDIFFA	VIN = V_{CCIB},TA=25℃	—	3.13	—	—	—	3.13	mA	Inconsistency

Amplifier Current		VIN = V_{CCIB},TA=-55℃,125℃	—	3.7	—	—	—	3.7	mA	Inconsistency
Port internal pull-up current	IPULLUP	V_{CCIB}=3.3V	—	—	—	—	-90	-50	μA	No overseas
		V_{CCIB}=2.5V	—	—	—	—	-55	-25	μA	No overseas
		V_{CCIB}=1.8V	—	—	—	—	-30	-8	μA	No overseas
		V_{CCIB}=1.5V	—	—	—	—	-20	-3	μA	No overseas
Port internal pull-down current	IPULLDown	V_{CCIB}=3.3V	—	—	—	—	30	80	μA	No overseas
		V_{CCIB}=2.5V	—	—	—	—	15	45	μA	No overseas

		V_{CCIB}=1.8V	—	—	—	—	3	20	μA	No overseas
		V_{CCIB}=1.5V	—	—	—	—	1	12	μA	No overseas
Port capacitance	CIO	f = 100 kHz, VIN = 0 V	—	15	—	15	—	15	pF	Consistency
Binning Circuit Delay	BIN_fast	V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V	—	6.6	—	6.6	—	7	μs	Bigger than abroad
	BIN_slow	V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V	—	8.5	—	8.5	—	9.5	μs	Bigger than abroad
Maximum operating frequency	Fmax		350	—	350	—	320	—	MHz	Consistency
		3.3V LVTTL level (VCCIBx=3.3±0.3V)								

Input low level	V_{IL}		-0.3	0.8	-0.3	0.8	-0.3	0.8	V	Consistency
Input high level	V_{IH}		2.0	3.6	2.0	3.6	2.0	3.6	V	Consistency
Output low level	V_{OL}	I_{OL}= 24mA	—	0.4	—	0.4	—	0.4	V	Consistency
Output high level	V_{OH}	I_{OH}= 24mA	2.4	—	2.4	—	2.4	—	V	Consistency
Port transmission delay	tDP+PY_H	High Slew, V_{CCA}=1.425V, VCCIBX=3V	—	6.29	—	6.27	—	8.0	ns	Consistency
	tDP+PY_L	Low Slew, V_{CCA}=1.425V, VCCIBX=3V	—	15.58	—	16.25	—	17.5	ns	Bigger than abroad
		2.5V LVCMOS (VCCIBx=2.5±0.125V)								

Input low level	V_{IL}		-0.3	0.7	-0.3	0.7	-0.3	0.7	V	Consistency
Input high level	V_{IH}		1.7	3.6	1.7	3.6	1.7	3.6	V	Consistency
Output low level	V_{OL}	I_{OL}= 12mA	—	0.4	—	0.4	—	0.4	V	Consistency
Output high level	V_{OH}	I_{OH}= -12mA	2.0	—	2.0	—	2.0	—	V	Consistency
Port transmission delay	tDP+PY_H	High Slew, V_{CCA}=1.425V, VCCIBX=2.375V	—	7.2	—	—	—	9.5	ns	Inconsistency
	tDP+PY_L	Low Slew, V_{CCA}=1.425V, VCCIBX=2.375V	—	23.77	—	—	—	24.7	ns	Inconsistency
		1.8V LVCMOS (VCCIBx=1.8±0.09V)								

Input low level	V_{IL}		-0.3	0.2 VCCIBx	-0.3	0.2 VCCIBx	-0.3	0.2 VCCIBx	V	Consistency
Input high level	V_{IH}		0.7 VCCIBx	2.1	0.7 VCCIBx	2.1	0.7 VCCIBx	2.1	V	Consistency
Output low level	V_{OL}	I_{OL}= 6mA	—	0.2	—	0.2	—	0.2	V	Consistency
Output high level	V_{OH}	I_{OH}= -6mA	VCCIBx - 0.2	—	VCCIBx - 0.2	—	VCCIBx - 0.2	—	V	Consistency
Port transmission delay	tDP+PY_H	HighSlew V_{CCA}=1.425V, VCCIBX=1.71V	—	10.71	—	—	—	10.6	ns	Inconsistency
	tDP+PY_L	LowSlew V_{CCA}=1.425V, VCCIBX=1.71V	—	40.7	—	—	—	32.6	ns	Inconsistency
		1.5V LVCMOS (VCCIBx=1.5±0.075V)								

Input low level	V_{IL}		-0.5	0.35 VCCIBx	-0.5	0.35 VCCIBx	-0.5	0.35 VCCIBx	V	Consistency
Input high level	V_{IH}		0.65 VCCIBx	1.95	0.65 VCCIBx	1.95	0.65 VCCIBx	1.95	V	Consistency
Output low level	V_{OL}	I_{OL}=8mA	—	0.4	—	0.4	—	0.4	V	Consistency
Output high level	V_{OH}	I_{OH}= -8mA	VCCIBx - 0.4	—	VCCIBx - 0.4	—	VCCIBx - 0.4	—	V	Consistency
Port transmission delay	tDP+PY_H	HighSlew V_{CCA}=1.425V, VCCIBX=1.425V	—	12.38	—	—	—	17.0	ns	Inconsistency
	tDP+PY_L	LowSlew V_{CCA}=1.425V, VCCIBX=1.425V	—	60.11	—	—	—	48.2	ns	Inconsistency
		3.3V PCI (VCCIBx=3.3±0.3V)								

Input low level	V_{IL}		-0.5	0.3 VCCIBx	-0.5	0.3 VCCIBx	-0.5	0.3 VCCIBx	V	Consistency
Input high level	V_{IH}		0.55 VCCIBx	VCCIBx +0.5	0.55 VCCIBx	VCCIBx +0.5	0.55 VCCIBx	VCCIBx +0.5	V	Consistency
Output low level	V_{OL}	I_{OL}=1.5mA	—	0.1VCC	—	0.1VCC	—	0.1VCC	V	Consistency
Output high level	V_{OH}	I_{OH}= -0.5mA	0.9VCC	—	0.9VCC	—	0.9VCC	—	V	Consistency
Port transmission delay	tDP+PY	V_{CCA}=1.425V, VCCIBX=3V	—	4.66	—	4.66	—	9.5	ns	Bigger than abroad
		3.3V GTL+ (VCCIBx=3.3±0.3V, VREF=1±0.1V)								
Input low level	V_{IL}			VREF-0.1		VREF-0.1		VREF-0.1	V	Consistency

Input high level	V_{IH}		VREF+0.1		VREF+0.1		VREF+0.1		V	Consistency
Output low level	V_{OL}	I_{OL}=4mA		0.6		0.6		0.6	V	Consistency
Port transmission delay	tDP+PY	V_{CCA}=1.425V, VCCIBX=3V, VREF=0.9V	—	3.85	—	3.81	—	8.0	ns	Consistency
		1.5V HSTL Class I (VCCIBx=1.5±0.075V, VREF=0.75±0.04V)								
Input low level	V_{IL}		-0.3	VREF-0.1	-0.3	VREF-0.1	-0.3	VREF-0.1	V	Consistency
Input high level	V_{IH}		VREF+0.1	3.6	VREF+0.1	3.6	VREF+0.1	3.6	V	Consistency
Output low level	V_{OL}	I_{OL}=8mA	—	0.4	—	0.4	—	0.4	V	Consistency

Output high level	V_{OH}	I_{OH}= -8mA	VCCIBx - 0.4	—	VCCIBx - 0.4	—	VCCIBx - 0.4	—	V	Consistency
Port transmission delay	tDP+PY	V_{CCA}=1.425V, VCCIBX=1.425V, VREF=0.71V	—	8.78	—	8.97	—	8.5	ns	Consistency
		2.5V SSTL2 Class I (VCCIBx=2.5±0.125V, VREF=1.25±0.06V)								
Input low level	V_{IL}		-0.3	VREF-0.2	-0.3	VREF-0.2	-0.3	VREF-0.2	V	Consistency
Input high level	V_{IH}		VREF+0.2	3.6	VREF+0.2	3.6	VREF+0.2	3.6	V	Consistency
Output low level	V_{OL}	I_{OL}=7.6mA	—	VREF-0.57	—	VREF-0.57	—	VREF-0.57	V	Consistency
Output high level	V_{OH}	I_{OH}= -7.6mA	VREF+0.57	—	VREF+0.57	—	VREF+0.57	—	V	Consistency

Port transmission delay	tDP+PY	V_{CCA}=1.425V, VCCIBX=2.375V, VREF=1.19V	—	5.59	—	5.65	—	8.0	ns	Consistency
		2.5V SSTL2 Class II (VCCIBx=2.5±0.125V, VREF=1.25±0.06V)								
Input low level	V_{IL}		-0.3	VREF-0.2	-0.3	VREF-0.2	-0.3	VREF-0.2	V	Consistency
Input high level	V_{IH}		VREF+0.2	3.6	VREF+0.2	3.6	VREF+0.2	3.6	V	Consistency
Output low level	V_{OL}	I_{OL}=15.2mA	—	VREF-0.8	—	VREF-0.8	—	VREF-0.8	V	Consistency
Output high level	V_{OH}	I_{OH}= -15.2mA	VREF+0.8	—	VREF+0.8	—	VREF+0.8	—	V	Consistency
Port transmission delay	tDP+PY	V_{CCA}=1.425V, VCCIBX=2.375V, VREF=1.19V	—	5.68	—	5.73	—	8.0	ns	Consistency

		3.3V SSTL3 Class I (VCCCIBx=3.3±0.3V, VREF=1.5±0.15V)								
Input low level	V_{IL}		-0.3	VREF-0.2	-0.3	VREF-0.2	-0.3	VREF-0.2	V	Consistency
Input high level	V_{IH}		VREF+0.2	3.6	VREF+0.2	3.6	VREF+0.2	3.6	V	Consistency
Output low level	V_{OL}	I_{OL}=8mA	—	VREF-0.6	—	VREF-0.6	—	VREF-0.6	V	Consistency
Output high level	V_{OH}	I_{OH}= -8mA	VREF+0.6	—	VREF+0.6	—	VREF+0.6	—	V	Consistency
Port transmission delay	tDP+PY	V_{CCA}=1.425V, VCCIBX=3V, VREF=1.35V	—	5.45	—	5.30	—	7.5	ns	Consistency
		3.3V SSTL3 Class II (VCCIBx=3.3±0.3V, VREF=1.5±0.15V)								

Input low level	V_{IL}		-0.3	VREF-0.2	-0.3	VREF-0.2	-0.3	VREF-0.2	V	Consistency
Input high level	V_{IH}		VREF+0.2	3.6	VREF+0.2	3.6	VREF+0.2	3.6	V	Consistency
Output low level	V_{OL}	I_{OL}=16mA	—	VREF-0.8	—	VREF-0.8	—	VREF-0.8	V	Consistency
Output high level	V_{OH}	I_{OH}= -16mA	VREF+0.8	—	VREF+0.8	—	VREF+0.8	—	V	Consistency
Port transmission delay	tDP+PY	V_{CCA}=1.425V, VCCIBX=3V, VREF=1.35V	—	5.54	—	5.38	—	7.5	ns	Consistency
		2.5V LVDS (VCCIBx=2.5±0.125V, VCCDA=3.3±0.3V)								
Output low level	V_{OL}			1.25		1.25		1.25	V	Consistency

Output high level	V_{OH}		1.25		1.25		1.25		V	Consistency
Differential output voltage	VODIFF		250	450	250	450	250	450	mV	Consistency
Output common mode voltage	VOCM		1.125	1.375	1.125	1.375	1.125	1.375	V	Consistency
Input common mode voltage	VICM		0.2	2.2	0.2	2.2	0.2	2.2	V	Consistency
Port transmission delay	tDP+PY	V_{CCA}=1.425V, VCCIBX=2.375V, VCCDA=3V	—	5.34	—	5.52	—	8.5	ns	Consistency
		3.3V LVPECL (VCCIBx=3.3±0.3V)								
Input low level	V_{IL}		0.86	2.125	0.86	2.125	0.86	2.125	V	Consistency

Input high level	V_{IH}		1.49	2.72	1.49	2.72	1.49	2.72	V	Consistency
Output low level	V_{OL}		0.96	1.57	0.96	1.57	0.96	1.57	V	Consistency
Output high level	V_{OH}		1.8	2.41	1.8	2.41	1.8	2.41	V	Consistency
Port transmission delay	tDP+PY	V_{CCA}=1.425V, VCCIBX=3V	—	5.03	—	5.22	—	9.2	ns	Consistency

Comparison conclusion:

- The static current and port leakage current of ICCA, ICCDA, ICCI, etc., the parameters of BSTRTAX1000 are consistent with those of foreign RTAX1000, but are greater than those of foreign AX1000.
- The Binning circuit delay is larger than that of foreign RTAX1000 and AX1000, and there are differences in device characteristics.

- The port delay parameter is larger than that of foreign RTAX1000 and AX1000. On the one hand, there are differences in device characteristics. On the other hand, this is an internal parameter. When testing with BSTRTAX1000, it is necessary to program the corresponding function. The total delay includes input buffer delay + output buffer delay, anti-fuse unit delay, and port-to-port transmission delay.
- For other parameters, there is no corresponding parameter range marked in foreign products.

Table G-7. Comparison of BSTRTAX1000 measured values and foreign products

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
Core power supply quiescent current	I_{CCA}	f=0, VCCA=1.575V, VCCIBx=3.6V, VCCDA=3.6V, TA=25℃	—	30	—	30	—	4.3	—	mA
		f=0, VCCA=1.575V, VCCIBx=3.6V, VCCDA=3.6V, TA=-55℃,125℃	—	450	—	450	9.1	—	45.1	mA

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
Port power quiescent current	I_{CCI}	f=0, VCCA=1.575V, VCCIBX=3.6V, VCCDA=3.6V, TA=25℃	—	10	—	10	—	2.8	—	mA
		f=0, VCCA=1.575V, VCCIBX=3.6V, VCCDA=3.6V, TA=-55℃,125℃	—	35	—	35	8.9	—	15.6	mA
Differential Supply Quiescent Current	ICCDA	f=0, VCCA=1.575V, VCCIBx=3.6V, VCCDA=3.6V, TA=25℃	—	7	—	7	—	5.2	—	mA
		f=0, VCCA=1.575V, VCCIBx=3.6V, VCCDA=3.6V, TA=-55℃,125℃	—	10	—	10	6.1	—	7.7	mA
Core power supply dynamic current	I_{OPA}	f=10MHz, VCCA=1.575V, VCCIBx=3.6V, VCCDA=3.6V	—	—	—	350	261.2	247.5	246.1	mA
Port power dynamic current	I_{OPI}	f=10MHz, VCCA=1.575V, VCCIBx=3.6V, VCCDA=3.6V	—	—	—	350	279.3	275.2	268.1	mA

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
Differential Supply Dynamic Current	IOPDA	f=10MHz, VCCA=1.575V, VCCIBx=3.6V, VCCDA=3.6V	—	—	—	50	28.9	26.6	25.4	mA
Input low level leakage current	I_{IL}	VIN=GND,TA=25℃	—	1	—	1	—	-0.003	—	μA
		VIN=GND,TA=-55℃,125℃	—	5	—	5	-0.015	—	-0.022	μA
Input high level leakage current	I_{IH}	VIN=VCCI,TA=25℃	—	1	—	1	—	0.093	—	μA
		VIN=VCCI,TA=-55℃,125℃	—	5	—	5	0.027	—	0.035	μA
Three-state output leakage current	IOZ	VIN=VCCI,TA=25℃	—	1	—	1	—	0.037	—	μA
		VIN=VCCI,TA=-55℃,125℃	—	5	—	5	0.058	—	0.067	μA
Differential incremental quiescent current	ICCDIFFA	VIN=VCCI,TA=25℃	—	3.13	—	3.13	—	2.51	—	mA
		VIN=VCCI,TA=-55℃,125℃	—	3.7	—	3.7	2.84	—	3.12	mA
	IPULLUP	VCCI=3.3V	—	—	-90	-50	-76	-68	-59	μA

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
Port internal pull-up current		VCCI=2.5V	—	—	-55	-25	-46	-37	-30	μA
		VCCI=1.8V	—	—	-30	-8	-23	-15	-11	μA
		VCCI=1.5V	—	—	-20	-3	-14	-9	-5	μA
Port internal pull-down current	IPULLDown	VCCI=3.3V	—	—	30	80	71	62	52	μA
		VCCI=2.5V	—	—	15	45	40	31	22	μA
		VCCI=1.8V	—	—	3	20	17	11	7	μA
		VCCI=1.5V	—	—	1	12	9.2	6	3.6	μA
Port capacitance	CIO	f = 100 kHz, VIN = 0 V	—	15	—	15	—	14.1	—	pF
Binning Circuit Delay	BIN fast	V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V	—	6.6	—	6.6	5.5	6.4	7.1	μs
	BIN low	V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V	—	8.5	—	8.5	7.3	8.1	9.1	μs
Maximum operating frequency	Fmax		250	—	320	—	480	428	390	MHz
3.3V LVTTL (VCCIBx=3.3±0.3V)										
Input low level	V_{IL}	V_{CCA}=1.425V, VCCIBX=3.0V, VCCDA=3.0V	-0.3	0.8	-0.3	0.8	1.17	1.16	1.16	V

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
		V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V					1.27	1.27	1.26	
		V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V					1.38	1.37	1.37	
Input high level	V_{IH}	V_{CCA}=1.425V, VCCIBX=3.0V, VCCDA=3.0V	2	3.6	2	3.6	1.77	1.73	1.69	V
		V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V					1.88	1.82	1.78	
		V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V					1.95	1.91	1.89	
Output low level	V_{OL}	I_{OL}= 24mA, V_{CCA}=1.425V, VCCIBX=3.0V, VCCDA=3.0V	—	0.4	—	0.4	0.129	0.152	0.179	V
		I_{OL}= 24mA, V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V					0.123	0.141	0.167	
		I_{OL}= 24mA, V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V					0.119	0.139	0.164	

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
Output high level	V_{OH}	I_{OH}= -24mA, V_{CCA}=1.425V, VCCIBX=3.0V, VCCDA=3.0V	2.4	—	2.4	—	2.801	2.752	2.687	V
		I_{OH}=- 24mA, V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V					3.115	3.064	3.006	
		I_{OH}=- 24mA, V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V					3.427	3.377	3.314	
Port transmission delay	tDP+PY_H	HighSlew,V_{CCA}=1.425V, VCCIBX=3V	—	—	—	8.0	5.2	5.5	5.9	ns
	tDP+PY_L	LowSlew,V_{CCA}=1.425V, VCCIBX=3V	—	—	—	17.8	9.6	10.4	11.3	ns
2.5V LVCMOS (VCCIBx=2.5±0.125V)										
Input low level	V_{IL}	V_{CCA}=1.425V, VCCIBX=2.375V, VCCDA=2.375V	-0.3	0.7	-0.3	0.7	1.25	1.23	1.25	V
		V_{CCA}=1.500V, VCCIBX=2.500V, VCCDA=2.500V					1.30	1.32	1.29	

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
		V_{CCA}=1.575V, VCCIBX=2.625V, VCCDA=2.625V					1.36	1.38	1.35	
Input high level	V_{IH}	V_{CCA}=1.425V, VCCIBX=2.375V, VCCDA=2.375V	1.7	3.6	1.7	3.6	1.3	1.28	1.26	V
		V_{CCA}=1.500V, VCCIBX=2.500V, VCCDA=2.500V					1.36	1.36	1.33	
		V_{CCA}=1.575V, VCCIBX=2.625V, VCCDA=2.625V					1.46	1.41	1.4	
Output low level	V_{OL}	I_{OL}= 12mA, V_{CCA}=1.425V, VCCIBX=2.375V, VCCDA=2.375V	—	0.4	—	0.4	0.122	0.137	0.167	V
		I_{OL}= 12mA, V_{CCA}=1.500V, VCCIBX=2.500V, VCCDA=2.500V					0.117	0.135	0.163	

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
		I_{OL}= 12mA, V_{CCA}=1.575V, VCCIBX=2.625V, VCCDA=2.625V					0.112	0.127	0.157	
Output high level	V_{OH}	I_{OH}= -12mA, V_{CCA}=1.425V, VCCIBX=2.375V, VCCDA=2.375V	2	—	2	—	2.185	2.129	2.056	V
		I_{OH}=-12mA, V_{CCA}=1.500V, VCCIBX=2.500V, VCCDA=2.500V					2.313	2.265	2.193	
		I_{OH}=-12mA, V_{CCA}=1.575V, VCCIBX=2.625V, VCCDA=2.625V					2.444	2.393	2.324	
Port transmission delay	tDP+PY_H	HighSlew,V_{CCA}=1.425V, VCCIBX=2.375V	—	—	—	10.2	6.3	6.8	7.3	ns
	tDP+PY_L	LowSlew,V_{CCA}=1.425V, VCCIBX=2.375V	—	—	—	24.5	13.7	14.5	15.3	ns
1.8V LVCMOS (VCCIBx=1.8±0.09V)										

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
Input low level	V_{IL}	V_{CCA}=1.425V, VCCIBX=1.71V, VCCDA=1.71V	-0.3	0.2VCCI	-0.3	0.2VCCI	0.96	0.98	0.98	V
		V_{CCA}=1.500V, VCCIBX=1.80V, VCCDA=1.80V					1.01	1.01	1.03	
		V_{CCA}=1.575V, VCCIBX=1.89V, VCCDA=1.89V					1.06	1.07	1.08	
Input high level	V_{IH}	V_{CCA}=1.425V, VCCIBX=1.71V, VCCDA=1.71V	0.7VCCI	2.1	0.7VCCI	2.1	0.98	0.99	0.99	V
		V_{CCA}=1.500V, VCCIBX=1.80V, VCCDA=1.80V					1.03	1.03	1.04	
		V_{CCA}=1.575V, VCCIBX=1.89V, VCCDA=1.89V					1.08	1.09	1.1	

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
Output low level	V_{OL}	I_{OL}= 8mA, V_{CCA}=1.425V, VCCIBX=1.71V, VCCDA=1.71V	—	0.2	—	0.2	0.060	0.069	0.083	V
		I_{OL}= 8mA, V_{CCA}=1.500V, VCCIBX=1.80V, VCCDA=1.80V					0.057	0.066	0.079	
		I_{OL}= 8mA, V_{CCA}=1.575V, VCCIBX=1.89V, VCCDA=1.89V					0.054	0.063	0.075	
Output high level	V_{OH}	I_{OH}= -8mA, V_{CCA}=1.425V, VCCIBX=1.71V, VCCDA=1.71V	VCCI-0.2	—	VCCI-0.2	—	1.622	1.597	1.561	V
		I_{OH}=- 8mA, V_{CCA}=1.500V, VCCIBX=1.80V, VCCDA=1.80V					1.715	1.692	1.663	

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
		I_{OH}=- 8mA, V_{CCA}=1.575V, VCCIBX=1.89V, VCCDA=1.89V					1.805	1.787	1.755	
Port transmission delay	tDP+PY_H	HighSlew,V_{CCA}=1.425V, VCCIBX=1.71V	—	—	—	10.8	6.5	6.9	7.4	ns
	tDP+PY_L	LowSlew,V_{CCA}=1.425V, VCCIBX=1.71V	—	—	—	32.5	20.6	22.7	24.9	ns
1.5V LVCMOS ((VCCIBx=1.5±0.075V))										
Input low level	V_{IL}	V_{CCA}=1.425V, VCCIBX=1.425V, VCCDA=1.425V	-0.5	0.35VCCI	-0.5	0.35VCCI	0.81	0.81	0.82	V
		V_{CCA}=1.500V, VCCIBX=1.500V, VCCDA=1.500V					0.85	0.86	0.86	
		V_{CCA}=1.575V, VCCIBX=1.575V, VCCDA=1.575V					0.89	0.9	0.91	
Input high level	V_{IH}	V_{CCA}=1.425V, VCCIBX=1.425V, VCCDA=1.425V	0.65VCCI	1.95	0.65VCCI	1.95	0.82	0.83	0.83	V

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
		V_{CCA}=1.500V, VCCIBX=1.500V, VCCDA=1.500V					0.86	0.87	0.87	
		V_{CCA}=1.575V, VCCIBX=1.575V, VCCDA=1.575V					0.9	0.91	0.92	
Output low level	V_{OL}	I_{OL}= 8mA, V_{CCA}=1.425V, VCCIBX=1.425V, VCCDA=1.425V	—	0.4	—	0.4	0.081	0.092	0.105	V
		I_{OL}= 8mA, V_{CCA}=1.500V, VCCIBX=1.500V, VCCDA=1.500V					0.071	0.087	0.102	
		I_{OL}= 8mA, V_{CCA}=1.575V, VCCIBX=1.575V, VCCDA=1.575V					0.067	0.074	0.093	

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
Output high level	V_{OH}	I_{OH}= -8mA, V_{CCA}=1.425V, VCCIBX=1.425V, VCCDA=1.425V	VCCI-0.4	—	VCCI-0.4	—	1.312	1.281	1.242	V
		I_{OH}=- 8mA, V_{CCA}=1.500V, VCCIBX=1.500V, VCCDA=1.500V					1.397	1.365	1.329	
		I_{OH}=- 8mA, V_{CCA}=1.575V, VCCIBX=1.575V, VCCDA=1.575V					1.478	1.453	1.414	
Port transmission delay	tDP+PY_H	HighSlew,V_{CCA}=1.425V, VCCIBX=1.425V	—	—	—	13.4	9.5	10.0	10.7	ns
	tDP+PY_L	LowSlew,V_{CCA}=1.425V, VCCIBX=1.425V	—	—	—	46.5	37.4	36.8	38.2	ns
3.3V PCI (VCCIBx=3.3±0.3V)										
Input low level	V_{IL}	V_{CCA}=1.425V, VCCIBX=3.0V, VCCDA=3.0V	-0.5	0.3VCCI	-0.5	0.3VCCI	1.12	1.09	1.12	V
		V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V					1.21	1.19	1.2	

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
		V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V					1.34	1.25	1.27	
Input high level	V_{IH}	V_{CCA}=1.425V, VCCIBX=3.0V, VCCDA=3.0V	0.55VCCI	VCCI+0.5	0.55VCCI	VCCI+0.5	1.6	1.55	1.5	V
		V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V					1.76	1.71	1.65	
		V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V					1.91	1.86	1.8	
Output low level	V_{OL}	I_{OL}= 1.5mA, V_{CCA}=1.425V, VCCIBX=3.0V, VCCDA=3.0V	—	0.1VCCI	—	0.1VCCI	0.010	0.011	0.013	V
		I_{OL}= 1.5mA, V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V					0.009	0.012	0.013	
		I_{OL}= 1.5mA, V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V					0.009	0.011	0.013	
Output high level	V_{OH}	I_{OH}= -0.5mA V_{CCA}=1.425V, VCCIBX=3.0V, VCCDA=3.0V	0.9VCCI	—	0.9VCCI	—	2.987	2.980	2.971	V

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
		I_{OH}=-0.5mA, V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V					3.283	3.281	3.275	
		I_{OH}=-0.5mA, V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V					3.584	3.583	3.571	
Port transmission delay	tDP+PY_	V_{CCA}=1.425V, VCCIBX=3V	—	—	—	9.5	6.3	6.8	7.1	ns
3.3V GTL+ (VCCIBx=3.3±0.3V, VREF=1.0±0.1V)										
Input low level	V_{IL}	V_{CCA}=1.425V, VCCIBX=3.0V, VCCDA=3.0V,VREF=0.9V	—	VREF-0.1	—	VREF-0.1	0.85	0.86	0.86	V
		V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V,VREF=1.0V					0.96	0.95	0.96	
		V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V,VREF=1.1V					1.07	1.05	1.05	
Input high level	V_{IH}	V_{CCA}=1.425V, VCCIBX=3.0V, VCCDA=3.0V,VREF=0.9V	VREF+0.1	—	VREF+0.1	—	0.93	0.93	0.93	V
		V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V,VREF=1.0V					1.04	1.03	1.03	

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
		V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V,VREF=1.1V					1.14	1.14	1.14	
Output low level	V_{OL}	I_{OL}= 4mA,VREF=0.9V V_{CCA}=1.425V, VCCIBX=3.0V, VCCDA=3.0V	—	0.6	—	0.6	0.031	0.034	0.038	V
		I_{OL}=-4mA,VREF=1.0V V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V					0.031	0.034	0.038	
		I_{OL}=-4mA,VREF=1.1V V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V					0.031	0.034	0.037	
Port transmission delay	tDP+PY_	V_{CCA}=1.425V, VCCIBX=3V, VREF=0.9V	—	—	—	8.0	4.7	5.1	5.4	ns
1.5V HSTL Class I (VCCIBx=1.5±0.075V, VREF=0.75±0.04V)										
Input low level	V_{IL}	V_{CCA}=1.425V, VCCIBX=1.425V, VCCDA=1.425V,VREF=0.71V	-0.3	VREF-0.1	-0.3	VREF-0.1	0.66	0.70	0.70	V

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
		V_{CCA}=1.500V, VCCIBX=1.500V, VCCDA=1.500V,VREF=0.75V					0.74	0.74	0.74	
		V_{CCA}=1.575V, VCCIBX=1.575V, VCCDA=1.575V,VREF=0.79V					0.78	0.78	0.78	
Input high level	V_{IH}	V_{CCA}=1.425V, VCCIBX=1.425V, VCCDA=1.425V,VREF=0.71V	VREF+0.1	3.6	VREF+0.1	3.6	0.73	0.72	0.72	V
		V_{CCA}=1.500V, VCCIBX=1.500V, VCCDA=1.500V,VREF=0.75V					0.76	0.76	0.76	
		V_{CCA}=1.575V, VCCIBX=1.575V, VCCDA=1.575V,VREF=0.79V					0.80	0.80	0.80	

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
Output low level	V_{OL}	I_{OL}= 8mA,VREF=0.71V V_{CCA}=1.425V, VCCIBX=1.425V, VCCDA=1.425V	—	0.4	—	0.4	0.080	0.091	0.106	V
		I_{OL}= 8mA,VREF=0.75V V_{CCA}=1.500V, VCCIBX=1.500V, VCCDA=1.500V					0.074	0.084	0.099	
		I_{OL}= 8mA,VREF=0.79V V_{CCA}=1.575V, VCCIBX=1.575V, VCCDA=1.575V					0.069	0.078	0.093	
Output high level	V_{OH}	I_{OH}= -8mA,VREF=0.71V V_{CCA}=1.425V, VCCIBX=1.425V, VCCDA=1.425V	VCCI-0.4	—	VCCI-0.4	—	1.317	1.285	1.244	V
		I_{OH}=- 8mA,VREF=0.75V V_{CCA}=1.500V, VCCIBX=1.500V, VCCDA=1.500V					1.398	1.369	1.331	

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
		I_{OH}=- 8mA,VREF=0.79V V_{CCA}=1.575V, VCCIBX=1.575V, VCCDA=1.575V					1.479	1.451	1.415	
Port transmission delay	tDP+PY	V_{CCA}=1.425V, VCCIBX=1.425V, VREF=0.71V	—	—	—	8.5	5.6	6.0	6.4	ns
2.5V SSTL2 Class I (VCCIBx=2.5±0.125V, VREF=1.25±0.06V)										
Input low level	V_{IL}	V_{CCA}=1.425V, VCCIBX=2.375V, VCCDA=2.375V,VREF=1.19V	-0.3	VREF-0.2	-0.3	VREF-0.2	1.11	1.05	1.14	V
		V_{CCA}=1.500V, VCCIBX=2.500V, VCCDA=2.500V,VREF=1.25V					1.08	1.12	1.2	
		V_{CCA}=1.575V, VCCIBX=2.625V, VCCDA=2.625V,VREF=1.31V					1.25	1.28	1.17	

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
Input high level	V_{IH}	V_{CCA}=1.425V, VCCIBX=2.375V, VCCDA=2.375V,VREF=1.19V	VREF+0.2	3.6	VREF+0.2	3.6	1.21	1.25	1.29	V
		V_{CCA}=1.500V, VCCIBX=2.500V, VCCDA=2.500V,VREF=1.25V					1.36	1.37	1.3	
		V_{CCA}=1.575V, VCCIBX=2.625V, VCCDA=2.625V,VREF=1.31V					1.45	1.42	1.39	
Output low level	V_{OL}	I_{OL}= 7.6mA,VREF=1.19V V_{CCA}=1.425V, VCCIBX=2.375V, VCCDA=2.375V	—	VREF-0.57	—	VREF-0.57	0.041	0.048	0.059	V
		I_{OL}= 7.6mA,VREF=1.25V V_{CCA}=1.500V, VCCIBX=2.500V, VCCDA=2.500V					0.04	0.047	0.057	

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
		I_{OL}= 7.6mA,VREF=1.31V V_{CCA}=1.575V, VCCIBX=2.625V, VCCDA=2.625V					0.039	0.045	0.055	
Output high level	V_{OH}	I_{OH}= -7.6mA,VREF=1.19V V_{CCA}=1.425V, VCCIBX=2.375V, VCCDA=2.375V	VREF+0.57	—	VREF+0.57	—	2.309	2.293	2.271	V
		I_{OH}=-7.6mA,VREF=1.25V V_{CCA}=1.500V, VCCIBX=2.500V, VCCDA=2.500V					2.436	2.42	2.400	
		I_{OH}=-7.6mA,VREF=1.31V V_{CCA}=1.575V, VCCIBX=2.625V, VCCDA=2.625V					2.563	2.548	2.528	
Port transmission delay	tDP+PY	V_{CCA}=1.425V, VCCIBX=2.375V, VREF=1.19V	—	—	—	8.0	4.7	5.1	5.4	ns
2.5V SSTL2 Class II (VCCIBx=2.5±0.125V, VREF=1.25±0.06V)										

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
Input low level	V_{IL}	V_{CCA}=1.425V, VCCIBX=2.375V, VCCDA=2.375V,VREF=1.19V	-0.3	VREF-0.2	-0.3	VREF-0.2	1.18	1.18	1.18	V
		V_{CCA}=1.500V, VCCIBX=2.500V, VCCDA=2.500V,VREF=1.25V					1.24	1.24	1.24	
		V_{CCA}=1.575V, VCCIBX=2.625V, VCCDA=2.625V,VREF=1.31V					1.30	1.30	1.30	
Input high level	V_{IH}	V_{CCA}=1.425V, VCCIBX=2.375V, VCCDA=2.375V,VREF=1.19V	VREF+0.2	3.6	VREF+0.2	3.6	1.20	1.20	1.20	V
		V_{CCA}=1.500V, VCCIBX=2.500V, VCCDA=2.500V,VREF=1.25V					1.26	1.26	1.26	

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
		V_{CCA}=1.575V, VCCIBX=2.625V, VCCDA=2.625V,VREF=1.31V					1.32	1.32	1.32	
Output low level	V_{OL}	I_{OL}= 15.2mA,VREF=1.19V V_{CCA}=1.425V, VCCIBX=2.375V, VCCDA=2.375V	—	VREF-0.8	—	VREF-0.8	0.097	0.103	0.106	V
		I_{OL}= 15.2mA,VREF=1.25V V_{CCA}=1.500V, VCCIBX=2.500V, VCCDA=2.500V					0.098	0.102	0.104	
		I_{OL}= 15.2mA,VREF=1.31V V_{CCA}=1.575V, VCCIBX=2.625V, VCCDA=2.625V					0.097	0.099	0.105	
Output high level	V_{OH}	I_{OH}= -15.2mA,VREF=1.19V V_{CCA}=1.425V, VCCIBX=2.375V, VCCDA=2.375V	VREF+0.8	—	VREF+0.8	—	2.236	2.200	2.148	V

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
		I_{OH}=-15.2mA,VREF=1.25V V_{CCA}=1.500V, VCCIBX=2.500V, VCCDA=2.500V					2.365	2.33	2.283	
		I_{OH}=-15.2mA,VREF=1.31V V_{CCA}=1.575V, VCCIBX=2.625V, VCCDA=2.625V					2.494	2.463	2.415	
Port transmission delay	tDP+PY	V_{CCA}=1.425V, VCCIBX=2.375V, VREF=1.19V	—	—	—	8.0	4.7	5.1	5.4	ns
3.3V SSTL3 Class I (VCCCIBx=3.3±0.3V, VREF=1.5±0.15V)										
Input low level	V_{IL}	V_{CCA}=1.425V, VCCIBX=3.0V, VCCDA=3.0V,VREF=1.35V	-0.3	VREF-0.2	-0.3	VREF-0.2	1.32	1.32	1.32	V
		V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V,VREF=1.50V					1.47	1.47	1.47	
		V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V,VREF=1.65V					1.63	1.43	1.62	
Input high level	V_{IH}	V_{CCA}=1.425V, VCCIBX=3.0V, VCCDA=3.0V,VREF=1.35V	VREF+0.2	3.6	VREF+0.2	3.6	1.36	1.36	1.36	V

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
		V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V,VREF=1.50V					1.52	1.52	1.53	
		V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V,VREF=1.65V					1.66	1.67	1.67	
Output low level	V_{OL}	I_{OL}= 8mA,VREF=1.35V V_{CCA}=1.425V, VCCIBX=3.0V, VCCDA=3.0V	—	VREF-0.6	—	VREF-0.6	0.047	0.051	0.076	V
		I_{OL}= 8mA,VREF=1.50V V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V					0.047	0.051	0.073	
		I_{OL}= 8mA,VREF=1.65V V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V					0.042	0.051	0.076	
Output high level	V_{OH}	I_{OH}= -8mA,VREF=1.35V V_{CCA}=1.425V, VCCIBX=3.0V, VCCDA=3.0V	VREF+0.6	—	VREF+0.6	—	2.929	2.909	2.891	V
		I_{OH}=-8mA,VREF=1.50V V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V					3.231	3.216	3.184	

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
		I_{OH}=-8mA,VREF=1.65V V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V					3.534	3.516	3.481	
Port transmission delay	tDP+PY	V_{CCA}=1.425V, VCCIBX=3V, VREF=1.35V	—	—	—	7.5	4.5	4.9	5.1	ns
3.3V SSTL3 Class II (VCCCIBx=3.3±0.3V, VREF=1.5±0.15V)										
Input low level	V_{IL}	V_{CCA}=1.425V, VCCIBX=3.0V, VCCDA=3.0V,VREF=1.35V	-0.3	VREF-0.2	-0.3	VREF-0.2	1.29	1.30	1.32	V
		V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V,VREF=1.50V					1.45	1.44	1.46	
		V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V,VREF=1.65V					1.59	1.59	1.61	
Input high level	V_{IH}	V_{CCA}=1.425V, VCCIBX=3.0V, VCCDA=3.0V,VREF=1.35V	VREF+0.2	3.6	VREF+0.2	3.6	1.36	1.36	1.36	V
		V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V,VREF=1.50V					1.51	1.51	1.51	
		V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V,VREF=1.65V					1.66	1.66	1.66	

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
Output low level	V_{OL}	I_{OL}= 16mA,VREF=1.35V V_{CCA}=1.425V, VCCIBX=3.0V, VCCDA=3.0V	—	VREF-0.8	—	VREF-0.8	0.082	0.101	0.126	V
		I_{OL}= 16mA,VREF=1.50V V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V					0.095	0.096	0.120	
		I_{OL}= 16mA,VREF=1.65V V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V					0.092	0.093	0.117	
Output high level	V_{OH}	I_{OH}= -16mA,VREF=1.35V V_{CCA}=1.425V, VCCIBX=3.0V, VCCDA=3.0V	VREF+0.8	—	VREF+0.8	—	2.860	2.831	2.787	V
		I_{OH}=-16mA,VREF=1.50V V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V					3.165	3.139	3.099	
		I_{OH}=-16mA,VREF=1.65V V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V					3.470	3.454	3.407	
Port transmission delay	tDP+PY	V_{CCA}=1.425V, VCCIBX=3V, VREF=1.35V	—	—	—	7.5	4.5	4.8	5.1	ns

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
2.5V LVDS (VCCIBx=2.5±0.125V, VCCDA=3.3±0.3V,)										
Output low level	V_{OL}	V_{CCA}=1.425V,VCCIBX=2.375V, VCCDA=3.0V	—	1.25	—	1.25	1.011	1.008	1.006	V
		V_{CCA}=1.500V, VCCIBX=2.5V, VCCDA=3.3V					1.064	1.062	1.059	
		V_{CCA}=1.575V, VCCIBX=2.625V, VCCDA=3.6V					1.118	1.115	1.113	
Output high level	V_{OH}	V_{CCA}=1.425V,VCCIBX=2.375V, VCCDA=3.0V	1.25	—	1.25	—	1.344	1.339	1.334	V
		V_{CCA}=1.500V, VCCIBX=2.5V, VCCDA=3.3V					1.415	1.410	1.405	
		V_{CCA}=1.575V, VCCIBX=2.625V, VCCDA=3.6V					1.486	1.481	1.477	
Differential output voltage	VODIFF	V_{CCA}=1.425V,VCCIBX=2.375V, VCCDA=3.0V	250	450	250	450	333	331	328	mV
		V_{CCA}=1.500V, VCCIBX=2.5V, VCCDA=3.3V					351	348	346	

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
		V_{CCA}=1.575V, VCCIBX=2.625V, VCCDA=3.6V					368	366	364	
Output common mode voltage	VOCM	V_{CCA}=1.425V,VCCIBX=2.375V, VCCDA=3.0V	1.125	1.375	1.125	1.375	1.1775	1.1735	1.17	V
		V_{CCA}=1.500V, VCCIBX=2.5V, VCCDA=3.3V					1.2395	1.236	1.232	
		V_{CCA}=1.575V, VCCIBX=2.625V, VCCDA=3.6V					1.302	1.298	1.295	
Input common mode voltage	VICM	V_{CCA}=1.425V,VCCIBX=2.375V, VCCDA=3.0V	0.2	2.2	0.2	2.2	Pass	Pass	Pass	V
		V_{CCA}=1.500V, VCCIBX=2.5V, VCCDA=3.3V					Pass	Pass	Pass	
		V_{CCA}=1.575V, VCCIBX=2.625V, VCCDA=3.6V					Pass	Pass	Pass	
Port transmission delay	tDP+PY	V_{CCA}=1.425V, VCCIBX=2.375V, VCCDA=3V	—	—	—	8.5	5.4	5.9	6.4	ns
3.3V LVPECL (VCCIBx=3.3±0.3V)										

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
Input low level	V_{IL}	V_{CCA}=1.425V,VCCIBX=3.0V, VCCDA=3.0V	0.86	2.125	0.86	2.125	0.9	0.89	0.89	V
		V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V					0.91	0.9	0.89	
		V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V					0.91	0.91	0.9	
Input high level	V_{IH}	V_{CCA}=1.425V,VCCIBX=3.0V, VCCDA=3.0V	1.49	2.72	1.49	2.72	2.67	2.68	2.68	V
		V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V					2.66	2.67	2.68	
		V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V					2.66	2.66	2.67	
Output low level	V_{OL}	V_{CCA}=1.425V,VCCIBX=3.0V, VCCDA=3.0V	0.96	1.57	0.96	1.57	1.133	1.130	1.128	V
		V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V					1.246	1.243	1.241	
		V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V					1.356	1.356	1.353	
Output high level	V_{OH}	V_{CCA}=1.425V,VCCIBX=3.0V, VCCDA=3.0V	1.8	2.41	1.8	2.41	1.836	1.827	1.817	V

Characteristic	symbol	condition	RTAX1000 US military standard		This specification		Measured value			unit
		Unless otherwise specified, 1.425V≤VCCA≤1.575V, VCCDA=VCCIBx, -55℃≤TA≤125℃	Minimum	maximum	Minimum	maximum	Low temperature -55℃	Normal temperature 25℃	high temperature 125℃	
		V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V					2.021	2.014	2.001	
		V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V					2.206	2.197	2.185	
Differential input voltage	VIDIFF	V_{CCA}=1.425V,VCCIBX=3.0V, VCCDA=3.0V	0.3	—	0.3	—	0.05	0.04	0.04	V
		V_{CCA}=1.500V, VCCIBX=3.3V, VCCDA=3.3V					0.06	0.05	0.04	
		V_{CCA}=1.575V, VCCIBX=3.6V, VCCDA=3.6V					0.06	0.06	0.05	
Port transmission delay	tDP+PY	V_{CCA}=1.425V, VCCIBX=3V	—	—	—	9.2	6.1	6.5	7.0	ns

Notes on import substitution

When BSTRTAX1000 replaces RTAX1000 and AX1000, the following aspects should be noted:

- In terms of user-available I/O ports, the BSTRTAX1000 device has the same ports as the RTAX1000 device; however, compared to the AX1000, the BSTRTAX1000 device has 8 fewer PLLs, so the 16 PLL ports corresponding to the 8 PLLs are changed to NC ports; the connections do not need to be adjusted.
- In terms of package size, the package sizes of BSTRTAX1000-CQ352 devices, BSTRTAX1000-CQ352 devices and AX1000-CQ352 devices are the same (BSTRTAX1000-CQ352 devices are slightly thicker than foreign circuits) and can be plugged in and replaced.
- In terms of power consumption, due to SEU reinforcement, the internal 6048 R units and all I/O registers of the BSTRTAX1000 and RTAX1000 devices all adopt a triple-mode redundant design, resulting in an increase in power consumption compared to the AX1000 devices at the same resource utilization and operating frequency. Therefore, if the power consumption is high after replacement, heat treatment is required, which may lead to changes in PCB design. The power consumption of BSTRTAX1000 is comparable to that of RTAX1000, and the simulated power consumption in Libero IDE can be used for reference and evaluation (see Appendix E).
- In terms of development environment and programming, Libero IDE (Integrated Design Environment) and a programmer from a foreign BPM company were used. The development and programming process is as follows.
  - Create a new project and select the device BSTRTAX1000-CQ352;
  - If the user has an original code file based on AX1000-CQ352 and does not use PLL, then import it directly without changing the original code file. After importing, the code needs to be recompiled;

- If there is no original code, new code can be developed directly in this RT series engineering environment;
- The subsequent compilation, synthesis and simulation operation process is the same as that of the A series;
- When programming, select BSTRTAX1000-CQ352 as the device.
- Unused clock pins should be connected to power or ground. Unused I/O pins are in high impedance state internally and are recommended to be left floating or connected to power or ground.