BSTPLL02-0015Q
Frequency Synthesizer
Data Sheet

I. Product Introduction

BSTPLL02-0015Q is a broadband frequency synthesizer integrated with a VCO, supporting an RF bandwidth output from 0.9375 to 15 GHz and a maximum phase-locked detection frequency of 200 MHz (integer mode) or 50 MHz (fractional mode).

There is no pre-divider inside the chip, and it integrates reference divider, phase detector, charge pump and feedback divider modules, AFC automatic calibration algorithm, 7.5~15GHz VCO direct output, no wandering spurious.

II. Key Technical Indicators

- **Frequency range**:
- Integer mode: 0.9375~15GHz
- Fractional mode: 0.9375~15GHz
- **Normalized noise floor**:
- Integer mode: -235dBc/Hz
- Fractional mode: -230dBc/Hz
- **Maximum phase detection frequency**:
- Integer mode: 200MHz
- Fractional mode: 50MHz
- **Power consumption**:
- Baseband direct output: 290mA
- Output 8-way frequency open: 300mA
- Package: 6.00mm × 6.00mm QFN-40L

III. Functional Block Diagram

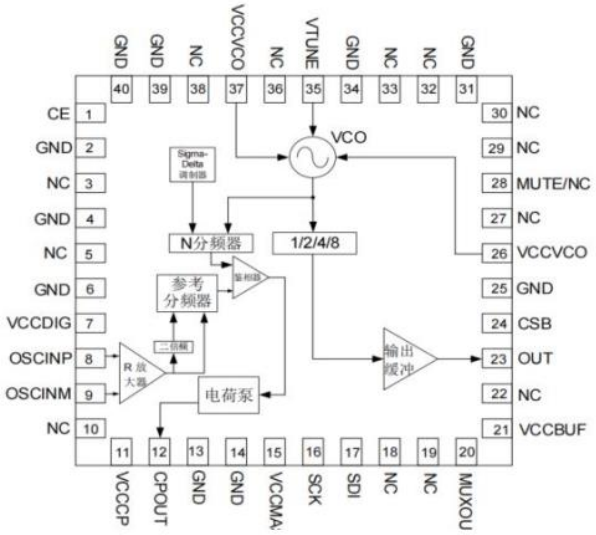

Figure 1

IV. Typical Applications

- Wireless Infrastructure
- Point-to-point radio
- Point-to-multipoint radio
- Test equipment and instruments

V. Electrical Performance Table (T_A = +25°C, V_{CCDIG} = V_{CCCP} = V_{CCMASH} = V_{CCBUF} = V_{CCVCO} = 3.3V)

Table 1

TEST PARAMETERS	DESCRIBE	UNIT	INDICATOR PARAMETERS		
			MINIMUM	NOMINAL	MAXIMUM
Output Parameters					
VOC fundamental frequency		GHz	7.5		15
Input power	Single-ended output	dBm		0	
Input Path					
Reference input frequency	Enable 2x frequency	MHz		TBD	
	Turn off 2x frequency	MHz		350	
Reference input power	5~200MHz	dBm	-5		10
Phase detector and charge pump parameters					

Phase detector frequency range	Integer mode	MHz	2		200
	Decimal mode	MHz	2		50
RF frequency range	Integer mode	GHz	0.9375		15
	Decimal mode	GHz	0.9375		15
CP current		mA		7.6	
Reset current		mA		180	
Shutdown current		mA		25	
Power consumption	Baseband direct output	mA		290	320
	Output 8 -way frequency open	mA		300	335

VI. Electrical Performance Table (T_A = +25°C, V_{CCDIG} = V_{CCCP} = V_{CCMASH} = V_{CCBUF} = V_{CCVCO} = 3.3V)

Table 2

TEST PARAMETERS		DESCRIBE	UNIT	INDICATOR PARAMETERS		
				MINIMUM	NOMINAL	MAXIMUM
PLL closed-loop parameters						
Normalized noise floor		Integer mode, P_D=100MHz, V_{CO}=15GHz	dBc/Hz		-235	
		Decimal mode, P_D=100MHz, V_{CO}=15.0001GHz	dBc/Hz		-230	
Normalized flicker noise		Integer mode @10KHz offset	dBc/Hz		-131	
Normalized flicker noise		Fractional mode @10KHz offset	dBc/Hz		-130	
Phase noise	Phase noise @1KHz	P_D=100MHz, P_{REF}=10dBm, Fout=7.5GHz integer mode	dBc/Hz		-103	
	Phase noise @10KHz		dBc/Hz		-111	
	Phase noise @100KHz		dBc/Hz		-112	
	Phase noise @1MHz		dBc/Hz		-114	
	Phase noise @10MHz		dBc/Hz		-145	
	Phase noise @100MHz		dBc/Hz		-152	
Phase noise	Phase noise @1KHz	P_D=50MHz, P_{REF}=10dBm, Fout=7.5001GHz fractional mode	dBc/Hz		-100	
	Phase noise @10KHz		dBc/Hz		-107	
	Phase noise @100KHz		dBc/Hz		-105	
	Phase noise @1MHz		dBc/Hz		-110	

TEST PARAMETERS		DESCRIBE	UNIT	INDICATOR PARAMETERS		
				MINIMUM	NOMINAL	MAXIMUM
	Phase noise @10MHz		dBc/Hz		-130	
	Phase noise @100MHz		dBc/Hz		-151	
Phase noise	Phase noise @1KHz	P_D=100MHz, P_{REF}=10dBm, F_{OUT}=15GHz integer mode	dBc/Hz		-97	
	Phase noise @10KHz		dBc/Hz		-102	
	Phase noise @100KHz		dBc/Hz		-104	
	Phase noise @1MHz		dBc/Hz		-110	
	Phase noise @10MHz		dBc/Hz		-141	
	Phase noise @100MHz		dBc/Hz		-151	
Phase noise	Phase noise @1KHz	P_D=100MHz, P_{REF}=10dBm, F_{OUT}=15,0001 GHz fractional mode	dBc/Hz		-94	
	Phase noise @10KHz		dBc/Hz		-97	
	Phase noise @100KHz		dBc/Hz		-98	
	Phase noise @1MHz		dBc/Hz		-103	
	Phase noise @10MHz		dBc/Hz		-133	
	Phase noise @100MHz		dBc/Hz		-151	
Frequency hopping time [1]		P_D=100MHz, P_{REF}=10dBm	us		25	
Logic Input	High level	SPI signal, CE signal	V	2		
	Low level		V			0.5
Logic Output	High level	Current 1mA	V	2.9		
	Low level		V			0.4
Lock detection		High level after locking, low level after unlocking				

To achieve fast frequency hopping, a high phase detection frequency is required

VII. Electrical Performance Table (T_A = +25°C, V_{CCDIG} = V_{CCCP} = V_{CCMASH} = V_{CCBUF} = V_{CCVCO} = 3.3V)

Table 3

TEST PARAMETERS		DESCRIBE	UNIT	INDICATOR PARAMETERS		
				MINIMUM	NOMINAL	MAXIMUM
V_{CO} open-loop parameters						
Tuning sensitivity @V_{CO1}		Kv	MHz/V	151		351.6
Tuning sensitivity @V_{CO2}		Kv	MHz/V	106.1		333.7
Tuning sensitivity @V_{CO4}		Kv	MHz/V	88.4		342.4
V_{CO} tuning voltage		The loop filter is an active loop	V	0		3.3
		The loop filter is a passive loop	V	0.3		3
Phase noise	Phase noise @10KHz	F_{OUT}=7.5GHz	dBc/Hz		-82	
	Phase noise @100KHz		dBc/Hz		-106	
	Phase noise @1MHz		dBc/Hz		-127	
	Phase noise @10MHz		dBc/Hz		-145	
	Phase noise @100MHz		dBc/Hz		-150	
Phase noise	Phase noise @10KHz	F_{OUT} =10GHz	dBc/Hz		-83	
	Phase noise @100KHz		dBc/Hz		-105	
	Phase noise @1MHz		dBc/Hz		-127	
	Phase noise @10MHz		dBc/Hz		-147	
	Phase noise @100MHz		dBc/Hz		-151	
Phase noise	Phase noise @10KHz	F_{OUT} =12GHz	dBc/Hz		-88	
	Phase noise @100KHz		dBc/Hz		-105	
	Phase noise @1MHz		dBc/Hz		-126	
	Phase noise @10MHz		dBc/Hz		-145	
	Phase noise @100MHz		dBc/Hz		-151	
Phase noise	Phase noise @10KHz	F_{OUT} =15GHz	dBc/Hz		-70	

TEST PARAMETERS		DESCRIBE	UNIT	INDICATOR PARAMETERS		
				MINIMUM	NOMINAL	MAXIMUM
	Phase noise @100KHz		dBc/Hz		-97	
	Phase noise @1MHz		dBc/Hz		-120	
	Phase noise @10MHz		dBc/Hz		-140	
	Phase noise @100MHz		dBc/Hz		-149	

VIII. Electrical Performance Table (T_A = +25°C, V_{CCDIG} = V_{CCCP} = V_{CCMASH} = V_{CCBUF} = V_{CCVCO} = 3.3V)

1K flicker noise: (the frequency unit in brackets is Hz)

PNflick = Flicker F0M +20log(fvco) -10log(foffset)

Normalized 10K flicker noise: (Frequency in brackets is in Hz)

PNflick = Flicker F0M +20log(fvco/1GHz) -10log(foffset/10kHz)

Frequency calculation method:

$$f_{vco} = f_{\text{int}} + f_{frac} = \frac{f_{xtal}}{R}(N_{\text{int}} + \frac{N_{\text{frac}}}{2^{24}}) = f_{PD}(N_{\text{int}} + \frac{N_{\text{frac}}}{2^{24}})$$

$N_{int:}$ integer division ratio, REG02h; integer division mode: division ratio range 20 to 2^{15} -1; fractional division mode: division ratio range 23 to 2^{15} -1;

$N_{frac:}$ Fractional part, the range of fractional part is 0 to 2^{24} -1, REG03h;

R: Reference division ratio, the range of division ratio is 1 to $2^{14,}$ REG01h;

$f_{xtal:}$ Reference input frequency;

fPD: phase detection frequency, fxtal / R

For example, integer mode outputs 10G and fractional mode outputs 10GHz+1MHz:

Integer mode: f_{xtal} = 100 MHz, R = 1, f_{PFD} = 100 MHz, N_{int} = 100, N_{frac} = 0 ;

$$f_{vco} = f_{\text{int}} + f_{frac} = \frac{f_{xtal}}{R} \times (N_{\text{int}} + \frac{N_{\text{frac}}}{2^{24}}) = f_{PD} \times (N_{\text{int}} + \frac{N_{\text{frac}}}{2^{24}})$$

=100 × (100 +0) =10.0 GHz Fractional mode: f_{xtal} = 100 MHz, R = 1, f_{PFD} = 100 MHz, N_{int} = 100, N_{frac} = 167772;

$$f_{vco} = f_{\text{int}} + f_{frac} = \frac{f_{xtal}}{R} \times (N_{\text{int}} + \frac{N_{frac}}{2^{24}}) = f_{PD} \times (N_{\text{int}} + \frac{N_{frac}}{2^{24}})$$

=100 × (100 +167772/224) = 10.0 GHz +1 MHz

IX. Test Curve

(T_A = +25°C, V_{CCDIG} = V_{CCCP} = V_{CCMASH} = V_{CCBUF} = V_{CCVCO} = 3.3 V)

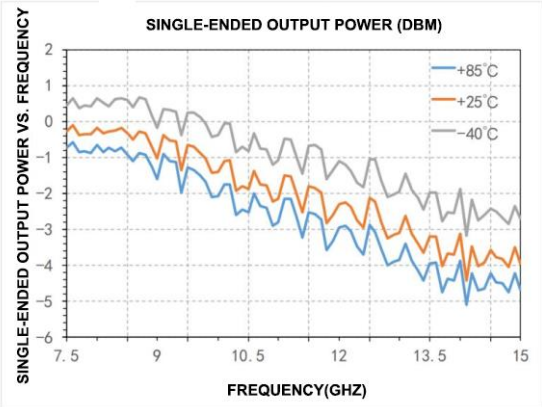

Figure 2

9.1. VCO Test Curve

(V_{CCDIG} = V_{CCCP} = V_{CCMASH} = V_{CCBUF} = V_{CCVCO} = 3.3V)

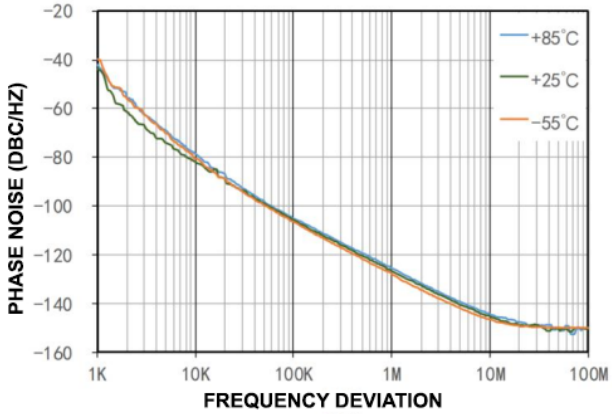

Figure 3. Phase Noise vs. Frequency Deviation (Fout = 7.5GHz)

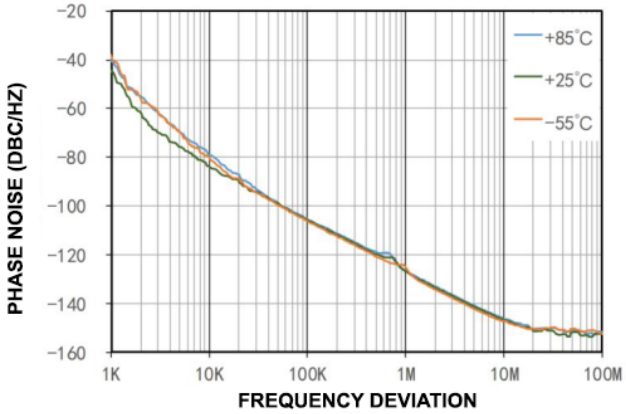

Figure 4. Phase Noise vs. Frequency Deviation (Fout = 10GHz)

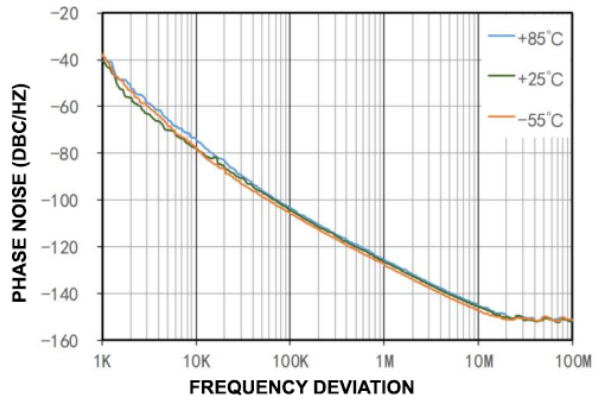

Figure 5. Phase Noise vs. Frequency Offset (Fout = 12 GHz)

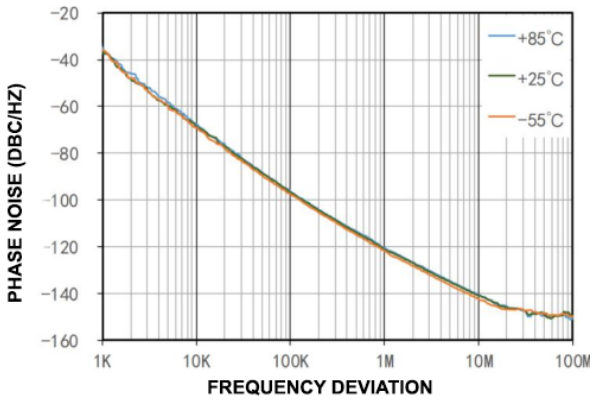

Figure 6. Phase Noise vs. Frequency Offset (Fout = 15 GHz)

9.2. Test Curve (Integer Mode R_{EF}=10dbm, P_D=100mhz)

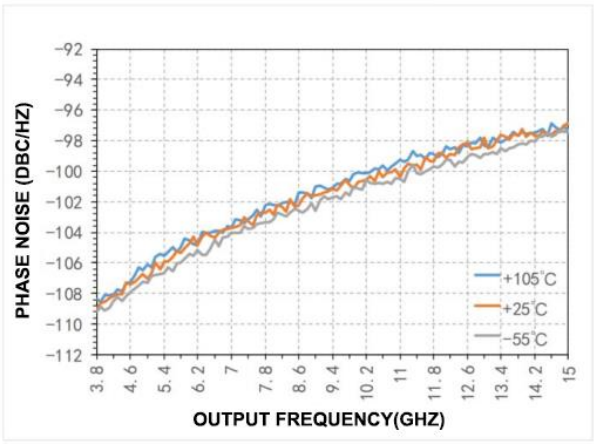

Figure 7. Phase Noise vs. Output Frequency (@ 1kHz Offset)

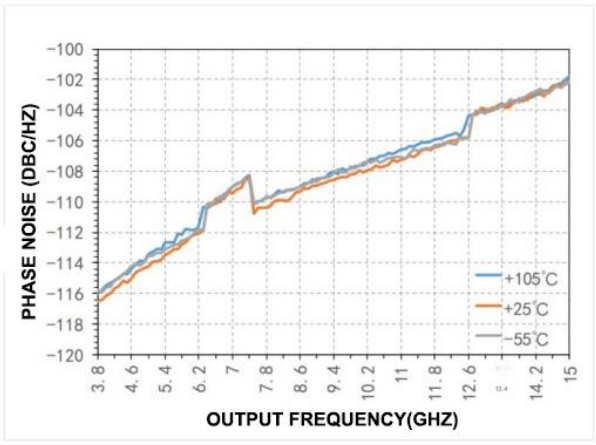

Figure 8. Phase Noise vs. Output Frequency (@ 10kHz Offset)

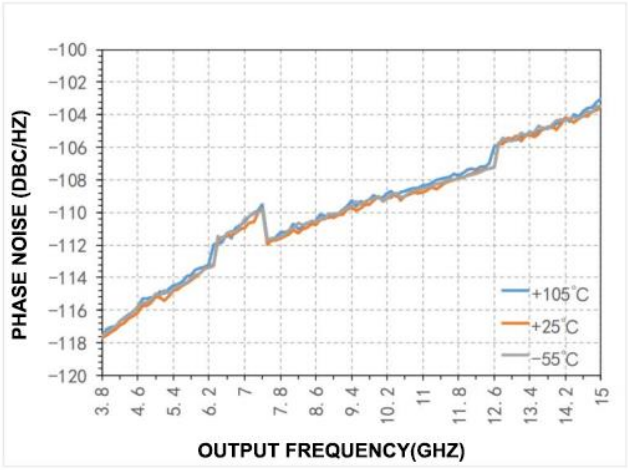

Figure 9. Phase Noise vs. Output Frequency (@ 100kHz Offset)

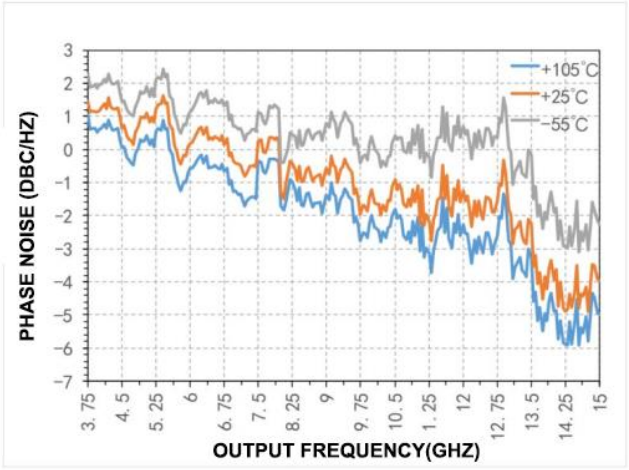

Figure 10. Phase Noise vs. Output Frequency (@ 10kHz Offset)

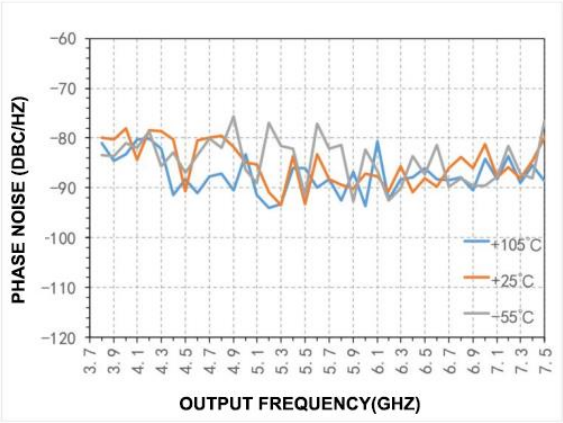

Figure 11. Output frequency vs. phase-locked leakage @3.8~7. 5GHz

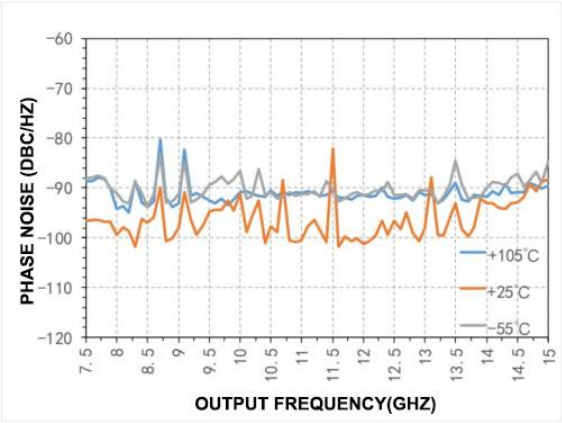

Figure 12. Output frequency vs. phase-locked leakage @7.5~15GHz

9.3. Test Curve (Decimal Mode P_{REF}=10dBm, P_D=50MHz)

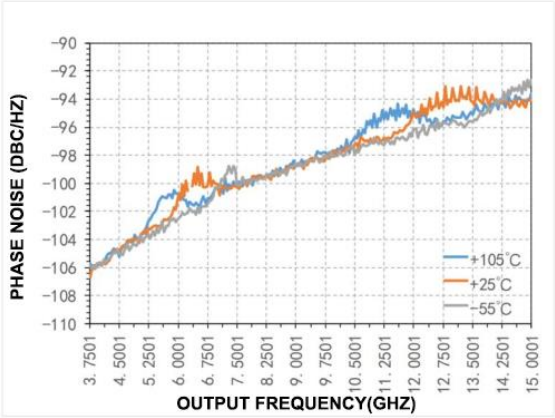

Figure 13. Phase Noise vs. Output Frequency (@ 1kHz Offset)

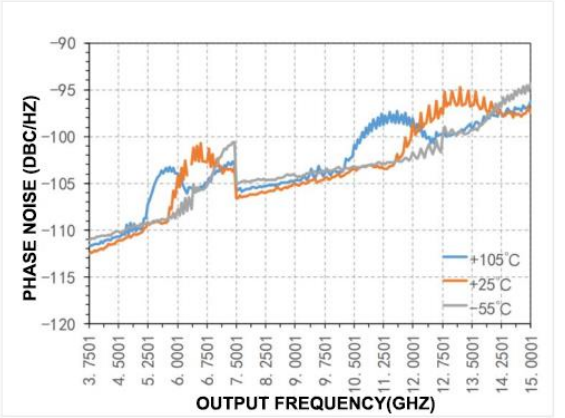

Figure 14. Phase Noise vs. Output Frequency (@ 10kHz Offset)

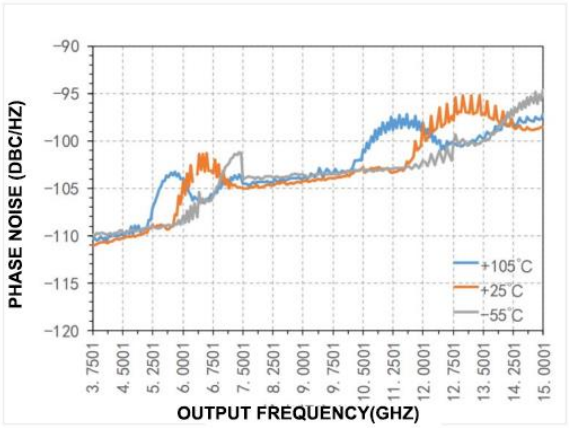

Figure 15. Phase Noise vs. Output Frequency (@ 10kHz Offset)

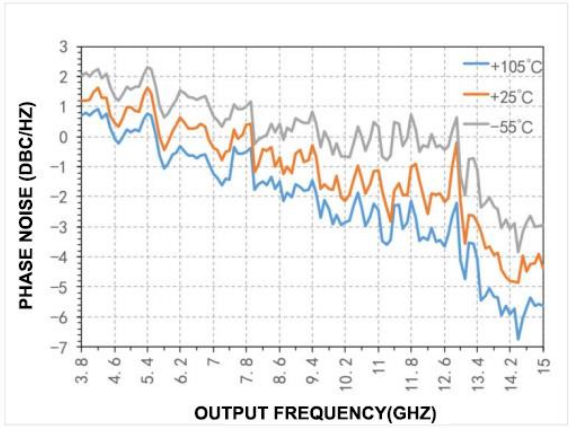

Figure 16. Output Frequency vs. 0 Offset Power

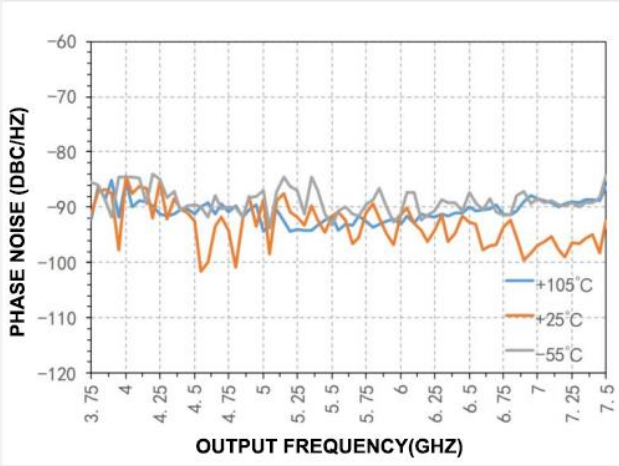

Figure 17. Output frequency vs. phase-locked leakage @3.75~7.5GHz

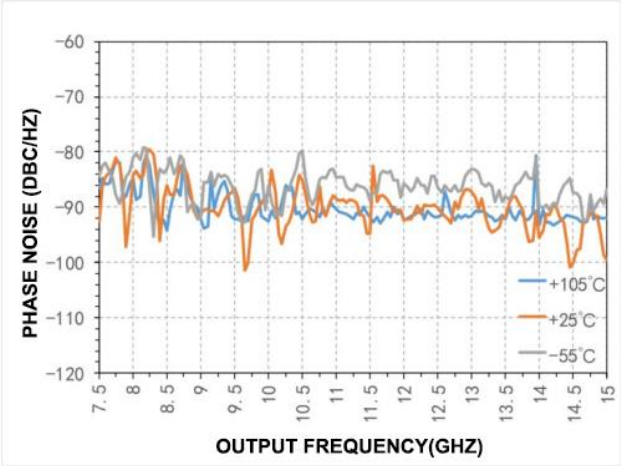

Figure 18. Output frequency vs. phase-locked leakage @7.5~15GHz

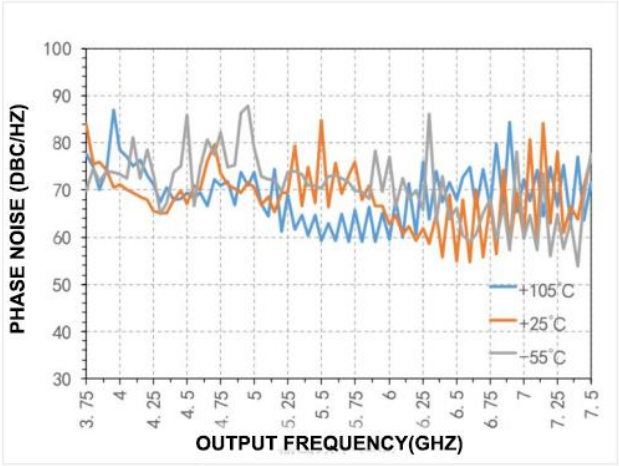

Figure 19. Output frequency vs integer boundary spurs @3.75~7.5GHz

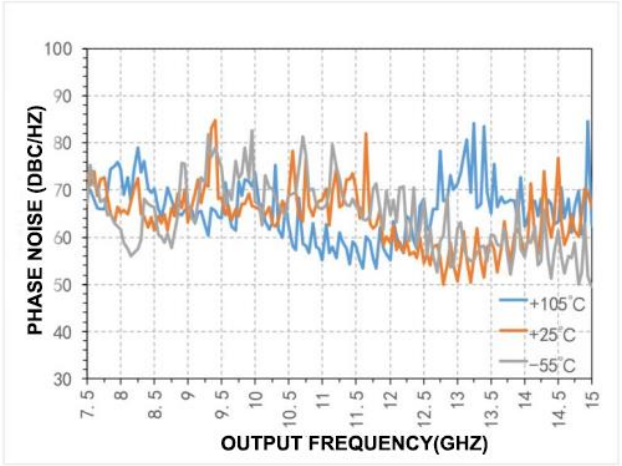

Figure 20. Output frequency vs integer boundary spurs @7.5~15GHz

X. Absolute Maximum Ratings

Table 4

PARAMETER	SYMBOL	MINIMUM	TYPICAL VALUES	MAXIMUM	UNIT
VCCDIG, VCCCP, VCCMASH, VCCBUF, VCCVCO		-0.3		+3.6	V
Storage temperature		-65		+150	℃
Operating temperature	TA	-40		+85	℃
Maximum normal operating junction temperature	Tjmax		+125		℃
Thermal resistance	RJc		TBD		℃ /W

PARAMETER	SYMBOL	MINIMUM	TYPICAL VALUES	MAXIMUM	UNIT
Electrostatic protection level	HBM		TBD		V

XI. Package Information

Table 5

MODEL	PACKAGING MATERIALS	PAD PLATING	MSL LEVEL [1]	ENVIRONMENTAL PROTECTION REQUIREMENTS
BSTPLL02-0015Q	Green resin compound	NiPdAuAg	MSL 3	RoHS compliant

[1] Maximum reflow temperature 260 °C

XII. SPI Control Description

12.1. Serial Data Timing Diagram

Write Timing

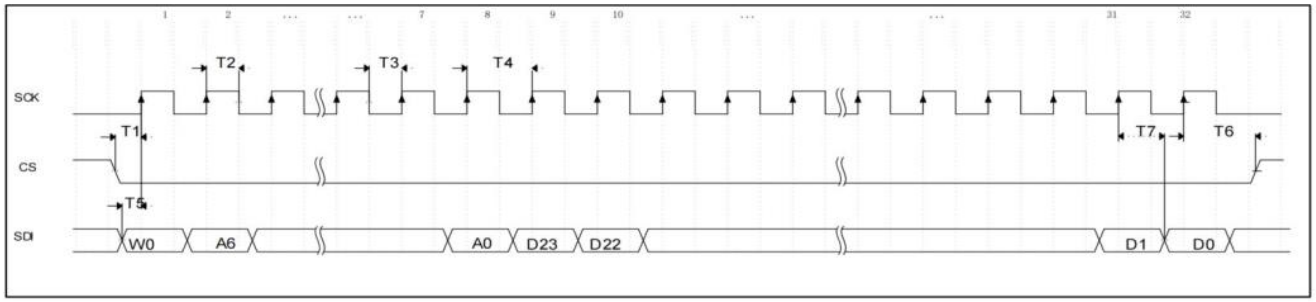

Figure 21. Write timing diagram

12.2. Write Timing Diagram

There are a few other considerations for writing over SPI:

- The R/W bit must be set to 0.
- The data on the SDI pin is written into the shift register on every rising edge of SCK.
- CS must be held low to write data. If CS is held high, the device will ignore the clock.
- When sharing SCK and SDI lines between devices, keep the CS line high on the idle device

Read Timing

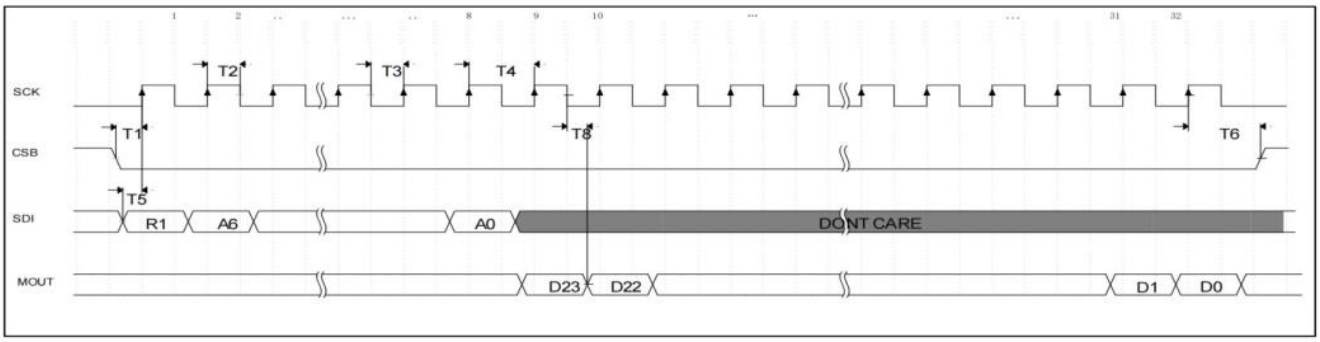

Figure 22

There are a couple of other considerations for reading back over SPI:

- The R/W bit must be set to 1.
- Data on MOUT is transferred on the falling edge of SCK.
- When reading back, the data portion of SDI is always ignored

Timing Parameters

Table 6

PARAMETER	DESCRIBE	MIN	MAX	UNIT
T1	CS falling edge to SCK setup time	10		ns
T2	SCK high level duration		10	ns
T3	SCK low level duration		10	ns
T4	SCK frequency		50	MHz
T5	Data creation time	8		ns
T6	SCS rising edge to CS falling edge	15		ns
T7	Data retention time	3		ns
T8	SCS rising edge readback data setup time	2		ns

XIII. Register

Table 7

CLASSIFICATION TABLE	ADDRESS ADDR-HEX	NAME	FUNCTION NAME FUNCTION	BIT NUMBER	READ AND WRITE R/W	DESCRIBE DESCRIPTION
Global Shutdown Control Register	0	PD_ALL	Global shutdown control	0	RW	0: Global normal operation 1: Global shutdown
		PD_REF	Switch reference channel	1	RW	1: Force shut down the reference channel

CLASSIFICATION TABLE	ADDRESS ADDR-HEX	NAME	FUNCTION NAME FUNCTION	BIT NUMBER	READ AND WRITE R/W	DESCRIBE DESCRIPTION
		PD_RF	Switching feedback frequency division	2	RW	1: Forced shutdown of feedback divider
		PD_PFD	Switching Phase Frequency Detector (PFD)	3	RW	1: Forced shutdown of PFD
		PD_CP	Switching charge pump CP	4	RW	1: Force the charge pump to shut down
		PD_BIAS	Switching charge pump bias current	5	RW	1: Forced shutdown of charge pump bias current
		PD_LD	Switch lock detection	6	RW	1: Forced shutdown lock detection
		PD_VCO	Switching VCO	7	RW	1: Force shut down VCO
		PD_CHA	Switch A channel divider	8	RW	1: Force shut down the A channel divider
		PD_OUTA	Switch A channel output buffer	9	RW	1: Force shut down the A channel output buffer
		PD_CHB	Switch B channel crossover	10	RW	1: Force shut down the B channel divider
		PD_OUTA	Switch B channel output buffer	11	RW	1: Force shut down the B channel output buffer
		BLK_UVL0	Shield UVLO signal	12	RW	0: Disable the undervoltage lockout function during power-on reset 1: Enable undervoltage lockout
		RESET	Reset register	13	RW	Reset all state machines and registers to default values 0: Normal operation 1: Reset
		VCO_PHASE_SYNC	SYNC mode switch	14	RW	0: Disable SYNC mode 1: Enable SYNC mode
		GPO	Global parallel port output	19:16	RW	LD_GPO_OUT pin output: 0000: NC not connected 0001: Reference frequency division REF_DIV 0010: Feedback frequency division RF_DIV 0011: Charge pump UP 0100: Charge pump DN 0101: Read back registers 00-08(H) 0110: Read back register 16-42 (H) 0111: Undervoltage lockout VUVLO 1000-1111: NC not connected

CLASSIFICATION TABLE	ADDRESS ADDR-HEX	NAME	FUNCTION NAME FUNCTION	BIT NUMBER	READ AND WRITE R/W	DESCRIBE DESCRIPTION
		GPO_EN	Switch GPO	23	RW	0: Turn off GPO and use LD mode 1: Turn off LD and use GPO mode
Reference divider register	1	rdiv	Reference division ratio	13:0	RW	Frequency division ratio 1-16383 (2^14-1)
		Reserved	Reserved bits	14	RW	Reserved bits
		RST_REF	Reset reference divider	15	RW	Reset reference divider, high active
		en_ref2div	Reference signal to digital enable	16	RW	Reference signal to digital enable, high effective
		multiplier	Frequency Multiplier	18:17	RW	00: Frequency multiplier off 01: 2- time multiplier on 11: 4-time frequency multiplier on
		AFCCLK	AFC clock selection	20:19	RW	00: Reference clock 01: Reference clock divided by 2 10: Reference clock divided by 4 11: Reference clock divided by 8
		AFCCLK_RST	AFC clock reset	21	RW	0: Normal operation 1: Reset
		REF2SYNC_RST	Reference to SYNC clock reset	22	RW	0: Normal operation 1: Reset
Integer divider register	2	intg	Feedback division ratio	18:0	RW	Integer mode: division ratio 20~32767 (2^15-1)
		ndiv_mux	VCO frequency sweep division ratio	19	RW	Select the VCO division ratio
		pd_rst_div	Reset feedback divider	21	RW	Reset feedback frequency division, high effective
		Ndiv BIAS	N -Fractional Current Regulation	23:22	RW	000: Minimum current 001: Current +5% 010: Current +10%
Fractional Divider Register A	3	frac	Fractional frequency ratio	23:0	RW	Set the fractional division ratio NUM[23:0]
Fractional frequency control	4	n_reset_dsm	Reset fractional frequency	0	RW	Initial reset signal, low valid,
		dsm_en	Switching fractional frequency	1	RW	0: Disable fractional division 1: Enable fractional division
		int_en	Toggle integer mode	5	RW	0: Decimal mode 1: Integer mode (fractional division disabled)
		sel	DSM mode selection	8:6		DSM noise transfer function configuration, default 001 001:z^{-1}

CLASSIFICATION TABLE	ADDRESS ADDR-HEX	NAME	FUNCTION NAME FUNCTION	BIT NUMBER	READ AND WRITE R/W	DESCRIBE DESCRIPTION
						010:$z^{-1}+z^{-2}$ (no wandering spurs) 100:z -1 +2z -2 - 2z -3
		NDiv_CIk_to_dig_en	Feedback frequency division to digital clock enable	9	RW	0: Disable 1: Enable
		NDiv_CIk_phase	Feedback frequency division to digital clock phase control	10	RW	0: In phase 1: In phase
		Ndiv_CIk_delay	Feedback frequency division to digital clock delay control	12:11	RW	00: Delay 1 10: Delay 2 11: Delay 3
Lock detection	6	Reserved bits	Reserved bits	2:0		
		Reserved bits	Reserved bits	4:3	RW	
		LD_MODE	LD working mode	5	RW	LD working mode: 0: Disable digital LD mode 1: Turn on the simulated LD mode
		LD_DCC	Analog LD duty cycle determination range	10:8	RW	LD duty cycle determination range: 000: 10% 001: 15% 010: 20% 011: 25% 100: 30% 101: 35% 110: 40% 111: 45%
Phase frequency detector and charge pump registers A	7	PD_tdelay	Set the PFD reset delay	1:0	RW	PFD reset delay: 00: 0.6ns 01: 1ns 10: 1.4ns 11: 1.8ns
		POL_INV	Setting the PFD Polarity	2	RW	PFD polarity control: 0: Positive polarity 1: Polarity reversed
		FUP_CP	Force the UP output of the PFD to be enabled	5	RW	Only valid when PFD is off 0: Forced shutdown of PFD UP output 1: Force enable the UP output of PFD
		FDN_CP	Force enable DN output of PFD	6	RW	Only valid when PFD is off 0: Forced shut down of the DN output of the PFD 1: Force enable DN output of PFD
		CPGup	CP gain current UP control word	15:8	RW	CP gain current UP control word (30uA/bit): Current calculation: 30uA*CPGup CPGup range: 0-255

CLASSIFICATION TABLE	ADDRESS ADDR-HEX	NAME	FUNCTION NAME FUNCTION	BIT NUMBER	READ AND WRITE R/W	DESCRIBE DESCRIPTION
		CPGdn	CP gain current DN control word	23:16	RW	CP gain current DN control word (30uA/bit): Current calculation: 30uA*CPGdn CPGdn range: 0-255
Phase frequency detector and charge pump registers B	8	CPOS_current	CP compensation current control word	6:0	RW	CP compensation current DN control word (12uA/bit): Current calculation: 12uA*CPGdn CPOS_current range: 0-127
		CP0S_UP_EN	UP compensation current of switch CP	8	RW	0: Enable UP compensation current of CP 1: Disable UP compensation current of CP
		CP0S_DN_EN	DN compensation current of switch CP	9	RW	0: Enable DN compensation current of CP 1: Disable DN compensation current of CP
		Reseved	Reserved bits	14:10	RW	Reserved bits
		INPIN_IGNORE	Shield external SYNC signal	15	RW	000: Minimum current 001: Current +5% 010: Current +10%
		INPIN_HYST	High hysteresis enabled in LVDS mode	16	RW	0: Disable 1: Enable
		INPIN_LVL	Bias setting in LVDS mode	18:17	RW	00: Vin/4 01: Vin 10: Vin/2 11: Invalid
		INPIN_FMT	SYNC input signal mode control	20:19	RW	01: SYNC = CMOS 10: SYNC = LVDS,
VCO Control Register	16	VT_monitor	VT monitoring range control	13:12	RW	00: 0.4-2.9 01: 0.5-2.8 10: 0.6-2.7 11: 0.7-2.6
		VTTC_EN	VCO segment select temperature compensation enable	14	RW	0: Off 1: On
		vco1rbc	vco1dc adjustment control	15	RW	Default 0
		vco2rbc	vco2dc adjustment control	16	RW	Default 0
		vco3rbc	vco3dc adjustment control	17	RW	Default 0
		div	Frequency division ratio	20:19	RW	00:1 frequency division 01:2 frequency division 10:4 frequency division 11:8 frequency division
		ibct	Bias control of 3 -to -1 circuit	23:21	RW	Bias control of 3 -to -1 circuit
VCO algorithm control register	17	n_reset_bsa	Reset AFC (Bisection Algorithm)	1	RW	Initial reset signal, low valid

CLASSIFICATION TABLE	ADDRESS ADDR-HEX	NAME	FUNCTION NAME FUNCTION	BIT NUMBER	READ AND WRITE R/W	DESCRIBE DESCRIPTION
		autogapcal_en	Switch continuous calibration	1	RW	0: Disable continuous calibration 1: Enable continuous calibration
		autodetcal_en	Switch lock detection function	1	RW	0: Disable the lock detection function 1: Enable the lock detection function
		instlock_en	Real-time function of switch lock detection	1	RW	0: Disable the real-time lock detection function. Wait for a period of time (callock_tmr) before detecting the lock again. 1: Enable the real-time detection function for loss of lock
		fc_bsa_en	Dichotomy Enable	4		
Binary register A	18	calstart_tmr	Waiting time to start calibration	15:0	RW	Waiting time = tref * calstart_tmr
Binary register B	19	calcomp_tmr	Comparison process waiting time	15:0	RW	Waiting time = tref * calcomp_tmr
Binary register C	1b	callock_tmr	Waiting time for the locking process	15:0	RW	Waiting time = tref * callock_tmr
Binary register D	1c	refcnt_num	Phase detection cycle comparison count value	13:0	RW	Number of phase detection cycles for each comparison
Binary register E	1d	refdet_num	Phase detection clock loss detection count value	11:0	RW	The number of cycles counted when the phase detection clock is lost
External Control Registers	1e	seginit_en	Switch initial segment number setting	1	RW	0: Disable the setting of the initial segment number and set the initial segment number internally
		seg_init	Initial segment number setting	6:1	RW	only when seginit_en=1, sets the initial segment number
		segext_en	Switch external output segment number setting	7	RW	0: Disable the setting of external output segment number or VCO, and generate the output segment number by binary division 1: Enable the setting of external output segment number or vco, external setting is seg_ext or vco_ext (When cutvco_en=1)
		seg_ext	External output fixed segment number setting	13:8	RW	only when segext_en=1, sets the fixed segment number of external output
		vco_ext	External output fixed VCO number setting	16:14	RW	only when segext_en=1, set the fixed VCO number of external output

CLASSIFICATION TABLE	ADDRESS ADDR-HEX	NAME	FUNCTION NAME FUNCTION	BIT NUMBER	READ AND WRITE R/W	DESCRIBE DESCRIPTION
		ld_temp_mux	Detect LD or temperature MUX	20	RW	0: Detect LD 1: Detect temp
VCO Adaptation Registers	1f	adapt_factor	Adaptation adjustment factor	2:0	RW	Adjust the error accuracy of the adaptive vco delay time, recommended = 4
		adapt_mux	Adaptive adjustment strobe	4:3	RW	Adjust the gate to adapt to the vco delay time, recommended = 2
		cutvco_en	Switch selects VCO first and then segment function	5	RW	0: Disable the function of selecting vco first and then selecting segment, seg_out outputs all segments 0 to 63 1: Enable the function of selecting vco first and then segment, sub_vco Output is high frequency vco1=001, intermediate frequency vco2=010, Low frequency vco3=100 ; sub_seg output is High frequency vco1=0~15, medium frequency vco2=0~15, low frequency Frequency vco3=0~31
		cutvcocnt_errmtp	Error precision control under the function of selecting VCO first and then segment	8:6	RW	only when cutvco_en=1, controls error accuracy, recommended =0
Comparator select control register	20	compnumext_en	External setting of switch comparison times	1	RW	0: Disable external setting of comparison times and set initial segment number internally 1: Enable external setting of comparison times, external setting is segcompnum_ext or
		segcompnum_ext	Externally set segment selection comparison times	4:1	RW	Externally set segment selection comparison times
		vcocompnum_ext	Externally set VCO comparison times	8:5	RW	Externally set VCO comparison times
AFC Status Register	42	VCO_SEL	VCO Information	2:0	RO	3'b001:HIGH CORE 3'b010:MID CORE 3'b100:LOW CORE
		SEG_SEL	Excerpt information	8:4	RO	Reread selected segment information
		AFC_DONE	AFC complete logo	12	RO	1: AFC completed 0: AFC working

IV. Pin Definition

Table 8

PAD NUMBER	NAME	I/O	DESCRIBE
1	CE	I	Digital I/O chip select port, chip enable input, high level 3.3V activates the chip
2, 4, 6, 13, 14, 25, 31, 34, 39, 40	GND		land
3, 5, 10, 18, 19, 22, 27, 29, 30, 32, 33, 36, 38	NC		Dangling
7	VCCDIG	P	Reference and digital circuit, 3.3V power supply
8	OSCINP	I	Reference signal input terminal P requires an external DC blocking capacitor
9	OSCINM	I	Reference signal input terminal M requires an external DC blocking capacitor
11	VCCCP	P	Charge pump, phase detector power supply, 3.3V power supply
12	CPOUT	O	Charge pump output
15	VCCMASH	P	N divider power supply, 3.3V power supply
16	SCK	I	SPI clock input, supports 3.3V CMOS logic level
17	SDI	I	SPI data input, supports 3.3V CMOS logic level
20	MUXOUT	O	Multiplexed signal output - lock detection, readback data, etc.
21	VCCBUF	P	Output channel power supply, 3.3V power supply
23	OUT	O	For RF output, a DC blocking capacitor is required on the output path.
24	CSB	I	SPI input enable signal, supports 3.3V CMOS logic level
26	VCC VCO	P	VCO power supply, 3.3V power supply, pay attention to add magnetic beads to isolate it from other power supplies, add capacitors and other filtering
28	MUTE/NC	I	A high level will silence the output port. This port has an internal pull-down function. If you need to connect it to the LMX2594 PIN TO PIN, this pin can be left floating.
35	VTUNE	I	VCO frequency tuning control port
37	VCC VCO	P	VCO power supply, 3.3V power supply, pay attention to add magnetic beads to isolate it from other power supplies, add capacitors and other filtering
DAP	GND		land

XIV. Appearance Assembly Drawing

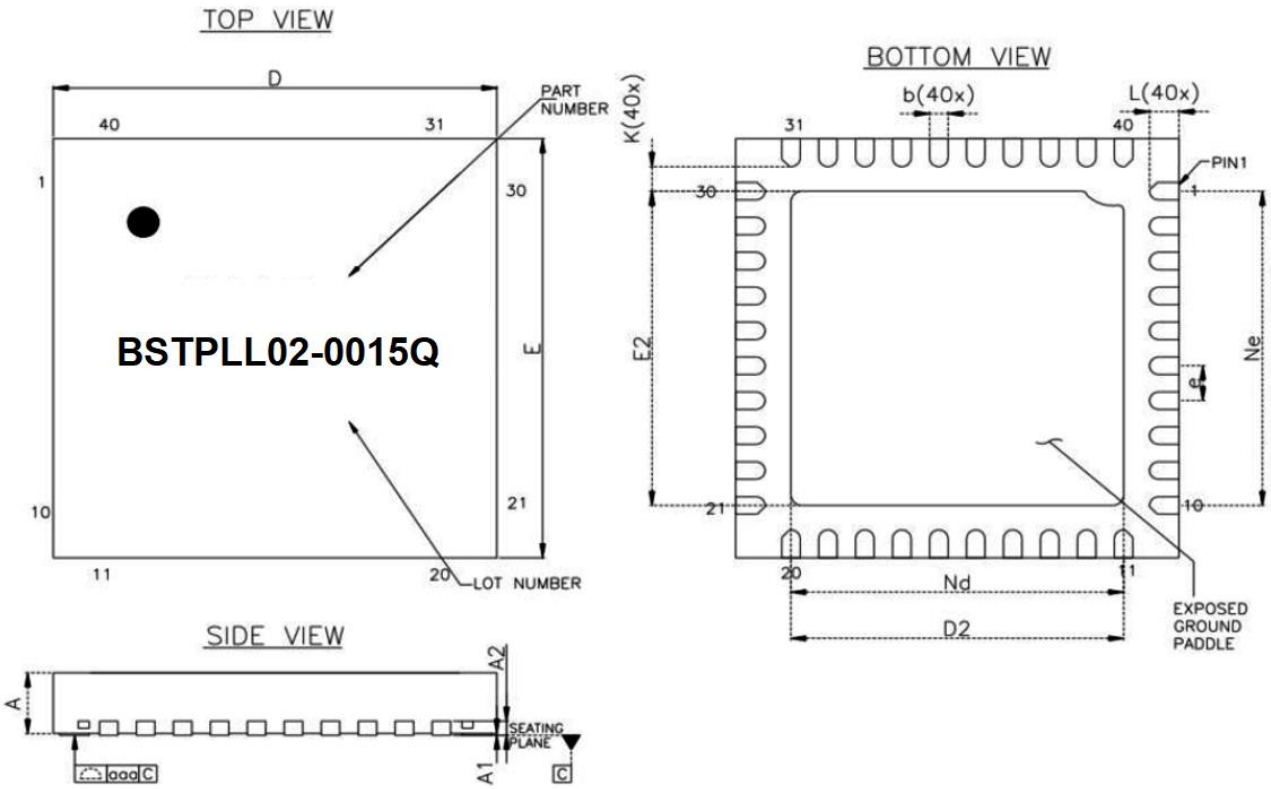

Figure 23

Table 9

SP6	DIMENSION TABLE•(UNIT:MM):		
SYMBOL	MIN	NOM	MAX •
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.20Ref :	
b	0.20 I 0.25		0.30
D	5.90	6.00	6.10
D2	4.40	4.50	4.60
e	0.50BSC		
Ne	4.50BSC		
Nd	4.50BSC		
E	5.90	6.00	6.10
E2	4.40	4.50	4.60
K	0.20	—	—
L	0.30	0.40	0.50
aaa		0.08	

XV. Evaluation Board Circuit (EVAL-BSTPLL02-0015Q-B)

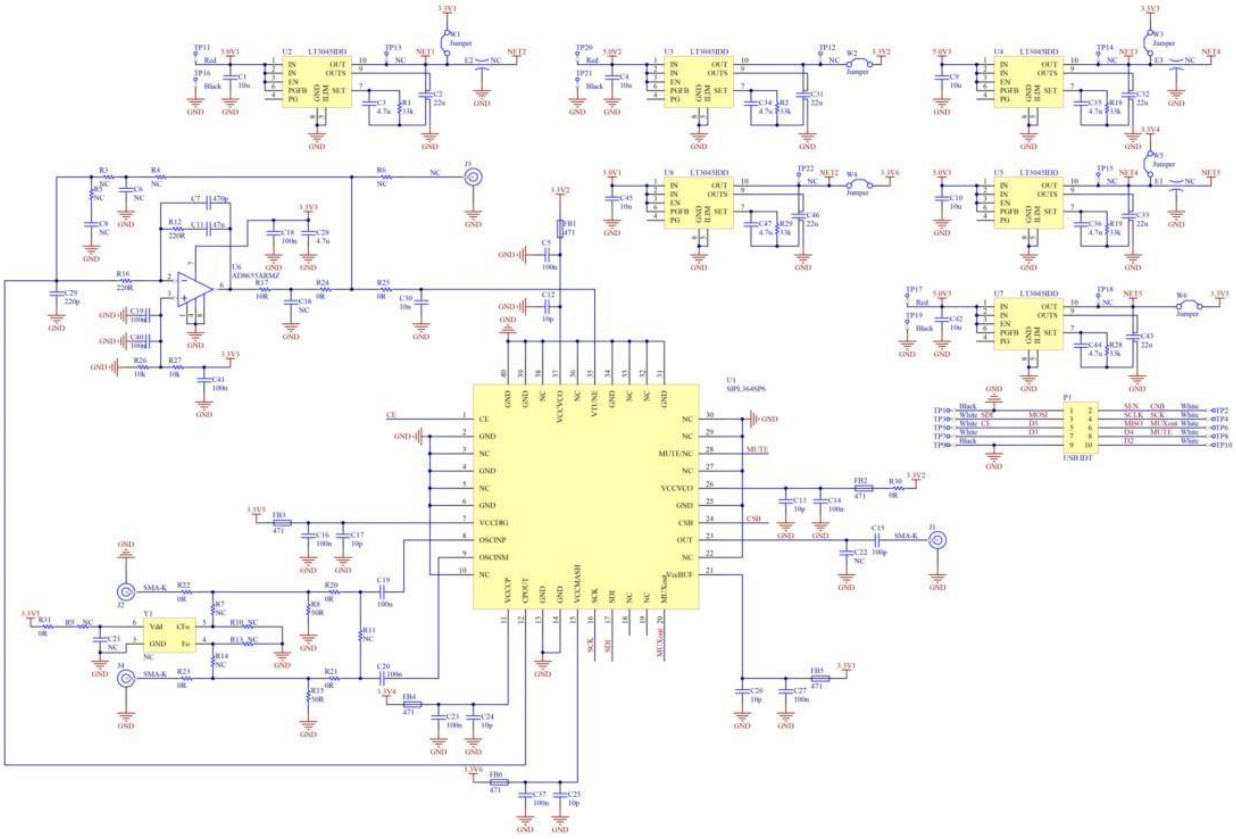

Figure 24

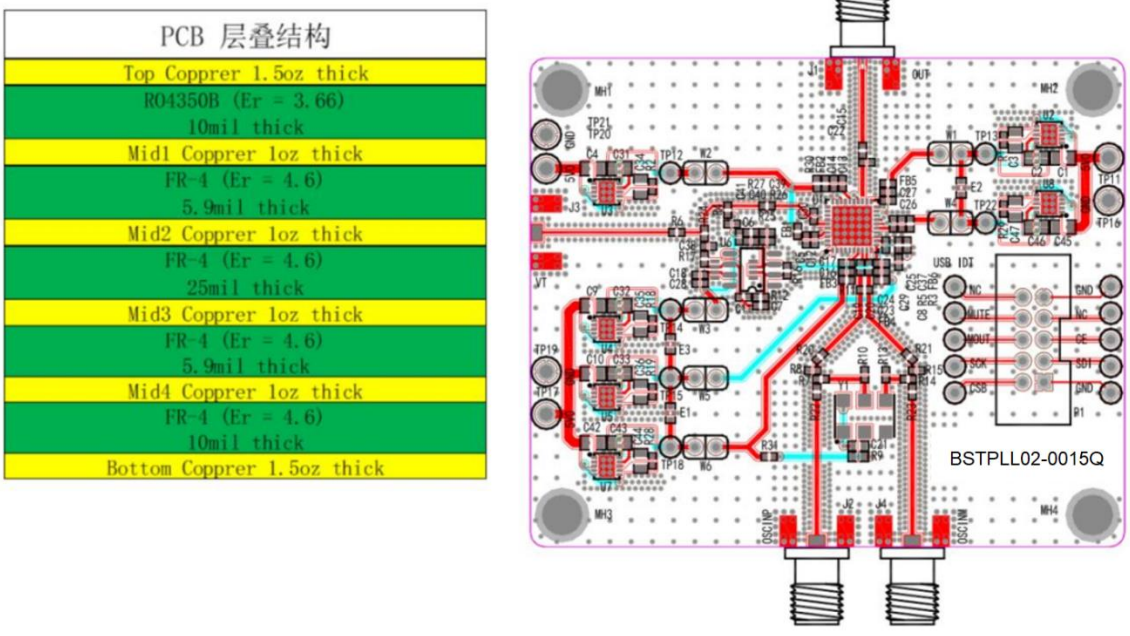

Figure 25

XVI. Evaluation Board Circuit (EVAL-BSTPLL02-0015Q-B)

Table 10

#	DESIGNATOR	COMMENT	DESCRIPTION	FOOTPRINT	MANUFACTURER	PART NUMBER	SOB	QUANTITY
1	PCB1	PCB	Printed Circuit Board		-	-	Y	1
2	C1,C4,C9,C10, C42,C45	10u	Capacitor	0805	Murata	GRM21BZ71E106KE15L	Y	6
3	C2,C31,C32,C33, C43,C46	22u	Capacitor	0805_4	Murata	GRM21BZ71A226ME15L	Y	6
4	C3,C34,C35,C36, C44,C47	4.7u	Capacitor	0805	Murata	GRM21BZ71E475KE15L	Y	6
5	C5,C14,C16,C18, C19,C20,C23,C27,C39 ,C40,C41	100n	Capacitor	0402	Murata	GRM155R71H104KE14D	N	12
6	C6	NC	Capacitor	0402	Murata	GRM155R71H104KE14D	Y	1
7	C7	470p	Capacitor	0402	Murata	GRM1555C1H471JA01D	Y	1
8	C8	NC	Capacitor	0402	Murata	GRM155R71E473JA88D	Y	1
9	C11	47n	Capacitor	0402	Murata	GRM155R71E473JA88D	Y	1
10	C12,C13,C17,C24 C25,C26	10p	Capacitor	0402	Murata	GRM1555C1H100FA01D	Y	6
11	C15	100p	Capacitor	0402	Murata	GRM1555C1H101FA01D	Y	1
12	C21	NC	Capacitor	0603	Murata	GRM155C80J106ME11D	N	1
13	C22	NC	Capacitor	0402	Murata	GRM155R71H103JA88D	N	1
14	C28	4.7u	Capacitor	0402	Murata	GRM155R61E475ME15D	Y	1
15	C29	220p	Capacitor	0402	Murata	GRM1555C1H221JA01D	Y	1
16	C30	10n	Capacitor	0402	Murata	GRM155R71H103JA88D	Y	1
17	C38	NC	Capacitor	0402	Murata	GRM1555C1H222GA01D	N	1
18	E1,E2,E3	NC	EMI Filter	NFM18C	Murata	NFM18CC223R1C3	N	3
19	FB1,DB2,FB3,FB5, FB6	471	470R	0402	Murata	BLM15BD471SH1	N	6

#	DESIGNATOR	COMMENT	DESCRIPTION	FOOTPRINT	MANUFACTURER	PART NUMBER	SOB	QUANTITY
20	J1,J2,J4	SMA-K	RF Connector	SMA 40G,SMA DC	Aowen	D550B12E01-023	Y	3
21	J3	NC	RF Connector	SMA DC	Aowen	D550B12E01-023	Y	1
22	MH1, MH2. MH3. MH4	702932000		702932000	WE	702932000	Y	4
23	P1	USB IDT	Header, 5-Pin, Dual row, Right Angle	IDC2.54-10		DC3-10P	Y	1
24	R1,R2, R18, R19, R28, R29	33k	Resistor	0402	Yageo	RCO402FR-0733KL	Y	6
25	R3	NC	Resistor	0402	Yageo	RCO402FR-07750RL	N	1
26	R4,R6	NC	Resistor	0402	Yageo	RCO402JR-070RL	N	2
27	R5	NC	Resistor	0402	Yageo	RCO402FR-07300RL	N	1
28	R7,R14	NC	Resistor	0402	Murata	GRM155R71C104KA88D	N	2
29	R8,R15	50R	Resistor	0402	Yageo	RCO402JR-0750RL	N	2
30	R9	NC	Resistor	0603	Yageo	RCO603JR-074R7L	Y	1
31	R10,R13	NC	Resistor	0402	Yageo	RCO402JR-07150RL	Y	2
32	R11	NC	Resistor	0402	Yageo	RCO402FR-07100RL	Y	1
33	R12,R16	220R	Resistor	0402	Yageo	RCO402FR-07220RL	Y	2
34	R17	10R	Resistor	0402	Yageo	RCO402JR-0710RL	Y	1
35	R20, R21, R22.R23,R24.R25.	0R	Resistor	0402	Yageo	RCO402JR-070RL	Y	8
36	R26,27	10k	Resistor	0402	Yageo	RCO402FR-0710KL	Y	2
37	TP1. TP9	Black	Test Point	Keystone5001	Keystone	Keystone5001	Y	2
38	TP2,TP3,TP4,TP5, TP6, TP7, TP8,TP10	White	Test Point	Keystone5002	Keystone	Keystone5002	Y	8
39	TP11,TP17,TP20	Red	Test Point	Keystone5005	Keystone	Keystone5005	Y	3
40	TP12.TP13, TP14.	NC	Test Point	Keystone5002	Keystone	Keystone5002	N	6

#	DESIGNATOR	COMMENT	DESCRIPTION	FOOTPRINT	MANUFACTURER	PART NUMBER	SOB	QUANTITY
	TP15.TP18.TP22							
41	TP16.TP19.TP21	Black	Test Point	Keystone5006	Keystone	Keystone5006	Y	3
42	U1	BSTPLL02-0015Q	PLL	SP6	YIFENG	BSTPLL02-0015Q	Y	1
43	U2. U3. U4. U5, U7, U8	LT3045IDD	LDO	DFN10	ADI	LT3045IDD	Y	6
44	U6	AD8655ARMZ	Operational Amplifier	SOP8-1	ADI	AD8655ARMZ	Y	1
45	W1, W2, W3, W4, W5, W6	Jumper	Jumper Wire	Jumper			Y	6
46	Y1	NC		X0-7.0X5.0	EPSON	BSTPLL02-0015Q	Y	1

XVI. Packaging Information

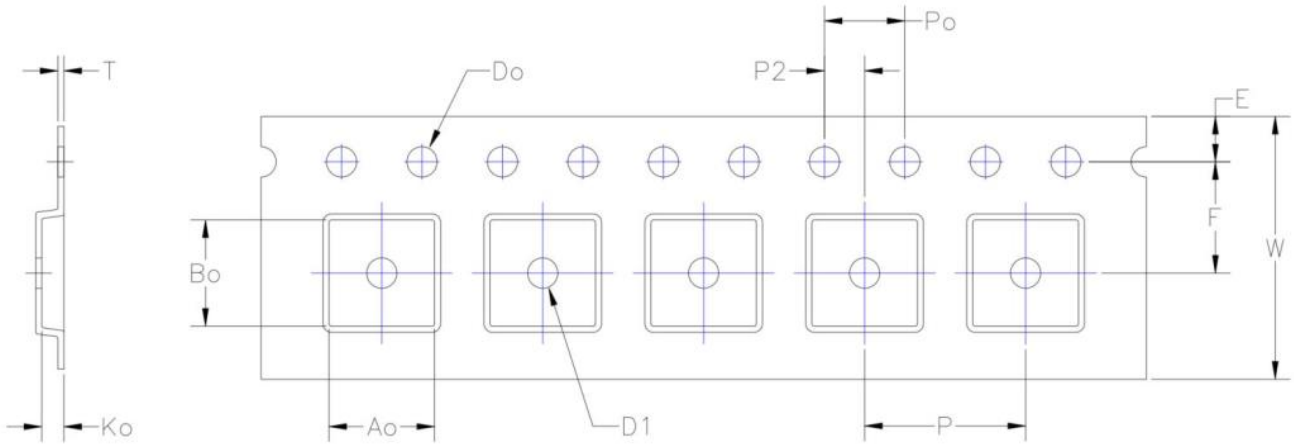

Figure 26

Table 11

DIMENSION	SPEC
W	16.00 +/-0.30
Do	Ø1.50 +0.10/-0.00
Po	4.00 +/-0.10
E	2.25 +/-0.10
D1	Ø 1.50 MIN
Ao	6.30 +/-0.10
Bo	6.30 +/-0.10

DIMENSION	SPEC
P	12.00 +/-0.10
P2	2.00 +/-0.10
Ko	1.10 +/-0.10
T	0.30 +/-0.05
F	5.50 +/-0.05

Illustrate:

- Unit: mm
- Material: Anti-static polypropylene
- Color: black
- 10 positioning hole center distance (PO) cumulative tolerance ±0.2

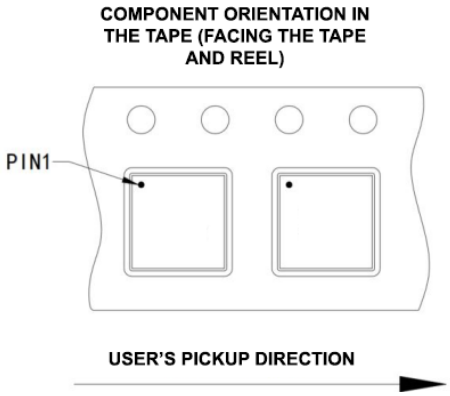

Figure 27

XVII. Precautions

- Do not attempt to clean the chip surface using wet chemical methods.
- This product is an electrostatic sensitive device. Please pay attention to anti-static during storage and use.
- Store in a dry, nitrogen environment.

Figure 28