BSTP10K50 Programmable Logic Array Circuit Military Product Manual

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Product description

Product description

The BSTP10K50Q240-4type programmable logic array circuit is a high-density programmable logic array circuit based on SRAM configuration. The circuit consists of two parts: control circuit and configurable resources. The control circuit includes JTAG circuit, configuration control circuit, word line, bit line, and configuration data storage unit (SRAM). The configurable resources include configurable logic array block (LAB), configurable embedded storage array block (EAB), and configurable input and output unit (IOE). The configurable resources are interconnected through configurable row and column wiring distributed among them.

The circuit standard configurable gate count (logic and storage) is 50 000, and the maximum system gate count is 116 000. The configurable resources include 360 logic array blocks (LABs), 2880 logic elements (LEs), and 20480 bits of embedded storage array blocks (EABs), supporting four configuration modes: JTAG, passive serial, synchronous, and asynchronous passive parallel.

Product features

- This circuit is fully pin and functionally compatible with the EPF10K50RC240-4 circuit.
- Supports programmable system-on-chip architecture.
- Embedded arrays support large functional logic, such as specialty memories and specialized logic functions.
- Logic arrays support general combinational logic functions.
- high density
- 50 000 typical gate count.
- Up to 20K RAM capacity, each embedded logic block (EAB) size is 2048 bits, the use of all EABs does not reduce the logic capacity.
- System Level Features
- Multi-level I/O interface.
- 3.3V/5V level input pin.
- Low power consumption design.

- Built-in JTAG boundary scan test circuit structure, according to IEEE standard 1149.1-1990, does not affect any device logic when used.
- Flexible internal wiring
- Distributed carry chains implement arithmetic logic functions such as adders, counters, and comparators (automatically called by software tools and large functions).
- Distributed cascade chains complete high-speed, high fan-in logic functions (automatically called by software tools and large functions).
- Two global clock signals.
- Complete I/O pins
- Each pin has independent three-state output enable control.
- Each I/O pin can be selected as open-drain.
- Programmable output slew rate control to reduce switching noise.

Product use and application range

The internal structure of the BSTP10K50 circuit enables the circuit to realize complex logic functions (digital logic replacement below 50,000 gates).

Implement digital processors, microcontrollers, decoders, counters, small-scale memories, multiplexers, data transmission converters

Exchange and some simple algorithm logic.

Corresponding to the situation of replacing foreign products

It corresponds to the EPF10K50 circuit of the foreign Altera company. The two have the same functions, but are slightly inferior to foreign products in speed. The package is pluggable and replaceable (the shell size is slightly larger than that of foreign products), and the reliability has been improved to military grade.

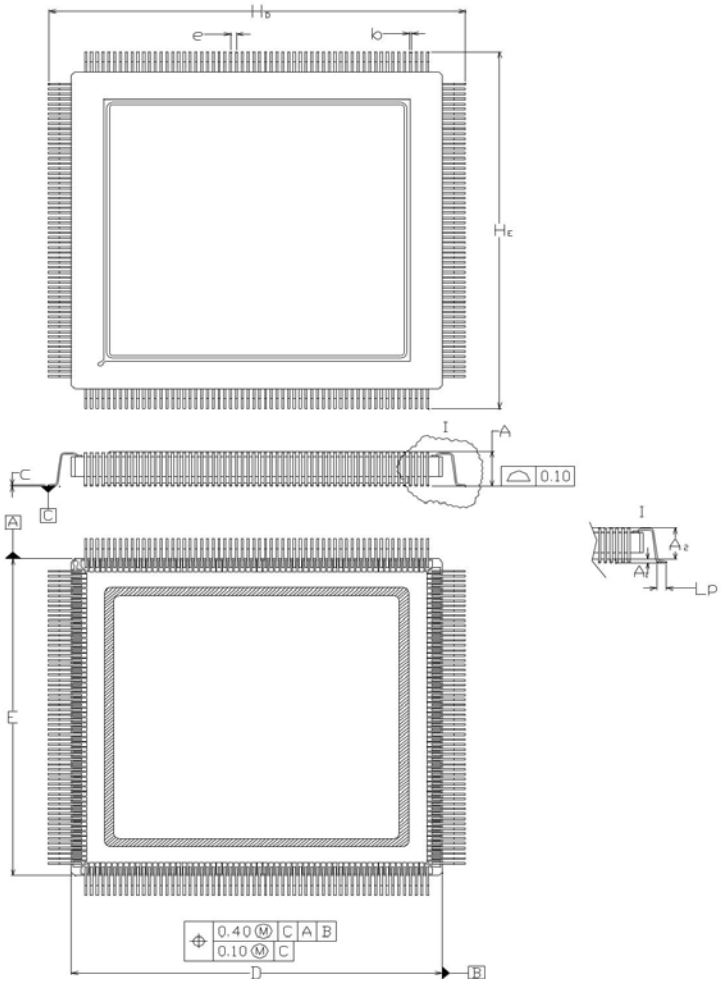
Product dimensions/Real photos

The circuit uses a 240-lead ceramic quad flat package (CQFP240). The specific dimensions are shown in Table 1.

Table 1.

Unit: mm

Size code	size		
	Minimum		Minimum
A	—	*A*	—
*A*1	0.20	*A*1	0.20
*A*2	—	*A*2	—
b	—	*b*	—
c	0.10	*c*	0.10



Standard Implementation

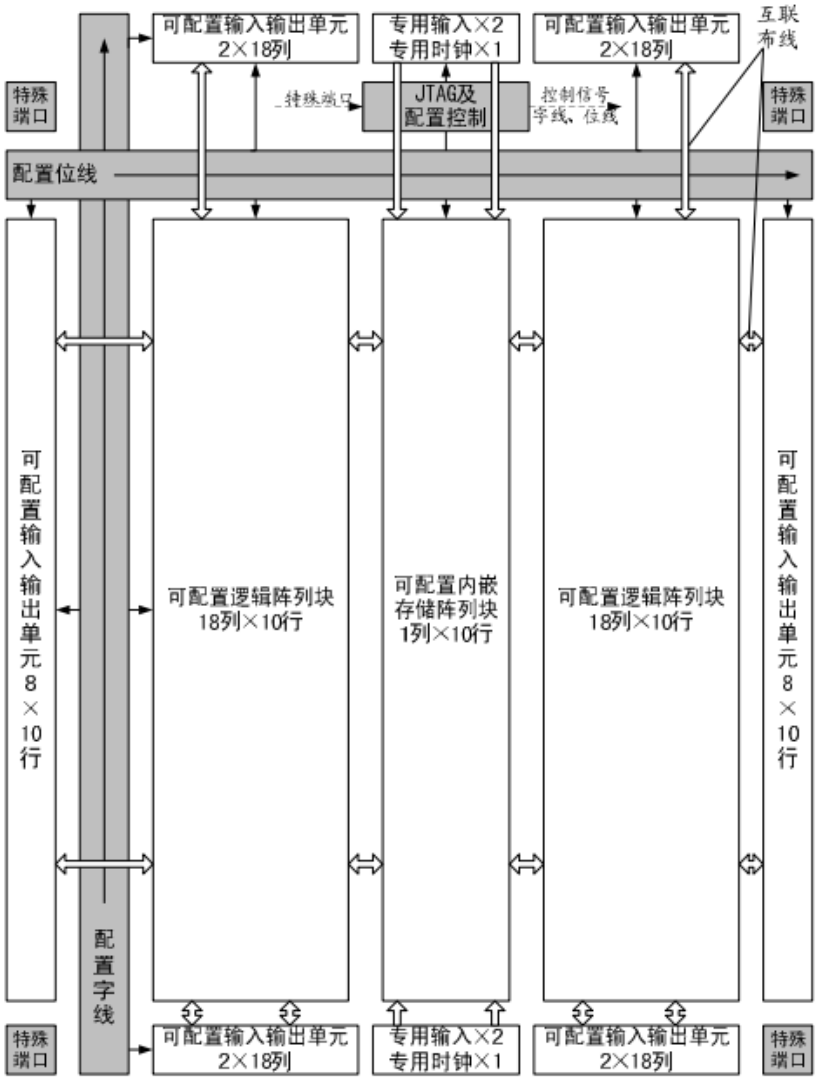
The product quality grade is B, and the assessment standard complies with Q/FC 30020-2009 "BSTP10K50 Circuit Detailed Specification"

Requirements and meet GJB597 "General Specification for Semiconductor Integrated Circuits" and GJB548B-2005 "Test Methods and Procedures for Microelectronic Devices"

The requirements of the Preface.

Brief description of basic working principle

Circuit Function Block Diagram



Package and Pin Description

The circuit is packaged with the cover facing downwards and the heat sink on the front. The bottom picture shows the circuit with the front side (where the heat sink is) facing upwards.

BSTP10K50Q240-4circuit pin arrangement diagram

Among the 240 pins of the circuit, there are 189 user-configurable IO ports (167 user-configurable IO ports, 2 user-configurable dedicated clock input ports, 4 user-configurable dedicated input ports, 16 configuration/user IO dual-purpose ports), 5 JTAG dedicated ports, 9 dedicated configuration ports, 19 power ports, and 18 ground ports. See Table 3-Table 7 for pin definitions.

Table 3. BSTP10K50Q240-4Circuit pin definition

Serial number	Pin Symbols	I/O/Z	Function	Serial number	Pin Symbols	I/O/Z	Function
1	TCK	I	JTAG Port	39	IO	IO	User Port
2	CONF_DONE	IO	Configuring Ports	40	IO	IO	User Port

3	CEO	O	Configuring Ports	41	IO	IO	User Port
4	TDO	O	JTAG Port	42	GND	I	power supply
5	VCC	I	power supply	43	IO	IO	User Port

	IO	IO	User Port	44	IO	IO	User Port
7	IO	IO	User Port	45	IO	IO	User Port
8	IO	IO	User Port	46	IO	IO	User Port
9	IO	IO	User Port	47	VCC	I	power supply
10	GND	I	power supply	48	IO	IO	User Port
11	CLKUSR/IO	I/IO	Configuration/user dual use	49	IO	IO	User Port
12	IO	IO	User Port	50	IO	IO	User Port
13	IO	IO	User Port	51	IO	IO	User Port
14	IO	IO	User Port	52	GND	I	power supply
15	IO	IO	User Port	53	IO	IO	User Port
16	VCC	I	power supply	54	IO	IO	User Port
17	IO	IO	User Port	55	IO	IO	User Port
18	IO	IO	User Port	56	IO	IO	User Port
19	IO	IO	User Port	57	VCC	I	power supply
20	IO	IO	User Port	58	TMS	I	JTAG Port
twenty one	IO	IO	User Port	59	TRST	I	JTAG Port
twenty two	GND	I	power supply	60	STATUS	IO	Configuring Ports
twenty three	RDYnBSY/IO	O/IO	Configuration/user dual use	61	IO	IO	User Port
twenty four	IO	IO	User Port	62	IO	IO	User Port
25	IO	IO	User Port	63	IO	IO	User Port
26	INIT_DONE/IO	O/IO	Configuration/user dual use	64	IO	IO	User Port
27	VCC	I	power supply	65	IO	IO	User Port
28	IO	IO	User Port	66	IO	IO	User Port
29	IO	IO	User Port	67	IO	IO	User Port
30	IO	IO	User Port	68	IO	IO	User Port
31	IO	IO	User Port	69	GND	I	power supply
32	GND	I	power supply	70	IO	IO	User Port
33	IO	IO	User Port	71	IO	IO	User Port
34	IO	IO	User Port	72	IO	IO	User Port
35	IO	IO	User Port	73	IO	IO	User Port
36	IO	IO	User Port	74	IO	IO	User Port
37	VCC	I	power supply	75	IO	IO	User Port
38	IO	IO	User Port	76	IO	IO	User Port
Serial number	Pin Symbols	I/O/Z	Function	Serial number	Pin Symbols	I/O/Z	Function
77	VCC	I	power supply	118	IO	IO	User Port
78	IO	IO	User Port	119	IO	IO	User Port
79	IO	IO	User Port	120	IO	IO	User Port
80	IO	IO	User Port	121	nCONFIG	I	Configuring Ports

81	IO	IO	User Port	122	VCC	I	power supply
82	IO	IO	User Port	123	MSEL1	I	Configuring Ports
83	IO	IO	User Port	124	MSEL0	I	Configuring Ports
84	IO	IO	User Port	125	GND	I	power supply
85	GND	I	power supply	126	IO	IO	User Port
86	IO	IO	User Port	127	IO	IO	User Port
87	IO	IO	User Port	128	IO	IO	User Port
88	IO	IO	User Port	129	IO	IO	User Port
89	VCC	I	power supply	130	VCC	I	power supply
90	DI	I	Dedicated input	131	IO	IO	User Port
91	GCLK	I	Dedicated clock input	132	IO	IO	User Port
92	DI	I	Dedicated input	133	IO	IO	User Port
93	GND	I	power supply	134	IO	IO	User Port
94	IO	IO	User Port	135	GND	I	power supply
95	IO	IO	User Port	136	IO	IO	User Port
96	VCC	I	power supply	137	IO	IO	User Port
97	IO	IO	User Port	138	IO	IO	User Port
98	IO	IO	User Port	139	IO	IO	User Port
99	IO	IO	User Port	140	VCC	I	power supply
100	IO	IO	User Port	141	IO	IO	User Port
101	IO	IO	User Port	142	IO	IO	User Port
102	IO	IO	User Port	143	IO	IO	User Port
103	IO	IO	User Port	144	IO	IO	User Port
104	GND	I	power supply	145	GND	I	power supply
105	IO	IO	User Port	146	IO	IO	User Port
106	IO	IO	User Port	147	IO	IO	User Port
107	IO	IO	User Port	148	IO	IO	User Port
108	IO	IO	User Port	149	IO	IO	User Port
109	IO	IO	User Port	150	VCC	I	power supply
110	IO	IO	User Port	151	IO	IO	User Port
111	IO	IO	User Port	152	IO	IO	User Port
112	VCC	I	power supply	153	IO	IO	User Port
113	IO	IO	User Port	154	IO	IO	User Port
114	IO	IO	User Port	155	GND	I	power supply

115	IO	IO	User Port	156	IO	IO	User Port
116	IO	IO	User Port	157	IO	IO	User Port
117	IO	IO	User Port	158	IO	IO	User Port
Serial number	Pin Symbols	I/O/Z	Function	Serial number	Pin Symbols	I/O/Z	Function
159	IO	IO	User Port	191	IO	IO	User Port
160	VCC	I	power supply	192	IO	IO	User Port
161	IO	IO	User Port	193	IO	IO	User Port
162	IO	IO	User Port	194	IO	IO	User Port
163	IO	IO	User Port	195	IO	IO	User Port
164	IO	IO	User Port	196	IO	IO	User Port
165	GND	I	power supply	197	GND	I	power supply
166	IO	IO	User Port	198	IO	IO	User Port
167	IO	IO	User Port	199	IO	IO	User Port
168	IO	IO	User Port	200	IO	IO	User Port
169	IO	IO	User Port	201	IO	IO	User Port
170	VCC	I	power supply	202	IO	IO	User Port
171	IO	IO	User Port	203	IO	IO	User Port
172	IO	IO	User Port	204	IO	IO	User Port
173	IO	IO	User Port	205	VCC	I	power supply
174	IO	IO	User Port	206	IO	IO	User Port
175	IO	IO	User Port	207	IO	IO	User Port
176	GND	I	power supply	208	IO	IO	User Port
177	TDI	I	JTAG Port	209	DEV_CLRn/IO	I/IO	Configuration/user dual use
178	nCE	I	Configuring Ports	210	DI	I	Dedicated input
179	DCLK	I	Configuring Ports	211	GCLK	I	Dedicated clock input
180	DATA0	I	Configuring Ports	212	DI	I	Dedicated input
181	DATA1/IO	I/IO	Configuration/user dual use	213	DEV_OE/IO	I/IO	Configuration/user dual use
182	DATA2/IO	I/IO	Configuration/user dual use	214	IO	IO	User Port
183	DATA3/IO	I/IO	Configuration/user dual use	215	IO	IO	User Port
184	IO	IO	User Port	216	GND	I	power supply
185	DATA4/IO	I/IO	Configuration/user dual use	217	IO	IO	User Port
186	DATA5/IO	I/IO	Configuration/user dual use	218	IO	IO	User Port

187	IO	IO	User Port	219	IO	IO	User Port
188	DATA6/IO	I/IO	Configuration/user dual use	220	IO	IO	User Port
189	VCC	I	power supply	221	IO	IO	User Port
190	DATA7/IO	I/IO	Configuration/user dual use	222	IO	IO	User Port
Serial number	Pin Symbols	I/O/Z	Function	Serial number	Pin Symbols	I/O/Z	Function
223	IO	IO	User Port	232	GND	I	power supply
224	VCC	I	power supply	233	IO	IO	User Port
225	IO	IO	User Port	234	IO	IO	User Port
226	IO	IO	User Port	235	IO	IO	User Port
227	IO	IO	User Port	236	nRS/IO	I/IO	Configuration/user dual use
228	IO	IO	User Port	237	IO	IO	User Port
229	IO	IO	User Port	238	nWS/IO	I/IO	Configuration/user dual use
230	IO	IO	User Port	239	CS/IO	I/IO	Configuration/user dual use
231	IO	IO	User Port	240	nCS/IO	I/IO	Configuration/user dual use

Table 4. Function description of dedicated configuration port

Pin Symbols	User mode usage	Configuration mode	Pin Type	Functional Description
MSEL0 MSEL1	N/A	all	enter	Two-bit configuration mode selection signal input. The relationship between the input signal and the configuration mode is shown in Table 13. These two pins must be constantly valid after power-on until the end of the entire configuration process.
nCONFIG	N/A	all	enter	Configuration control signal input. Pulling this pin down in user mode will cause the FPGA to lose all configuration data and enter a reset state. All I/O pins are tri-stated. Pulling the pin back to a logic high state will initialize the FPGA to reconfigure.
nSTATUS	N/A	all	Bidirectional open drain	The FPGA pulls nSTATUS low immediately after power-on and releases it within 5μs. As a status output, if an error occurs during configuration, nSTATUS will be pulled low. As a status input. If an external source pulls nSTATUS low during configuration or initialization, the device enters the error state. Pulling nSTATUS low after configuration and initialization is complete does not affect the configured device.
CONF_DONE	N/A	all	Bidirectional open drain	The FPGA pulls the CONF_DONE pin low before and during configuration. Once all configuration data is received without error, the device enters the initialization state and the CONF_DONE pin is released and goes high. Pulling CONF_DONE low after configuration and

				initialization is complete will not affect the configured device.
nCE	N/A	all	enter	Chip enable signal, low effective. nCE goes low to allow configuration and activate the chip. The nCE pin must remain low during the configuration process, initialization process and user mode. It can be pulled down when configuring a single device. When multiple devices are chained, the nCE of the first configured device is pulled down and its nCEO is connected to the nCE of the next device in the chain. nCE must also remain low in the JTAG configuration mode.
CEO	N/A	all	Output	Driven low when the device is configured. When configuring a single device, leave it unconnected. When configuring multiple devices in a chain, connect it to the nCE of the next device in the chain and leave the nCEO of the last device in the chain unconnected.
DCLK	N/A	Synchronous configuration process (PS, PPS)	enter	Clock signal input. Data is latched into the FPGA on the rising edge of DCLK. In PPA mode, DCLK should be pulled up to VCC to prevent it from floating. After configuration is complete, this pin is tri-stated.
DATA0	N/A	all	enter	Data input. In serial configuration mode, the bit-width configuration data is passed

Table 5. Relationship between MSEL0, MSEL1 and configuration mode

MSEL1	MSEL0	Configuration Mode
0	0	PS
1	0	PPS
1	1	PPA
②	②	JTAG ①

Note:

- JTAG configuration has the highest configuration priority. When JTAG configuration is performed, the MSEL signal is ignored.
- After configuration is complete, do notMSELThe pins are left floating and connected to high or low levels.JTAGConfiguration mode, inJTAGJust ground them during configuration.

Table 6. Configuration/User IO dual-purpose port function description

Pin Name	User mode usage	Configuration mode	Pin Type	Functional Description
DATA [7…1]	I/O	Parallel mode (PPS, PPA)	enter	Data input. Bit-width configuration data enters the target device through DATA[7…0]. In serial configuration mode, these pins are used as user I/O pins during the configuration process and are left floating. After PPA or PPS configuration, DATA[7…1] are used as user I/O and their status depends on the setting of Dual_Purpose Pin option in software.
DATA7	I/O	PPA	Bidirectional	In PPA configuration mode, after nRS is selected, the DATA7 pin represents the RDYnBSY signal. In serial configuration mode, the DATA7 pin is used as a user I/O pin during the configuration process and is left floating. After PPA configuration, DATA7 is used as user I/O and its status depends on the setting of Dual_Purpose Pin option in software.
nW	I/O	PPA	enter	Write strobe signal input. Its rising edge causes the device to latch one byte of data from DATA[7…1]. In non-PPA configuration mode, it is used as a user I/O pin during configuration and is left floating. After PPA configuration, nWS is used as user I/O and its status depends on the setting of Dual_Purpose Pin option in software.
nR	I/O	PPA	enter	Read strobe signal input. When the input signal is low, the device will send the RDYnBSY signal to the DATA7 pin. If the nRS pin is not used in PPA configuration pull it high. In non-PPA configuration mode, it is used as a user I/O pin during configuration and is left floating. After PPA configuration, nRS is used as user I/O and its status depends on the setting of Dual_Purpose Pin option in software.
RDY	I/O	PPS PPA	Output	Ready to complete signal output. When the output signal goes high, it means the target device is ready to receive the next byte of data; when the output signal goes low, it means the target device is busy and not ready to receive the next byte of data. In PPS and PPA configuration modes, this pin will be pulled high at power-on, before configuration starts, and after configuration ends before entering user mode. In non-PPS and PPA configuration modes, it is used as user I/O during the configuration process and is left floating. After PPS or PPA configuration, RDYnBSY is used as user I/O and its status depends on the setting of Dual_Purpose Pin option in software.
nCS/CS	I/O	PPA	enter	Chip select signal input. The target chip is selected for configuration by inputting nCS low and CS high. During

				configuration and initialization, the nCS and CS pins must remain valid. In PPA configuration mode, only one of nCS or CS is needed to make the selection, and the unused pin is connected to a valid state. If nCS is grounded, the configuration process can be controlled by the jump of CS. In non-PPA configuration mode, it is used as user I/O during the configuration process and is left floating. After PPA configuration, nCS and CS are used as user I/O, and its status depends on the setting of Dual_Purpose Pin option in software.
CLKUSR	Software setting on: N/A Software setting off: I/O	all	enter	Optional user initialization clock input. Can be used to synchronize the initialization of one or more devices. This pin can be enabled by turning on the Enable user-suoolied start-up option in the QuartusII software.
INIT_ DONE	Software setting on: N/A Software setting off: I/O	all	Output open drain	Status output pin. It can be used to identify whether the device has completed initialization and entered user mode. When the nCONFIG pin is low at the beginning of configuration, the INIT_DONE pin is tri-stated and pulled up by an external 1kΩ resistor. Once the control word that enables INIT_DONE is written into the device (the control word is the beginning segment of the configuration data), INIT_DONE will go low. When initialization is completed, INIT_DONE will be released and pulled up, and the FPGA will enter user mode. Therefore, if there is a monitoring circuit, it must be able to detect the low-to-high jump. This pin can be enabled by turning on the Enable INIT_DONE option in the QuartusII software.
DEV_OE	Software setting on: N/A Software setting off: I/O	all	enter	Selectable pin allows the user to control all tri-states of the device. When this pin is pulled down, all I/Os are tri-stated; when this pin is pulled up, all pins work as configured. This pin can be enabled by turning on the Enable device-wide output enable (DEV_OE) option in the QuartusII software.
DEV_CLRn	Software setting on: N/A Software setting off: I/O	all	enter	Optional pin allows the user to control the clearing of all registers. When this pin is pulled down, all registers are cleared; when this pin is pulled up, all registers work as set. This pin can be enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the QuartusII software.

Table 7. JTAG dedicated port function description

Pin Name	User mode usage	Pin Type	Functional Description
TDI	N/A	enter	JTAG instruction, test data, and configuration data serial input pin. Data is shifted on the rising edge of TCK. If the JTAG interface is not used in the circuit, connect TDI to VCC to disable the JTAG circuit.
TDO	N/A	Output	JTAG instruction, test data, and configuration data serial output pin. Data is shifted on the falling edge of TCK. This pin is tri-stated when no data is being shifted out of the device. If the JTAG interface is not used in the circuit, leave TDO floating to disable the JTAG circuit.
TMS	N/A	enter	Provides a control signal input pin that determines the TAP state machine flip. The TAP state machine flips on the rising edge of TCK. Therefore, TMS must be set before the rising edge of TCK arrives. TMS will be sampled on the rising edge of TCK. If the JTAG interface is not used in the circuit, connect TMS to VCC to disable the JTAG circuit.
TCK	N/A	enter	JTAG clock input signal. Some operations occur on the rising edge of TCK, and some on the falling edge. If the JTAG interface is not used in the circuit, connect TCK to GND to disable the JTAG circuit.
TRST	N/A	enter	Active low input used to synchronize the reset of the boundary scan circuitry. The TRST pin is optional per IEEE Std. 1149.1. If the JTAG interface is not used in the circuit, connect TRST to GND to disable the JTAG circuit.

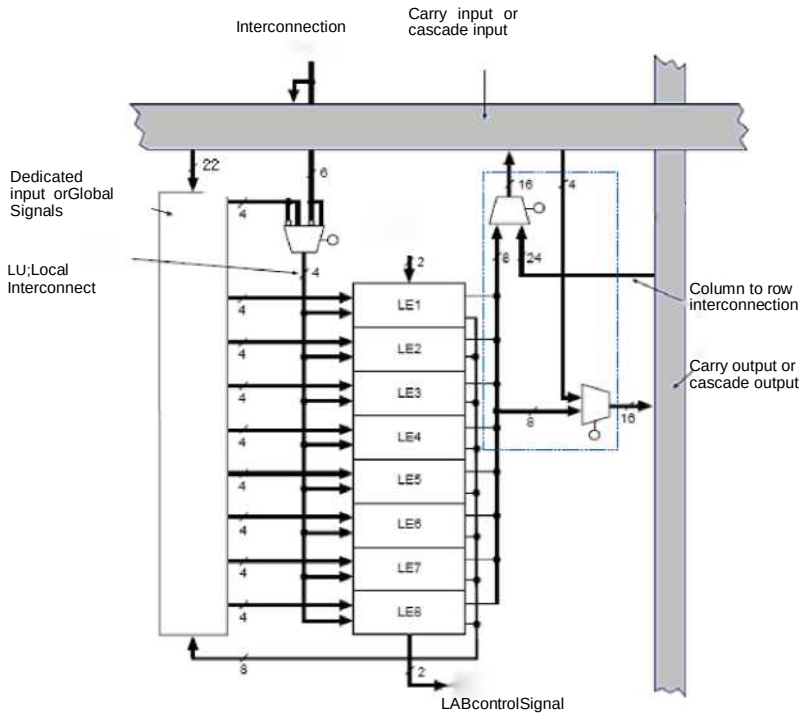
Functional Description

The circuit itself has no fixed logic functions, and its operation is divided into two main stages: configuration mode and user mode. In configuration mode, under the action of the configuration control circuit, the configuration data is written into the SRAM through the word line and bit line. The data determines the function and connection relationship of the circuit's configurable resources. After all the data is written, it enters the user mode to realize the configured function. The SRAM can be repeatedly erased and written to realize different circuit functions.

The internal structure consists of two parts: control circuit and configurable resources. The control circuit includes JTAG circuit, configuration control circuit, word line, bit line, and configuration data storage unit (SRAM); the configurable resources include configurable logic array block (LAB), configurable embedded memory array block (EAB), and configurable input and output unit (IOE). The configurable resources are connected to each other through configurable row and column wiring distributed among them.

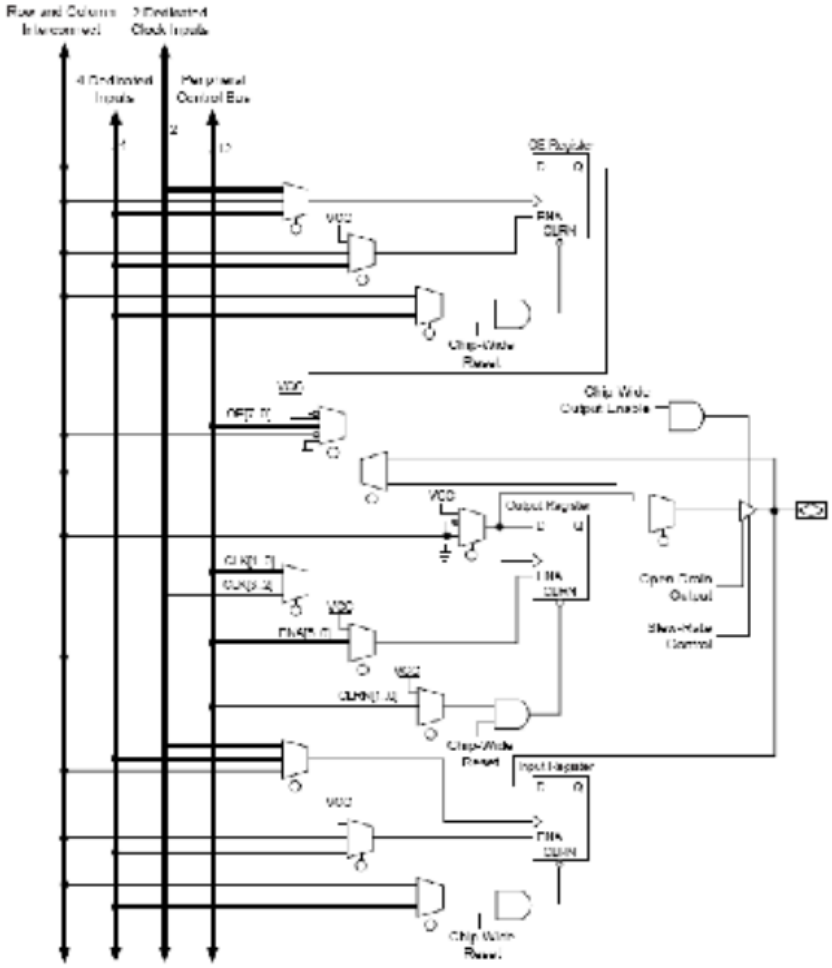
Logic Array Block (LAB)

The logic array of BSTP10K50 consists of logic array blocks (LABs), each of which contains eight logic elements (LEs), carry chains and cascade chains associated with the LEs, LAB control signals, and LAB local interconnects. These eight LEs can be used to implement medium-sized block logic - 8-bit counters, address decoders, or state machines - or to implement larger logic blocks through the combination of multiple LABs. See figure.



Configurable general purpose input and output units (Input/Output ELEMENT, IOE)

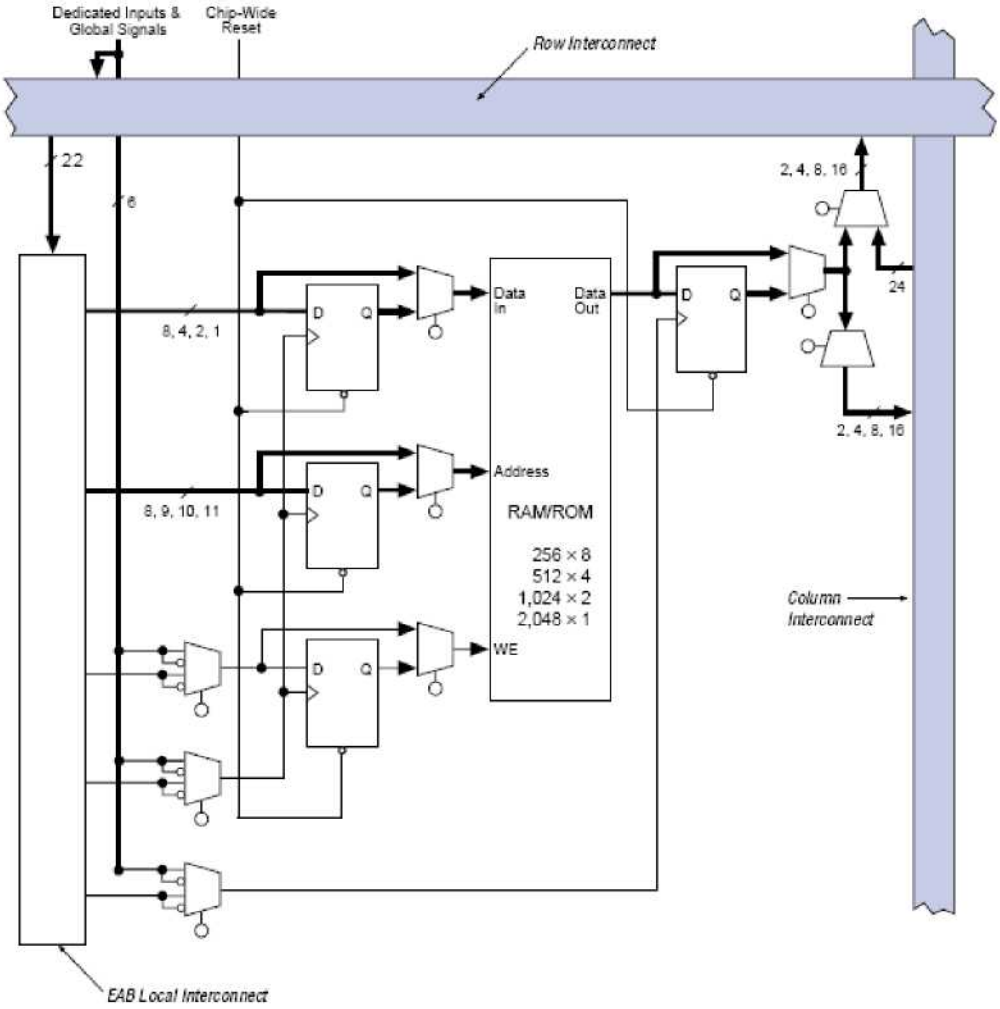
The configurable general-purpose input and output unit (IOE) provides an interface between the chip's external pins and internal logic functions. Each general-purpose input/output pin of the chip corresponds to an IOE. There are 304 general purpose IOE resources in the chip, including 72 in the upper and lower parts and 80 in the left and right parts. IOE can realize the data exchange function inside and outside the chip under the control of internal logic and external ports. The IOE structure is shown in the figure.



Input and output unit (IOE)

Embedded Storage Array Embedded array block, EAB)

The embedded array contains 10 EABs, each with a capacity of 2048 bits and a total capacity of 20480 bits. When used as a memory, it can be used as RAM, ROM, dual-port RAM, or FIFO. When configured as a logic function, it can be used for complex logic functions of 100 to 600 gates, such as multipliers, microcontrollers, state machines, and DSP chips. The EAB array can be used alone, or multiple EABs can be combined to form a larger logic function. The figure shows the structure of the embedded storage array block (EAB).



内嵌存储阵列块（EAB）结构图

Extreme working conditions and recommended working conditions

Extreme working conditions

Parameter name	Parameter range	unit
Supply voltage	-1.0~6.5	V
I/O input voltage	-1.0~6.5	V
Storage temperature range	-65~150	℃
Junction temperature	150	℃

Recommended operating conditions

Parameter name	Parameter range	unit
Operating temperature range	-55~125	℃
Device supply voltage	5±0.5	V
Port DC input voltage	-0.5~VCC+0.5	V

Main technical parameters

Electrical characteristic parameters

characteristic		symbol	condition (Unless otherwise specified, VCC=5V, -55℃≤TA≤125℃)	Standard value		unit
				Minimum	Maximum	
quiet state Ginseng number	Supply current (standby)	*I*CC0	*V*I=GND, no load		10	mA
	Input high level voltage	*V*IH		2.0	*V*CC+0.5	V
	Input low level voltage	*V*IL		-0.5	0.8	V
	Output high level voltage	*V*OH	*I*OH=-4mA DC, VCC=4.75V	2.4		V
	Output low level voltage	*V*OL	*I*OL=12mA DC, VCC=4.75V		0.45	V
	Input pin leakage current	*I*I	*V*I = VCC or GND	-10	10	μA
	Three-state input/output pin leakage current	*I*OZ	*V*O = VCC or GND	-40	40	μA
	Input Capacitance a)	*C*IN	*V*IN=0V, f=1.0MHz		10	pF
	Dedicated clock pin input capacitance a)	*C*INCLK	*V*IN=0V, f=1.0MHz		15	pF
	Output Capacitor a)	*C*OUT	*V*OUT=0V, f=1.0MHz		10	pF
logic Edit one Yuan L E	Data Input LUT Delay	*t*LUT			1.8	ns
	Carry Input LUT Delay	^{t}CLUT			0.6	ns
	LE register feedback LUT delay	*t*RLUT			2.0	ns
	Data input to packed register delay	*t*PACKED			0.8	ns
	LE Register Enable Delay	^{t}EN			1.5	ns
	Carry-in to carry-out delay	*t*CICO			0.4	ns
	Data-in to Carry-out Delay	^{t}CGEN			1.4	ns
	LE register feedback to carry output delay	^{t}CGENR			1.4	ns
	Cascade Input to Cascade Output Delay	*t*CASC			1.2	ns
	LE register control signal delay	*t*C			1.6	ns
	LE Register Clock to Output Delay	*t*CO			1.2	ns

hour	Combined Delay	*t*COMB			0.6	ns
Sequence Parameters	The setup time of the LE register data and enable signal before the clock; The recovery time of the LE register after asynchronous clear, preset or load	*t*SU		1.4		ns
	LE register data and enable signal, hold time after clock	*t*H		1.3		ns
	LE register preset delay	^{t}PRE			1.2	ns
sdf	LE register clear delay	^{t}CLR			1.2	ns

Minimum high time of clock pin	*t*CH		4.0		ns
Minimum low time of clock pin	*t*CL		4.0		ns

characteristic		symbol	Condition (Unless otherwise specified, VCC=5V, -55℃≤TA≤125℃)	Standard value		unit
				Minimum	Maximum	
Input and output unit IOE Timing Parameters	IOE data delay	*t*IOD			0.6	ns
	IOE register control signal delay	^{t}IOC			0.9	ns
	IOE Register Clock to Output Delay	^{t}IOCO			0.5	ns
	IOE combination delay	*t*IOCOMB			0.0	ns
	The setup time of IOE register data and enable signal before the clock; The recovery time of IOE register after asynchronous clearing	*t*IOSU		3.5		ns
	IOE register data and enable signal hold time after clock	*t*IOH		1.9		ns
	IOE register clear time	^{t}IOCLR			1.2	ns
	Output Buffer and PAD Delay	^{t}OD1	slow slew rate=off,C1=35pF		3.6	ns
	Output Buffer and PAD Delay	*t*OD3	slow slew rate=on, C1=35pF		8.3	ns
	IOE output buffer disable delay	^{t}XZ			5.5	ns
	IOE output buffer enable delay	^{t}ZX1	slow slew rate=off, C1=35pF		5.5	ns
	IOE output buffer enable delay	*t*ZX3	slow slew rate=on, C1=35pF		10.2	ns
	IOE input pad and buffer to IOE register delay	^{t}INREG			10.0	ns
	IOE register feedback delay	^{t}IOFD			4.0	ns
	IOE input pad and buffer to fast interconnect delay	*t*INCOMB			4.0	ns
Embedded Array Block	Combination input data or address to EAB delay	^{t}EABDATA			1.9	ns

EAB Micro Timing Parameters	Register input data or address to EAB delay	^{t}EABDATA			6.0	ns
	Combinatorial Input Write Enable to EAB Delay	*t*EABWE1			1.2	ns
	Register input write enable to EAB delay	^{t}EABWE2			6.2	ns
	EAB Register Clock Delay	*t*EABCL			2.2	ns
	EAB Register Clock to Output Delay	*t*EABCO			0.6	ns
	Bypass Register Delay	^{t}EABBYPAS			1.9	ns
	EAB register setup time	*t*EABSU		1.8		ns
	EAB register hold time	^{t}EABH		2.5		ns
	Address access delay	^{t}AA			10.7	ns
	Write pulse width	*t*WP		7.2		ns
	Data setup time before the falling edge of the write pulse	^{t}WDSU		2.0		ns
	Data hold time after the falling edge of the write pulse	*t*WDJ		0.4		ns
	Address setup time before the rising edge of the write pulse	*t*WASU		0.6		ns
	Address hold time after the falling edge of the write pulse	^{t}W.A.H.		1.2		ns
	Write Enable to Data Output Valid Delay	*t*WO			6.2	ns
	Data input to data output valid delay	^{t}DD			6.2	ns

sd

Data output delay	*t*EABOUT			0.6	ns
Clock high time	*t*EABCH	4.0			ns
Clock low time	^{t}EABCL	7.2			ns

characteristic		symbol	Condition (Unless otherwise specified VCC = 5V -55℃≤TA≤125℃)	Standard value		unit
				Minimum	Maximum	
Embedded Array Block EAB macro timing parameters	EAB address access delay	^{t}EABA			17.0	ns
	EAB asynchronous read cycle	*t*EABRCCO		17.0		ns
	EAB synchronous read cycle	^{t}EABRCRE		11.9		ns
	EAB write pulse width	*t*EABWP		7.2		ns
	EAB asynchronous write cycle	*t*EABWCCO		9.0		ns

	EAB Synchronous Write Cycle	$t_{EABWCRE}$		16.0		ns
	EAB data input to data output valid delay	t_{EABDD}			12.5	ns
	EAB clock to output delay when using output registers	$t_{EABDATAC}$			3.4	ns
	When using input registers, EAB data/address, setup time before clock	$t_{EABDATAS}$		5.6		ns
	When using input registers, EAB data/address, hold time after clock	$t_{EABDATA}$		0.0		ns
	When using the input register, EAB write enable is set up before the clock	t_{EABWES}		5.8		ns
	When using the input register, EAB write enable is enabled, and the hold time after the clock	t_{EABWEH}		0.0		ns
	The setup time of EAB data before the falling edge of the write pulse when the input register is not used	t_{EABWDS}		5.8		ns
	When the input register is not used, the EAB data is held after the falling edge of the write pulse.	t_{EABWDH}		0.0		ns
	When the input register is not used, the EAB address setup time before the falling edge of the write pulse	t_{EABWAS}		2.7		ns
	When the input register is not used, the EAB address is held after the falling edge of the write pulse.	t_{EABWAH}		0.0		ns
	Delay from EAB write enable to data output valid	t_{EABWO}			11.8	ns
JTAG Timing Parameters	TCK clock cycle	t_{JCP}		100		ns
	TCK clock high level time	t_{JCH}		50		ns
	TCK clock low level time	t_{JCL}		50		ns
	JTAG port setup time	t_{JPSU}		20		ns
	JTAG port hold time	t_{JPH}		45		ns
	JTAG port clock to output	t_{JPCO}			25	ns
	JTAG port high impedance to valid output	t_{JPZX}			25	ns
	JTAG port valid output to high impedance	t_{JPXZ}			25	ns

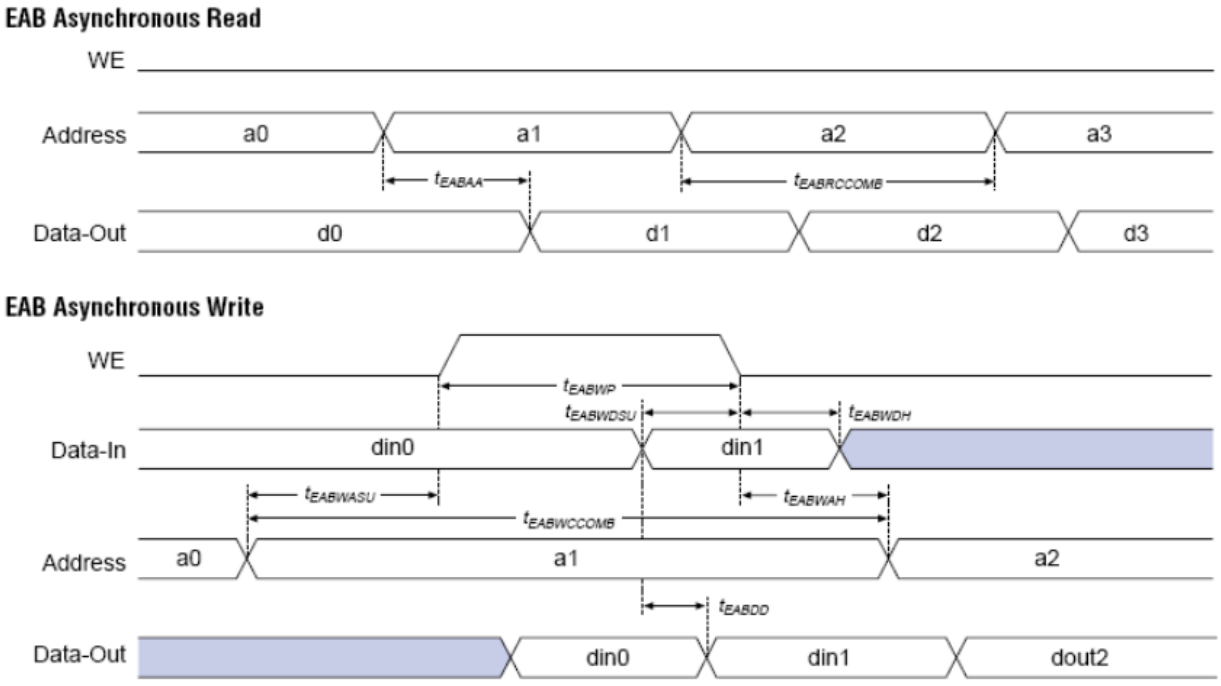
	Capture register setup time	*t*JSSU		20		ns
	Capture register hold time	*t*JSH		45		ns
	Update register clock to output	*t*JSCO			35	ns
	Update register high impedance to valid output	*t*JSZX			35	ns
	Update register valid output to high impedance	*t*JSXZ			35	ns

asdaTable (continued)

characteristic		symbol	condition (Unless otherwise specified VCC = 5V - 55℃≤TA≤125℃)	Standard value		unit
				Minimum	Maximum	
Interconnect routing timing parameters	Dedicated input to IOE control input delay	*t*DIN2IOE			10.2	ns
	Dedicated clock to LE or EAB clock delay	*t*DIN2LE			4.8	ns
	Dedicated input to LE or EAB data delay	*t*DIN2DAT			7.2	ns
	Dedicated clock to IOE clock delay	*t*DCLK2IO			6.2	ns
	Dedicated input to LE or EAB to control input delay	*t*DCLK2LE			4.8	ns
	Routing delay of an LE driving another LE in the same LAB	*t*SAMELA			0.3	ns
	The routing delay of a row of IOE, LE or EAB driving the same row to IOE, LE or EAB	*t*SAMERO			3.7	ns
	Routing delay of LE driving the same column IOE	*t*SAMECOLUN			4.1	ns
	A row of IOE, LE or EAB is driven differently Routing delay of row LE or EAB	*t*DIFFROW			7.8	ns
	One row of IOE or EAB drives different rows of outing delay of LE or EAB	*t*TWOROW			11.5	ns
	The wiring delay of the control signal of LE driving IOE through the peripheral control bus	*t*LEPERIPH			8.2	ns
	The routing delay of the carry-out signal of an LE driving the carry-in signal of an LE in a different LAB	*t*LABCARR			0.6	ns
	The cascaded output signals of LE drive the Routing delay of cascade input signals of LE	*t*LABCASC			3.0	ns
External Timing Parameters	Register-to-register delay through 4 LEs, 3 row nterconnects, 4 local interconnects	*t*DRR			21.1	ns
	IOE register global clock setup time	*t*INSU		6.4		ns

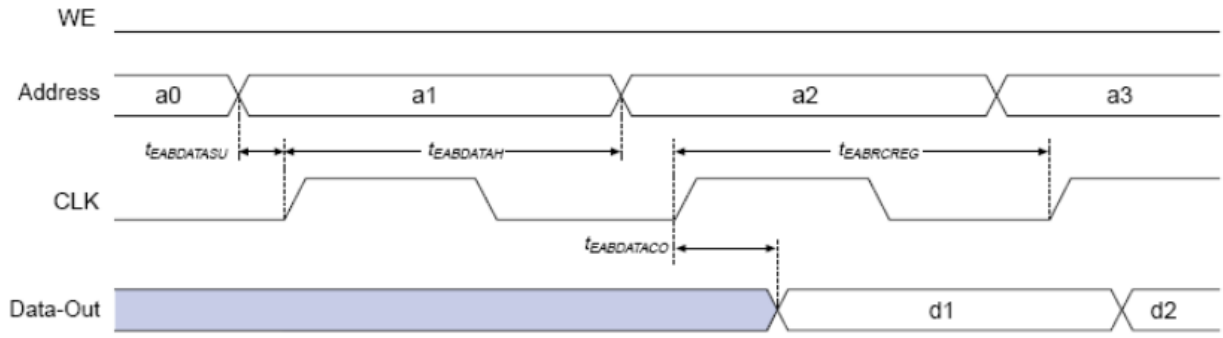
	IOE register global clock hold time	*t*INH		0.0		ns
	Clock-to-output delay for IOE register global clock	^{t}OUTCO		2.0	11.2	ns
External Bidirectional Timing Parameters	Setup time of the global clock from the bidirectional pin to the adjacent LE register	^{t}INSUBIDI		4.6		ns
	Hold time of the global clock from the bidirectional pin to the adjacent LE register	*t*INHBIDIR		0.0		ns
	Clock-to-output delay of bidirectional pin IOE register global clock	*t*OUTCOBID		2.0	11.2	ns
	Synchronous IOE output buffer disable delay	^{t}XZBIDIR			15.0	ns
	Synchronous IOE output buffer enable delay	^{t}ZXBIDIR	slow slew rate=off		15.0	ns

Timing diagram

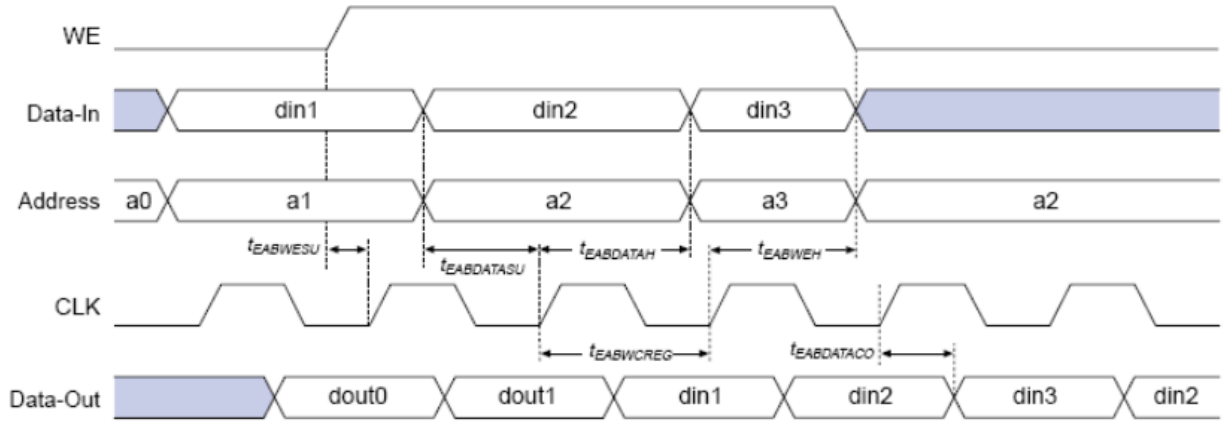


Embedded storage array block (EAB) Asynchronous read and write timing diagram

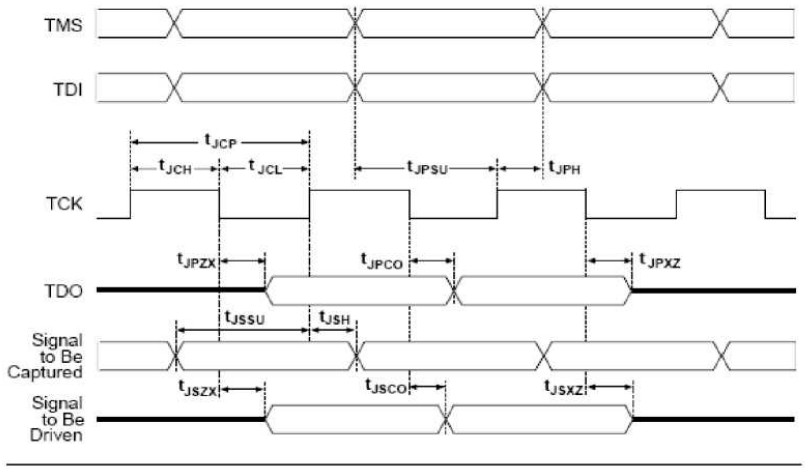
EAB Synchronous Read



EAB Synchronous Write (EAB Output Registers Used)



Embedded storage array block (EAB) Synchronous read and write timing diagram



JTAG working timing diagram

Key parameter timing diagram/typical application peripherals

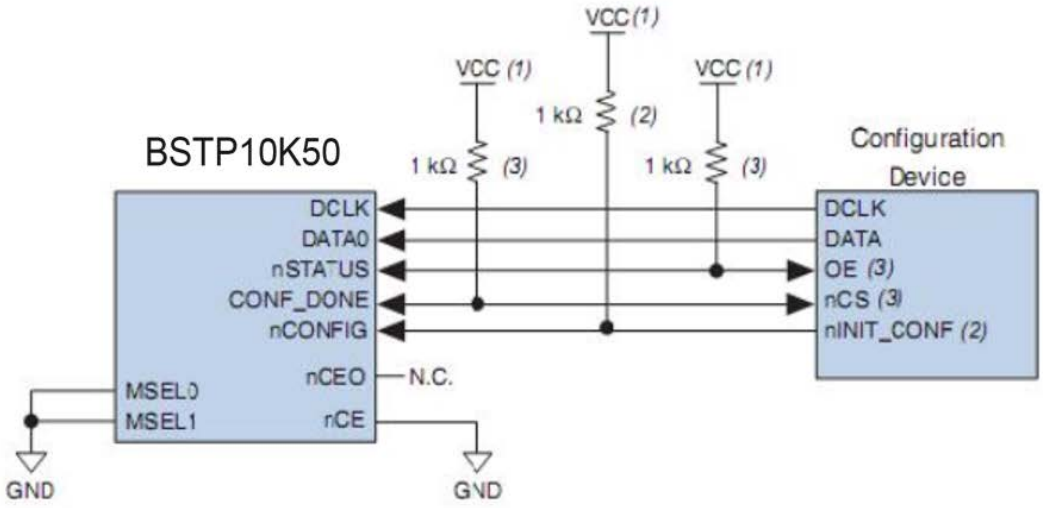
Supported configuration modes

MSEL0	MSEL1	Configuration Mode
0	0	PS
1	0	PPS
1	1	PPA
Not floating	Not floating	JTAG

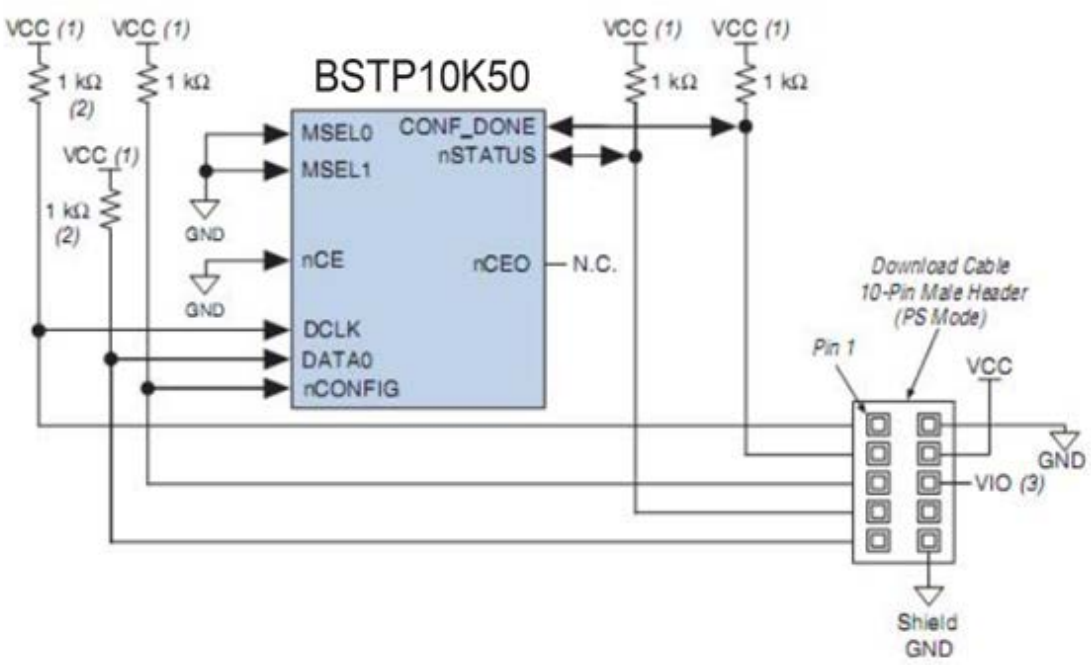
Note: JTAGMode takes precedence over other configuration modes

The BSTP10K50 configuration code stream data size is 784184 bits (98023 bytes). You need to select a suitable configuration chip based on this size.

Typical applications are shown in the figure below:



PS configuration mode connection diagram



PS configuration mode JTAG connection diagram

ESD Characteristics

According to the 3015.1 experimental conditions in GJB548B-2005, it can withstand 1000V ESD impact test.

FAQ

BSTP10K50 has a startup configuration process. Do not access the circuit before the configuration is completed.

BSTP10K50 is a CQFP240 package and weighs 20 grams. When installing the circuit, it is recommended that users give priority to epoxy resin adhesive materials and use the bottom fill curing method as much as possible.

Precautions

Product transportation and storage precautions

During the transportation of the circuit, use the designated anti-static packaging box to package it and ensure that the circuit does not collide or squeeze with foreign objects.

Circuit storage environment temperature: -65℃ to 150℃.

Product unpacking and inspection

When you unpack and use the circuit for the first time, check the circuit case and pins to make sure the case is not damaged or scratched, and the pins are neat, not missing, or deformed. At the same time, pay attention to the product logo on the circuit case to make sure it is clear, without stains or scratches.

Circuit Operation Precautions

Anti-static operation requirements

Devices must be handled with anti-static measures. Wear anti-static gloves when handling circuits to prevent ESD from damaging the circuits. When inserting the circuit into the base on the circuit board, pay attention to the direction of the circuit to prevent reverse insertion;

The following actions are recommended:

- The device should be operated on an anti-static workbench or by wearing anti-static gloves;
- Test equipment and instruments should be properly grounded;
- Do not touch the device surface and leads at will;
- Devices should be stored in containers made of conductive materials (e.g., special boxes for integrated circuits);
- Avoid using plastics, rubber or silk fabrics that cause static electricity during production, testing, use and transportation;
- Keep relative humidity above 50% as much as possible;
- When using, correctly distinguish the power supply and ground of the circuit to prevent short circuit.
- Do not use beyond the limit parameters.
- Add capacitor filtering at the power supply end.

Version and Disclaimer

Version Number	Release time
A1	January 21, 2015

Disclaimer:

Our institute is only responsible for the current validity of this product manual at the time of issuance, and will not notify you of version updates. If you need to know the latest information about this product, please consult us according to the contact information in Article 9.2.

All technical information contained in this product manual is only for users to have a preliminary understanding of this product. If there is any discrepancy with the detailed product specifications, the detailed product specifications shall prevail.