

BSTMFNP8G08BH4

8Gbit Parallel NAND Flash Circuit

Military Product Manual

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I. Product Introduction

1.1. Product Overview

BSTMFNP8G08BH4 For capacity 1G×8bit Non-volatility SLC NAND FLASH Flash storage

Device Support ONFI 1.0 The device is divided into blocks that can be erased

independently, so the device contains 4096 blocks, by 64 pages, each consisting of 32

A series of NAND structure Flash. The programming operation writes 4352 Typical times for byte/page are 200us, Erase 256K Typical times for bytes/blocks are 2ms The data read cycle in a page is 30ns.

1.2. Product Features

- Supply voltage VCC: 1.7V~1.95V
- Synchronous (4096+256) Byte Page Read
- Random read access maximum 35us
- Serial page read access is fastest 30ns
- Typical Page Programming Time 200us
- Block size: 256K+16K) byte

- Fast Block Erase Typical Value 2ms
- Supports fast data copying without external buffering
- Array layout: 4K+256) byte x 64 Page x 4096 piece
- Support ONFI 1.0 Parameter Table
- Operating temperature range: -55°C~125°C
- Erasing times: 3 Ten thousand times
- Data retention time: 10 Year
- Packaging type: plastic package FBGA63
- External ECC need: 8 Bit/512 byte ECC

1.3. Product use and application range

BSTMFNP8G08BH4 The circuit is 8 Gbit parallel SLC NAND FLASH Memory. The device is non random storage, non-executable code, but storage operations are performed in blocks, with high storage speed, suitable for large-capacity data storage. Widely used in smart phones, smart products, automotive electronics, industrial industry control, SSD, data center, enterprise-class switches, wired and wireless equipment, data center, video processing it is widely used in processing, test equipment, medical equipment, military and aviation, etc. where code or data storage is required.

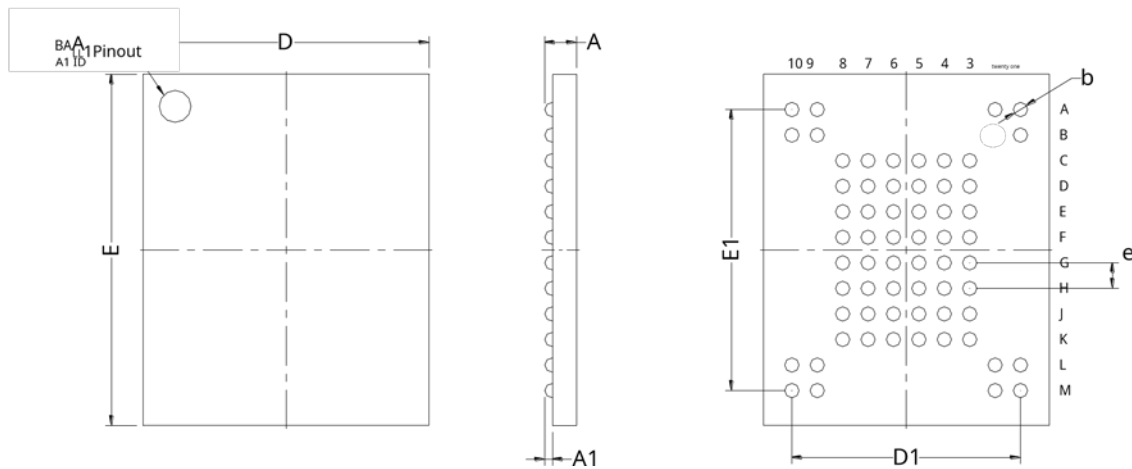
1.4. Corresponding to the situation of replacing foreign products

BSTMFNP8G08BH4 Circuit and MICRON Company MT29F8G08ADBCAH4 Product compatibility, only 4. There are differences in the pins, see the appendix for details A, can replace imported devices in situation.

II. Product appearance

2.1. Product size

BSTMFNP8G08BH4 use 63 ball FBGA Package, size as shown 2-1 shown.



UNIT: mm

OIMTIWON SYMBOLS	MINIMUM	NOMINAL	MAXIMUM
A	—	—	1.40
A1	0.25	—	—
b	—	0.4	—
D	8.9	—	9.1
e	—	0.80	—
E	10.9	—	11.1
D1	—	7.2	—
E1	—	8.8	—

Picture 2-1. FBGA63Dimensions

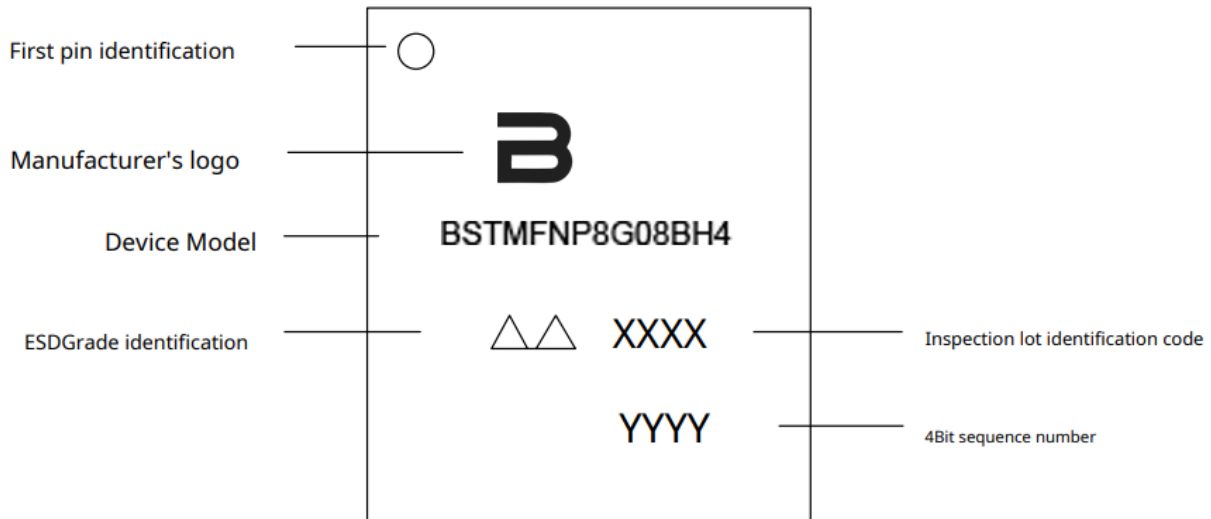
2.2. Weight

BSTMFNP8G08BH4The device weight is $0.15\text{g} \pm 0.05\text{g}$.

2.3. Packaging process

BSTMFNP8G08BH4 The device is encapsulated in plastic FBGA63Package. Solder balls are lead-freeSAC305, diameter 0.4mm.

2.4. Product photos and logo descriptions



Picture 2-3. Device Photos

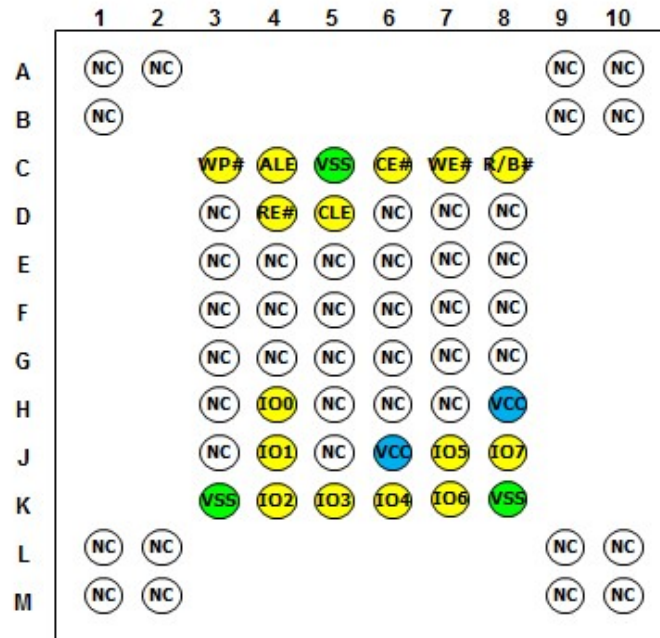
III. Standard Implementation

Product quality level meets GJB7400 Regulations N1 Level, assessment standards implementation Q/FC 50309-2022 Semiconductor Integrated Circuits BSTMFNP8G08BH4 type 8Gbit parallel NAND Flash Circuit Detailed Specifications.

IV. Brief description of basic working principle

4.1. Pin Description

BSTMFNP8G08BH4 Pinout arrangement:



Picture 4-1. Terminal arrangement diagram

Table 4-1. FBGA63 Package pin arrangement and function description

LEAD-OUT TERMINAL SERIAL NUMBER	LEAD END SYMBOL	TYPE	FUNCTION	LEAD-OUT TERMINAL SERIAL NUMBER	LEAD END SYMBOL	TYPE	FUNCTION
A1	NC	—	No connection	G4	NC	—	No connection
A2	NC	—	No connection	G5	NC	—	No connection
A9	NC	—	No connection	G6	NC	—	No connection
A10	NC	—	No connection	G7	NC	—	No connection
B1	NC	—	No connection	G8	NC	—	No connection
B9	NC	—	No connection	H3	NC	—	No connection
B10	NC	—	No connection	H4	I/O0	Bidirectional	data

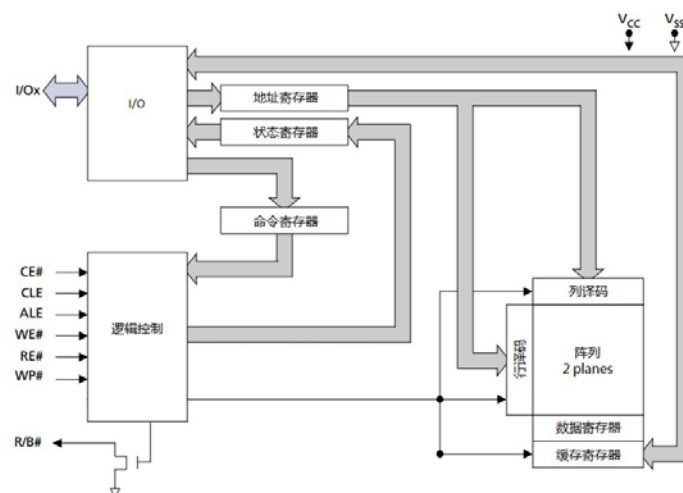
C3	WP#	enter	Write protection	H5	NC	—	No connection
C4	ALE	enter	Address latch enables able	H6	NC	—	No connection
C5	VSS	land	Core reference ground	H7	NC	—	No connection
C6	CE#	enter	Chip Enable	H8	VCC	power supply	Core Power Supply
C7	WE#	enter	Write Enable	J3	NC	—	No connection
C8	R/B#	Output	Preparation/Busy	J4	I/O1	Bidirectional	data
D3	NC	—	No connection	J5	NC	—	No connection
D4	RE#	enter	Read Enable	J6	VCC	power supply	Core Power Supply
Lead-out terminal Serial number	Lead end symbol	type	Function	Lead-out terminal Serial number	Lead end symbol	type	Function
D5	CLE	enter	Command latch enables able	J7	I/O5	Bidirectional	data
D6	NC	—	No connection	J8	I/O7	Bidirectional	data
D7	NC	—	No connection	K3	VSS	land	Kernel Reference land
D8	NC	—	No connection	K4	I/O2	Bidirectional	data
E3	NC	—	No connection	K5	I/O3	Bidirectional	data
E4	NC	—	No connection	K6	I/O4	Bidirectional	data
E5	NC	—	No connection	K7	I/O6	Bidirectional	data
E6	NC	—	No connection	K8	VSS	land	Kernel Reference land
E7	NC	—	No connection	L1	NC	—	No connection
E8	NC	—	No connection	L2	NC	—	No connection

F3	NC	—	No connection	L9	NC	—	No connection
F4	NC	—	No connection	L10	NC	—	No connection
F5	NC	—	No connection	M1	NC	—	No connection
F6	NC	—	No connection	M2	NC	—	No connection
F7	NC	—	No connection	M9	NC	—	No connection
F8	NC	—	No connection	M10	NC	—	No connection
G3	DNU	—	Do not use				

4.2. Circuit Function

This product is a high-speed, large-capacity parallel NAND FLASH Memory, the storage capacity of a single chip is 8Gbit (1G×8bit), the highest frequency can reach 40MHz. I/O. The pins are used as address and data input/output to Commands, data, and addresses are used CE#, WE#, ALE and CLE Input Pins synchronous introduction. The on-chip program/erase controller automatically performs all programming and erase functions, including pulse repetition (where required) and internal validation and data margining. WP# Input pin to lock modification operations.

The circuit functional block diagram is shown in the figure below.



Picture 4-2. Functional Block Diagram

Table 4-2. Chip pin function description

PIN NAME	DESCRIBE
I/O0-I/Ox	Data Input/Output IO The pin allows command, address, and data to be input and data to be output during read/program operations. WE#)When the device is deselected or the output is disabled ,I/O The buffer floats to high impedance.
CLE	Command latch enable This input is used during write enable (WE#)The rising edge of DQInput latch.
ALE	Address Latch Enable This input is used during write enable (WE#)The rising edge of DQInput latch.
CE#	Chip Enable This input controls the device selection. When the device is busy, CE#Low does not deselect memory.
WE#	Write Enable This input is used as the clock to latch commands, addresses, and data. DQ Input WE# The rising edge of the SPI is latched.
RE#	Read Enable RE# The input is the serial data output control and when activated drives data into the I/O The data is on the bus. RE# After the falling edget Valid, this also increments the internal column address counter by one.
WP#	Write protection WP# When the pin is low, hardware protection is provided to prevent accidental modification (program/erase) operations.
Pin Name	describe
R/B#	Ready/Busy R/B# The output is an open-drain pin that indicates the memory status.
VCC	Supply voltage VCC Provides power for all operations (read, write, erase).V CC Less than V L K Internal locking circuitry prevents command insertion when
VSS	land
NC/DNU	Not Connected/Do Not Use

This product is SLC Process large capacity NAND Memory, support tONFI Standard interface, storage capacity is 8Gbit(1G× 8bit), 8The 1-bit bus transmits commands, addresses, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE# Additional signals control hardware write protection and monitor device status (R/B#). The device truth table is shown in Table 4-3.

Table 4-3. Device read and write truth table

CLE	ALE	CE#	WE#	RE#	WP#	MODEA,B	
H	L	L	Rising edge	H	X	Read Mode	Command Input
L	H	L	Rising edge	H	X		Address input
H	L	L	Rising edge	H	H	Write Mode	Command Input
L	H	L	Rising edge	H	H		Address input
L	L	L	Rising edge	H	H	Data Entry	
L	L	L	H	Falling edge	X	Data export (in progress)	
X	X	L	H	H	X	Data output (pause)	
L	L	L	H	H	X	Busy time in reading	
X	X	X	X	X	H	Busy time in programming	
X	X	X	X	X	H	Busy time in erasure	
X	X	X	X	X	L	Write protection	
X	X	H	X	X	0V / VCC	Standby	

Illustrate:

- L=Logic Low, H=Logic High, X=Logic low or logic high, WP#In standby mode, the bias 0 Vor VCC.
- Device functional operation should be performed externally 8bit/512 Byte ECC under the conditions of.

4.2.1. Bus command operation mode

- Command Input

The command input bus operation is used to issue commands to the memory device.

The device accepts commands when enable is high, address latch enable is low, and read enable is high, and write enable is high.

In addition, for commands that initiate modification operations (write/erase), the write protection pin must be high.

The command code always applies to IO<7:0>, regardless of the bus configuration (X8/X16).

- Address input

The address input bus operation allows the insertion of memory addresses. The address is held low when the chip enable is low and the address latch is enabled.

It is accepted when the command latch enable is high, the command latch enable is low, and the read enable is high, and is accepted on the rising edge of the write enable.

In addition, for commands to initiate a modify operation (write/erase), the Write Protect pin must be high.

Address always applies to IO<7:0>, regardless of the bus configuration (X8/X16).

- Data Entry

The data input bus operation allows the data to be supplied to the device for programming. Data insertion is serial and is done by Write enable cycle timing. Only when chip enable is low, address latch enable is low, command latch enable is low, and read enable is low

Data is accepted only when write enable is high and write protect is high, and is latched on the rising edge of write enable.

- Data Output

The data output bus operation allows data to be read from the memory array and

the status register contents to be checked, locked, Status and ID Data. Data can be shifted out serially when the chip enable is low, the write enable is high, and the address

Toggles the read enable pin when latch enable is low and commands latch enable low.

- Write protection

When the write protection pin is low, the hardware write protection is activated. In this case, the repair will not be started.

The write protection pin is not latched by the write enable latch to ensure that even if protection is also provided during power-up.

- Standby

In the standby state, the device is deselected, the outputs are disabled, and power consumption is reduced. 4.2.2 Device command set and operation mode

Table 4-4. Device Operation Command Set

SERIAL NU	MBER FUNCTION	1 ST CYCLE	2 ND CYCLE	3 RD CYCLE	4 TH CYCLE	BUSY TIME RECEIVED COMMAND
1	Page Read	00h	30h	-	-	
2	Multi-sided reading	00h	00h	30h		
3	Read replication	00h	35h	-	-	
4	Multi-sided read replication	00h	00h	35h		
5	ReadID	90h	-	-	-	
6	Reset	FWf	-	-	-	Yes
7	Page programming (start) / cache programming (end)	80h	10h	-	-	
8	Cache programming (start/continue)	80h	15h	-	-	
SERIAL NU MBER	FUNCTION	1 ST CYCLE	2 ND CYCLE	3 RD C CLE	4 TH CYCLE	BUSY TIME RECEIVED COMMAND
9	Copy Programming	85h	10h	-	-	
10	ONFI Multifaceted Programming	80h	11h	80h	10h	
11	ONFI Multi-faceted Cache Programming	80h	11h	80h	15h	

12		ONFI Multi-faceted replication programming	85h	11h	85h	10h	
13		Block Erase	60h	D0h	-	-	
14		ONFI Multi-sided block erase	60h	HkDJ	60h	D0h	
15		Read Status Register	70h	-	-	-	Yes
16		Read Status Enhancement	78h				Yes
17		Random data input	85h	-	-	-	
18		Random data output	05h	E0h	-	-	
19		ONFI Random data output enhancement	06h	E0h			
20		Read Cache (Sequential)	31h				
twenty	one	Read cache enhancement (random)	00h	31h	-	-	
twenty	two	Read cache end	3F	-	-	-	
twenty	three	Read parameter page	ECh				
twenty	four	Read ON FI only ID	HkDJ	-	-	-	
25		Get features	E				
26		Setting Features	E				

- Page Reading

At initial device power-up, the device defaults to read mode. This operation is also accomplished by 00 hand 30 even same 5. The second of two consecutive read operations is initiated by writing the command register together with the address cycle.

Definitely need 00h command, these four address cycles and 30 h command to start the operation.

If the operation is also performed using the Random Data Output command, the second read operation always requires a Set command.

Two types of operations are available: random read, serial page read. Random read is enabled when the page address changes.

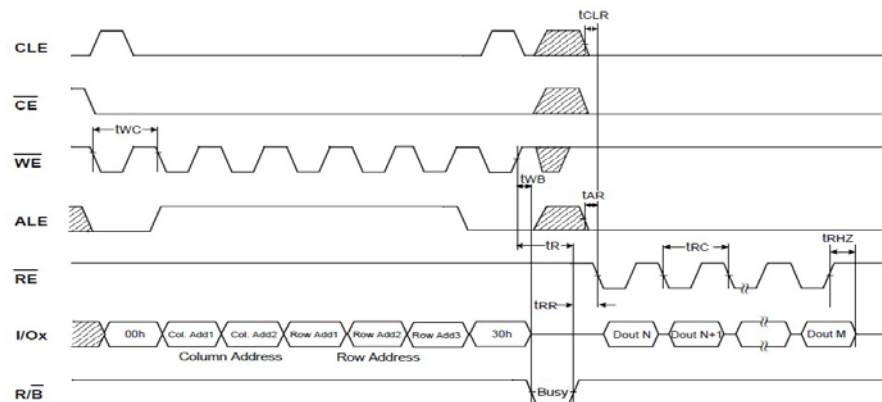
The selected page 4352 Bytes of data in less than 35us (tR) Transmitted to the data server within

The system controller can analyze R/B # The output of the pin is used to detect this data transmission (tR) of completion.

Once the data in the page are loaded into the data register, they can be reset by sequential pulses RE #exist 30 ns cycle

Read out within time. RE# Repeated high-to-low transitions of the clock cause the device to output the address starting with the selected column and ending with the last address.

Data of a column address.



Picture 4-3. Read Timing

The device can output random data in pages instead of consecutively by writing the random data output command.

The column address of the next data to be output can be changed to the address following the random data output command. site.

Random data output can be performed multiple times regardless of how many times it is completed in one page.

The device is in read mode, so no00hA read operation can be initiated by a command cycle.

Any operation other than machine data output will cause the device to exit read mode.

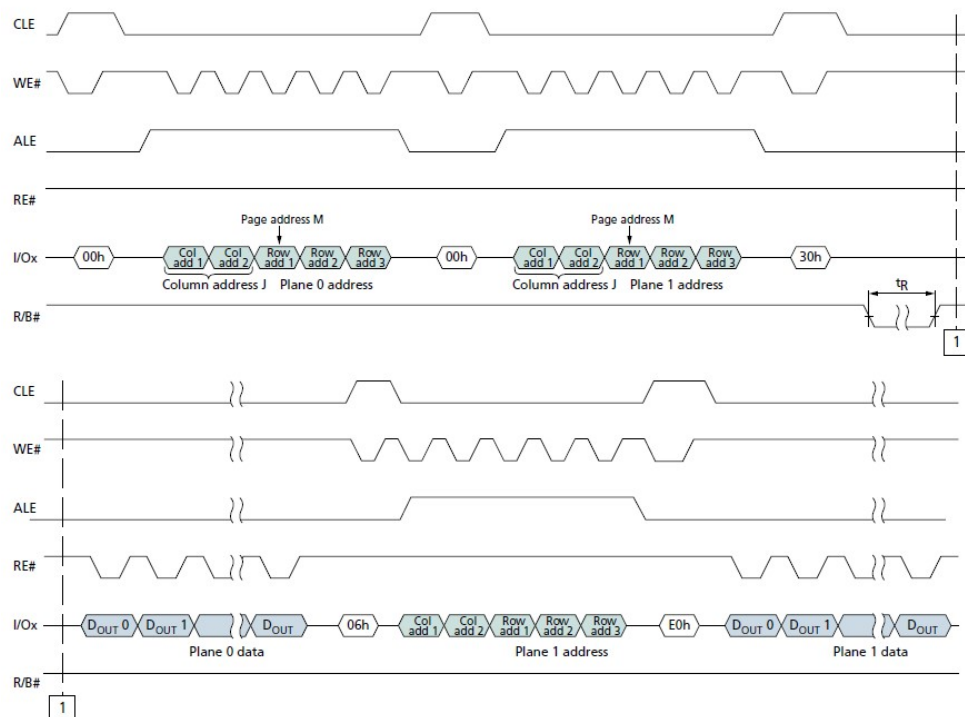
- Multi-page reading

Multi-page page read operations work by simultaneously copying data from

multiple pages to a specified cache register.

Improve data throughput. This is achieved by multi-page reads (00h-00h-30h or 60h-60h-30h) Command completed of when die (LUN). When you are ready, ONFI. Random data output enhancement (06h-E0h). Command determines which face Output data. During data output, the data in the cache register can be read and modified using the following commands:

Random Data Read(05h-E0h)and random data input (85h).



Picture 4-4. Multi-sided read timing

- Read Cache

The read cache feature allows one page to be read from the page register while another page is being read from the flash array.4-4

The Read Page command defined in the Read Cache Sequence should precede the initial sequential or random Read Cache command in the Read Cache Sequence issued before.

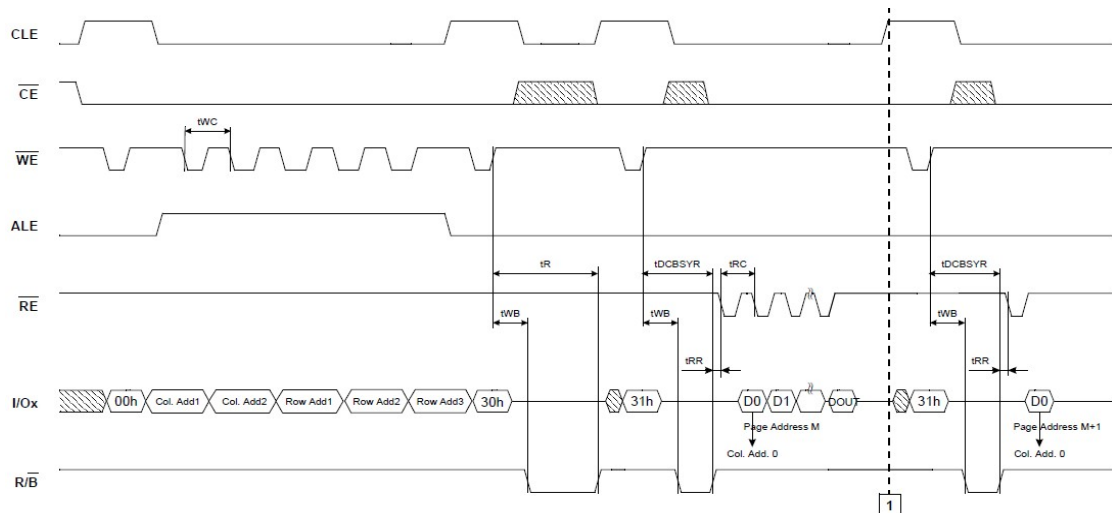
The read cache function can be issued after the read function is completed

(SR[6]Set to 1) The host can enter the the address of the next page to be read from the Flash array. Data output always starts from the column address 00h. If the host does not enter the address to be retrieved, and read the next consecutive page. When the read cache function is issued, SR[6] Cleared (Busy). After the operation starts, SR[6]Set to 1(Ready) , the host can start reading from a previous read or read buffer

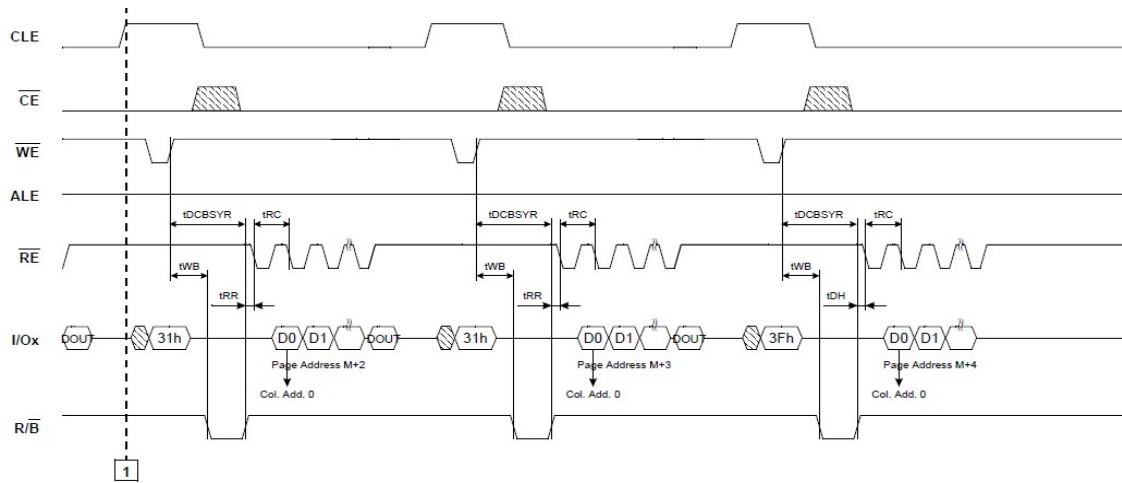
The cache function reads the data. Issues an additional read cache function to copy the most recently read data from the array.

into the page register. When the page is no longer needed, 3F The command copies the last page to In the page register. SR[6]Set to 1(Ready), the host can start reading data from the page register when issued 31 hand 3F. When commanding, SR[6]Should be cleared (busy) until the page is completed from Flash Array

After reading the last page of the device, the host should not issue a sequential read cache (31h) Order.



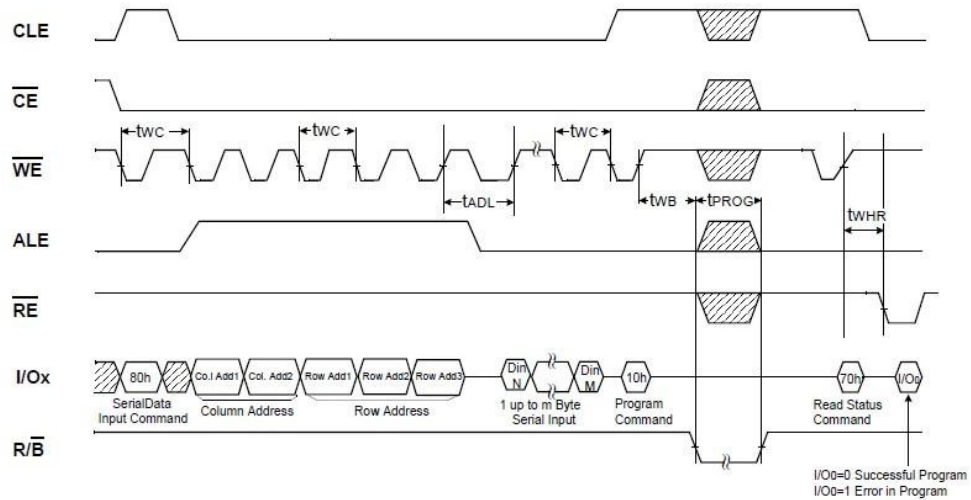
Picture 4-5. Read Buffer Timing(a)



Picture 4-6. Read Buffer Timing(b)

Multi-sided read cache the multi-side read cache operation can be used to output data from multiple cache registers and to transfer one or more pages from NANDThe flash array is copied to the data registers. This is done by31h)Add multiple faces before the command read(00h-00h-30h)command to complete. Page programming the device is basically page-programmed, but it allows one word or up to 4352Multiple partial page programming of consecutive bytes.

- The page programming cycle consists of a serial data loading cycle with a maximum of 4352 Bytes of data can be added The data is then loaded into the data registers, followed by a nonvolatile programming cycle, where the loaded data is programmed into the appropriate single In the element grid.
- The serial data load cycle starts with the input serial data input command (80h) Start, then 5 Cycle The address is entered followed by the serial data. Words other than the word to be programmed do not need to be loaded.



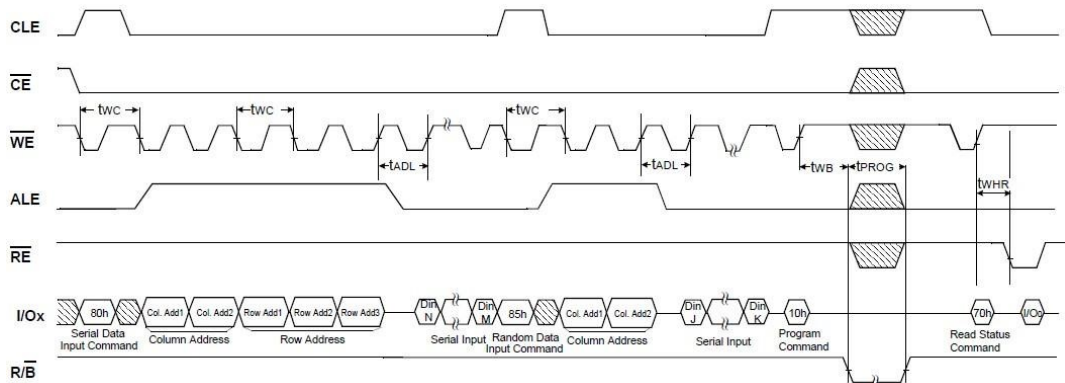
Picture 4-7. Page Programming Timing

The device supports random data entry in a page. The column address of the next data to be entered can be changed to the same column address as the Enter the command with random data (85h) address. Random data input may be operated on multiple times regardless of How many times it is done in one page. Page Program Confirm Command (10h) Starts the programming process. The internal write state controller automatically performs programming and verify the algorithms and timing required, freeing up the system controller to perform other tasks.

The system controller can read the status register by entering the read status register command.

Monitoring RB# Output or Status Register Status Bits (I/O 6) To detect the completion of the program cycle.

During the process, only the read status command and reset command are valid.



Picture 4-8. Random Input Timing in Page Programming

When page programming is complete, the write status bits can be checked (I/O 0). Internal write verification only detects failure programming as "0" of "1" Error. The command register remains in the read state command mode until another a valid command is written to the command register.

- Multifaceted Programming

Device supports multi-side programming: can be programmed in parallel 2 Pages, one per page.

A multi-side programming cycle consists of a dual serial data load cycle, in which up to 8704 Character. The data of the first section is loaded into the data register, followed by a nonvolatile programming cycle, and the loaded data is programmed. to the appropriate cell.

The serial data load cycle starts with the input serial data input command (80h) Start, then the 1 Page 5 cycle address input and serial data. The page address must be on the first side ($A_{19} = 0$). The device supports the random data input is exactly the same as the page program operation. The virtual page program confirmation command (11h) Stop first Page data is input, the device becomes busy for a short time (t_{DBSY}).

Once it is ready again, it must issue a 81h or "80h" command, followed by the second page address (5 cycles) and its serial data input. This page address must be in the second plane ($A_{19} = 1$). Programming confirmation command make (10h) Start by programming two pages in parallel.

Users can monitor RB# pin or the Read Status Register command (70h or 78h) to check the operation. The read status register command can also be used during the virtual busy time.

(tDBSY) Use during this period.

If either the first or second page programming fails, the fail bit in the status register will be set;

However, in order to know which page failed, you must issue ONFI 1.0 "Read Status Enhanced" command.

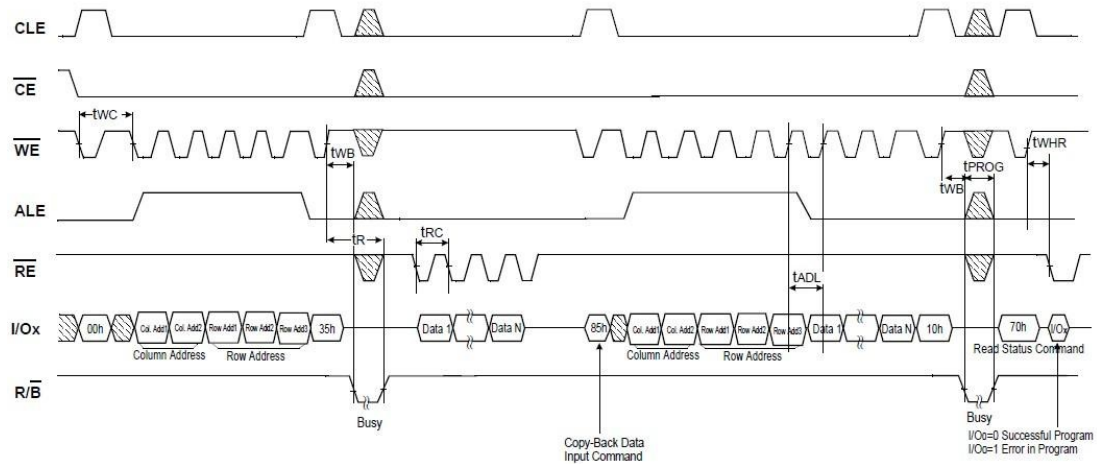
Replication Programming overwrite programming is configured to quickly and efficiently rewrite the data stored in a page without using external memory. This improves system performance by eliminating time-consuming serial access and reload cycles.

This is especially useful when part of a block is updated and the rest of the block also needs to be copied to a newly allocated free block.

The copyback programming operation is a sequential process of page read without serial access and copy program with target page address.

Use "35h" command and the source page address read operation will be the entire 4352 byte (X8 device) or 2176 Character (X16 device) data is moved into the internal data buffer.

Once the device returns to the ready state, it can be switched RE# to allow optional data readout or write a copyback command with the target page address cycle (85h). Programming Confirmation Command (10h) Need to start programming Operations. A data entry loop that allows modification of a portion of a source page or multiple remote portions.



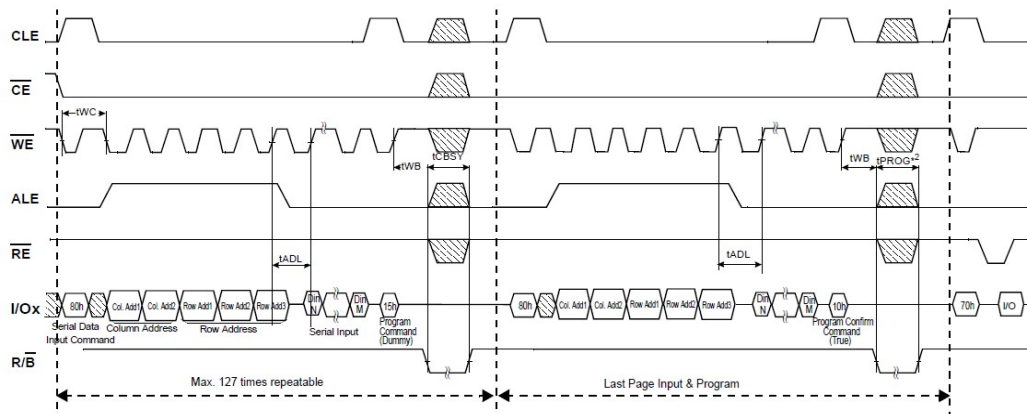
Picture 4-9. Rewrite programming sequence

Multi-faceted replication programming for page programming, the device supports multi-plane copy programming with exactly the same sequence and restrictions.

Reprogramming must be done in the Copy Back command sequence. Before reading a single page (the first page must be read from the first side, The second page must be read from the second side).

Multi-side copyback cannot cross side boundaries: the contents of a source page on one device side can only be copied to the destination page on the same side.

- Label page.
- Cache programming
- Cache programming is an extension of standard page programming, which uses two 4352 byte (x8 device) or 2176
- Words (x16 device) registers, data, and cache registers.
- In short, cache programming allows data from one page to be inserted while programming of another page is in progress.
- Programming is only available within blocks.



Picture 4-10. Cache Programming Timing

During the serial data input command (80h) is loaded into the command register, followed by 5 address cycles, a full or partial page of data is latched into the cache register.

Once the cache write command (15h) is loaded into the command register, the data in the cache register will be transferred to the data register for cell programming. The device will remain busy for a short time (PCBSY). After all the data in the cache registers are transferred to the data registers, the device returns to the ready state and allows another cache programming command sequence (80h-15h) to load the next data into the cache in the device.

The first sequence 80h - 15h. The subsequent busy time is equal to the transfer of data from the cache register to the data register. The time required to program the data register data unit and load the next data into the cache registers are processed through a pipeline model.

In any subsequent sequence 80h - 15h. In this case, the transfer from the cache register to the data register will be suspended until the cell programming of the current data register contents is complete; until then, the device will remain in a busy state (tPCBSY).

You can issue a read status command (70h) to check the status of different registers and pass/fail status state.

More details as follows:

- Cache busy bit I/O<6> Indicates when a cache register is ready to accept new data.
- Status Bits I/O<5> Can be used to determine when cell programming of the current data register contents is complete
- Cache Program Error Bit I/O<1> Can be used to identify the previous page in a cache programming operation
- (No.N-1 The latter can be found in I/O<6> The status bit changes to "1" Time Wheel Inquiry.
- Error bit I/O<0> Used to identify the Program/Erase Controller in the Programming Page N Is any Error. The latter can be I/O<5> The status bit changes to "1" Polling is performed at the same time.

I/O<1> Can be used with I/O<0> Read together.

If the system only uses R/B# To monitor the progress of the operation, you must use the Page Program Confirm command (10h) right If you use the cache program command (15h), but Status bits must be polled I/O<5> to determine whether the last operation has completed before starting any other operations programming.

- Multi-faceted Cache Programming

The device supports multi-side cache programming, which allows data from both sides to be utilized simultaneously by programming two pages in parallel and cache registers to implement caching, thereby achieving high programming throughput.

The device supports traditional and ONFI 1.0 Command set. The command sequence can be summarized as follows:

- Serial Data Input Command (80h), followed by five cycles of address input, and then the first page of the string The address of this page must be in 1 Within each face (A<19>=0) In addition to the data to be programmed. The data for the page does not need to be loaded. The device supports random

data input exactly the same as the page programming operation.

- Virtual Page Program Confirm Command (11h) Ends at 1 Page data is input, and the device is briefly Becomes busy (tDBSY).
- Once the device returns to the ready state, it must issue 81h(or 80h) command, followed by the second

Page Address (5cycles) and its serial data input. The address of this page must be within the second plane ($A_{19}=1$) It is not necessary to load the first 2 Page data.

- Cache Programming Confirmation Command (15h) Once the cache write command (15h) is loaded into the command register, the data in the cache register is transferred to the data register for unit programming. Keep busy during the PCBSY). After all the data in the cache register is transferred to the data register,

The device returns to the Ready state and allows the next data to be loaded into the cache via another sequence of cache programming commands.

Stored in register sequence 80h-...- 11h-...-...81h-...-...15h(or the corresponding ONFI 80h-...- 11h-...-...80h-...-...15h) can be iterated, and any new time the device will be busy completing the unit programming of the current data register contents required PCBSY time and can allow transfers from cache registers.

- The order to end multi-sided cache programming is 80h-...- 11h-...-...81h-...-...10h(or ONFI 1.0 Condition
- Down 80h-...- 11h-...-...80h-...10h Multi-faceted cache programming is only possible within two pairs of blocks belonging to two faces. use.
- Users can R/B#pin or the Read Status Register command (70h or 78h) Check the operating status state
- If the user selects 70h, a status register read will provide “global” information about the operation in both planes interest.

- More details as follows:

- I/O<6>Indicates when the two cache registers are ready to accept new data.
- I/O<5>Indicates when the cell programming of the current data register is complete
- I/O<1>Identifies the previous page in both pages (pageN-1) has been successfully programmed. The latter can be
- I/O<6>The status bit changes to "1"Polling is performed at the same time.
- I/O<0>Mark on two pagesNDoes the Program/Erase Controller detect any Error. The latter can beI/O<5>The status bit changes to "1"Polling is performed at the same time.

If the system only usesR/B#To monitor the progress of the operation, you must use the Page Program Confirm command (10h) program the last few pages of the target programming sequence. If you use the cache program command (15h), you must poll the status bitI/O<5>to determine whether the last sub-programming.

- Block Erase

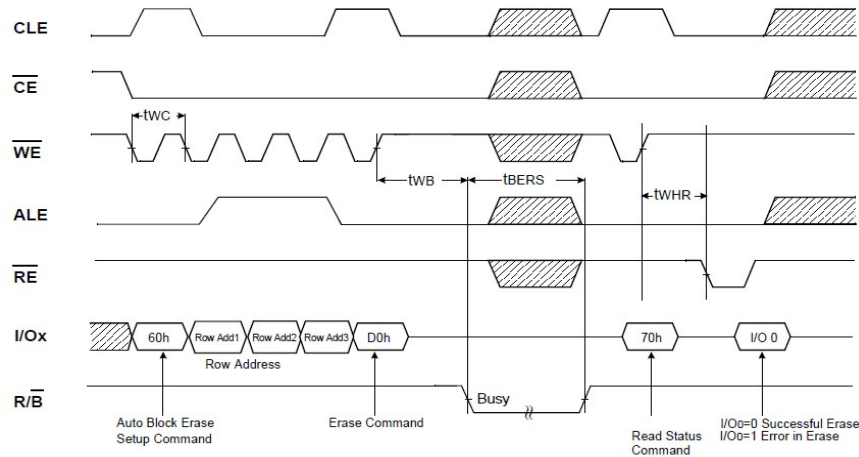
The erase operation is done on a block basis. The block address is loaded in the Erase Set command (60h) start up of3The erase confirmation command after the block address is loaded (D0h)Starts the internal erase process.

A two-step setup sequence following the command execution ensures that the memory contents are not accidentally erased due to external noise conditions.

After the erase confirmation command is enteredWE#. On the rising edge of 0, the internal write controller handles the erase and erase verification.

Once the erase process begins, the status register can be read by entering the Read Status Register command. The system controller can monitorRB#Output or Status Register Status Bits (I/O 6)To detect erasure is during the erase process, only the read status command and reset command are valid. When the erase

operation is completed, The write status bit can be checked (I/O 0).



Picture 4-11. Block Erase Timing

- 12 Multi-sided erasing

Multi-plane erase, allowing erasing of two blocks in parallel, one on each storage plane.

In these cases, two different command sequences are allowed, traditional and ONFI 1.0.

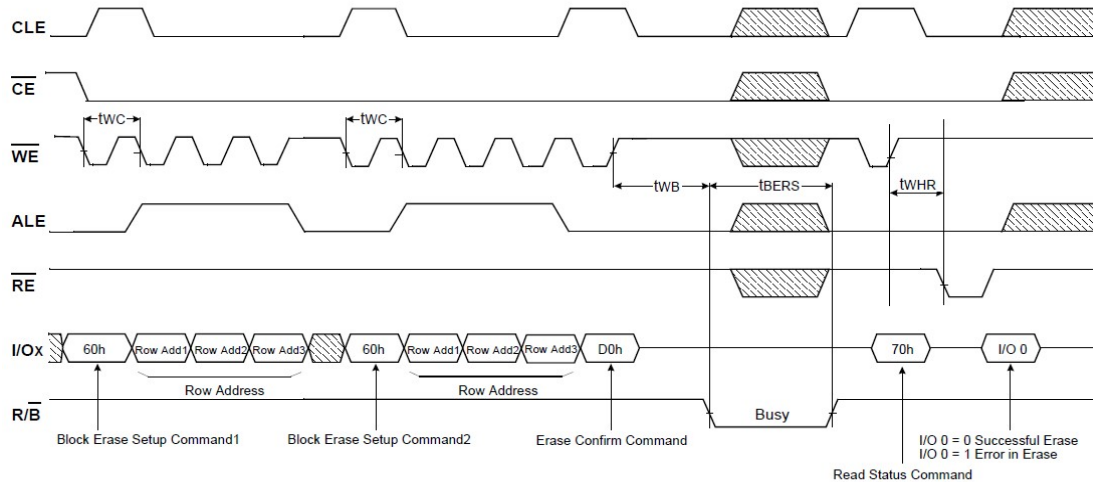
Traditionally, the Block Erase Setup command (60h) must be repeated twice, then the first and the second block address (each time 3 cycles). For block erase, D0h The command starts the embedding operation.

In this case, multi-side erase does not require any virtual busy time between the first and second block insertions.

As an alternative, you can use ONFI 1.0 Multifaceted Command Protocol, 60h Erase settings followed by the first block addresses and HkDJ. First, confirm that 60h The erase setting is followed by the second block address and D0h (Multiple confirmation). Between two block-related sequences, a short busy time occurs. TIEBSY.

The address restrictions required for multi-side programming also apply to multi-side erasing.

ONFI 1.0 Read status enhancement to check operation progress like in multi-faceted programming.

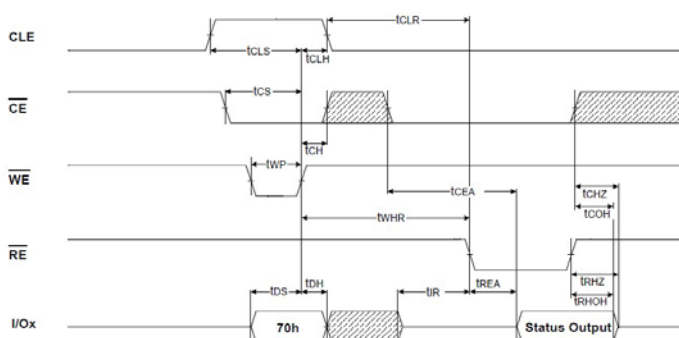


Picture 4-12. Multi-side erase timing

- Read the status register

The device contains a status register that can be read to determine whether the device is reading, programming, or erasing the erase operation is complete and the program or erase operation is completed successfully. 70h Command write command send after the status register is loaded, a read cycle places the contents of the status register in $\overline{CE}$ or $\overline{RE}$. The falling edge (the last occurring whichever) output to I/O. These two lines control the multiple memory connections that allow the system to poll each The progress of the device, even if $\overline{RB}$ The pins are wired in common. $\overline{RE}$ or $\overline{CE}$. No need to switch to update status. The command register remains in status read mode until further commands are issued to it.

- If the status register is read during a random read cycle, the read command should be given before starting the read cycle. (00h) .onePage



Picture 4-13. Read Status Register Timing

Table 4-5. Status Register Definition

IO	PAGE PROGRAMMING	BLOCK ERASE	READ	CACHE READ	CACHE PROGRAMMING/ CACHE RECOMPILATION PROCEDURE	CODING
0	Pass/Fail	Pass/Fail	NA	NA	Pass/Fail	NPage pass:'0' fail:'1'
1	NA	NA	NA	NA	Pass/Fail	N-1Page pass:'0' fail:'1'
2	NA	NA	NA	NA	NA	-
3	NA	NA	NA	NA	NA	-
4	NA	NA	NA	NA	NA	-
5	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Busy: '0' Ready:'1'
6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Data Cache Ready/Busy busy Busy: '0'Ready:'1'
7	Write protection	Write protection	Write protection	Write protection	Write protection	Protect:'0' Unprotected:'1'

- Read status enhancement

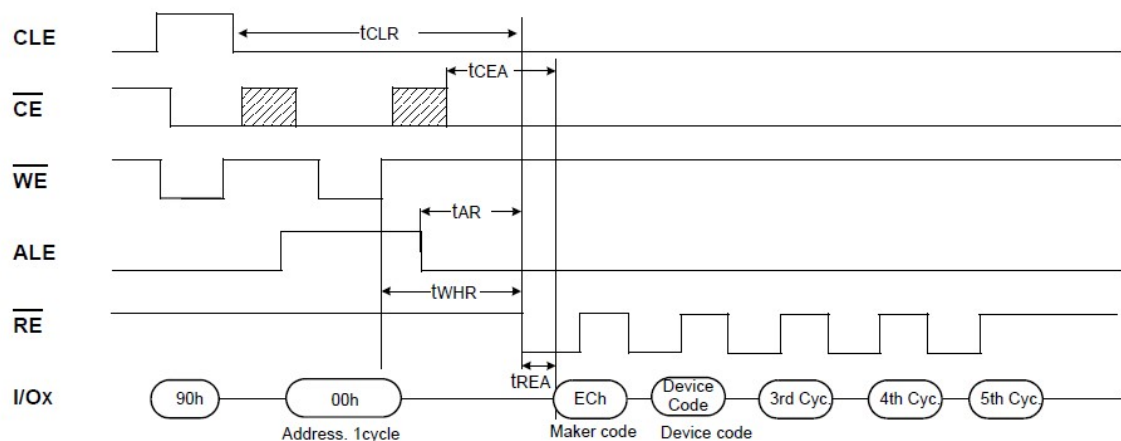
The read status enhancement is an additional feature for retrieving the status value of a previous operation in the following situations:

- In case of parallel operation, multi-chip stack configuration (single CE#)
Specific die superior.
- On a specific Table die When performing multi-faceted operations.
- Defines the behavior and timing of read status enhancement. The plane and die Address, Search for interesting die. The command register remains in

status read mode until an entry is issued.

- One step command twoPage
- Read ID

The device contains a product identification mode, which is achieved by writing to the command register 90h Start, then address enter 00h.



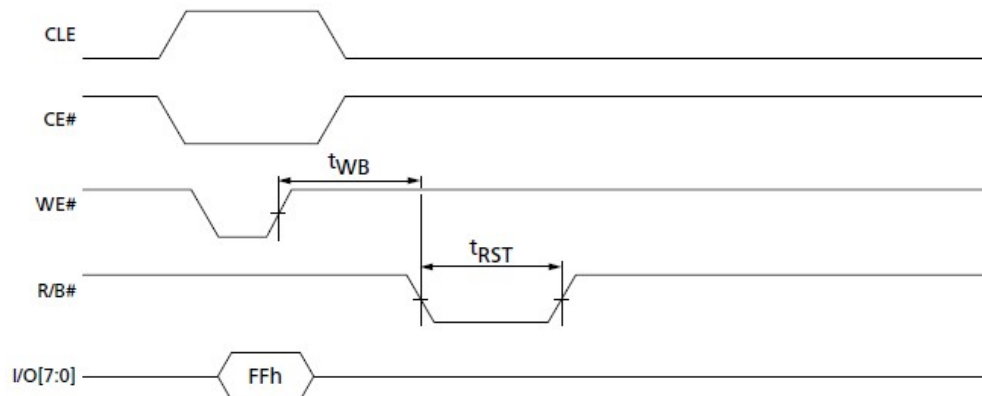
Picture 4-14. Read ID Timing

Table 4-6. IDInformation Definition

DEVICE IDENTIFIER BYTE	DESCRIBE
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, unit type...
4th	Page size, block size, spare size, organization
5th	Multifaceted information

Reset

The device provides a reset function by turning FWf Write to the command register to execute.



Picture 4-15. Reset Timing

When the device is busy during random read, program, or erase mode, the reset operation is aborted these operations. The contents of the memory cells being altered are no longer valid because the data will be partially programmed or erased three Page.

The command register is cleared to wait for the next command. WP# When high, the status register is cleared for value E0h. See Table 4-4 Understand the device status after the reset operation.

The command register will not accept new reset commands. After writing the reset command, RB# Pin in RST Expect becomes low level.

Read parameter page

The Read Parameter Page function retrieves data structures that describe the chip organization, features, timing, and other behavioral parameters.

The values in the parameter page are static and must not be changed. The host is not required to read the parameter page after a power management event.

A change read column command may be issued during execution of a read parameter page to read a specific portion of the parameter page.

Read Status can be used to check the status of the Read Parameter Page during execution. After the Read Status command completes,

The host should issue the following command on the command line: 00h to continue reading the data output stream of the parameter page command.

The Enhanced Read state should not be used during the Read Parameter Page command.

V. Extreme working conditions and recommended working conditions

5.1. Extreme working conditions

Supply voltage (VCC).....0.6V~+2.4V

Input voltage (VIN).....0.6V~+2.4V

Storage temperature range (Tstg).....65°C~150°C

Maximum lead soldering temperature (Th)(10s).....245°C

Maximum Junction Temperature (Tj).....175°C

Maximum power consumption (PD).....84mW

5.2. Recommended operating conditions

Supply voltage (VCC)1.7V~1.95V

Input high level (VIH)0.8×VCC~VCC+0.3V

Input low level (VIL)0.3V~0.2×VCC

Working environment temperature (TA)55°C~+125°C

VI. Main technical parameters

Table 6-1. Electrical properties

CHARACTERISTIC	SYMBOL	UNLESS OTHERWISE SPECIFIED VIO=VCC=3.3V, - 55°C≤TA≤+125°C	LIMIT VALUE		ONE BIT
			MINIMUM	MAXIMUM	
Input leakage current	ILI	VIN= 0V to VCC	—	±10	μA
Output leakage current	ILO	VOUT= 0V to VCC	—	±10	μA
Input high level	VIH	I/O, CE#, CLE, ALE, WE#, RE#, WP#, R/B#	0.8VCC	VCC+0.3	V
Input low level	VIL	—	— 0.3	0.2VCC	V
Output high level	VOH	IOH= -400μA	VCC-0.1	—	V

Output low level	VOL	IOL= 100μA	—	0.1	V
Output low current	IOL	testR/B#port,VOL= 0.2V	3	—	mA
Sequential reading current	ICC1	tRC=tRC(min); CE# =VIL;IOUT= 0mA	—	35	mA
Programming Current	ICC2	—	—	35	mA
Erase current	ICC3	—	—	35	mA
Standby Current(TTL)	ISB1	CE# =VIH; WP# = 0V/VCC	—	1	mA
Standby Current (CMOS)	ISB2	CE# =VCC- 0.2V; WP# = 0V/VCC	—	100	μA
ALETo the beginning of data	tADL		100	—	ns
ALEKeep Time	tALH		5	—	ns
ALEBuild Time	tALS		10	—	ns
CE#Keep Time	tCH		5	—	ns
CLEKeep Time	tCLH		5	—	ns
CLEBuild Time	tCLS		10	—	ns
CE#Build Time	tCS		25	—	ns
Data retention time	tDH		5	—	ns
Data creation time	tDS		10	—	ns
Write command cycle	tWC		30	—	ns
WE#Pulse width is high	tWH		10	—	ns
WE#Pulse Width	tWP		15	—	ns
ALEarriveRE#Delay	tAR		10	—	ns
CE#Access time	tCEA		—	30	ns
CLEarriveRE#Delay	tCLR		10	—	ns
CE#To output hold	tCOH		15	—	ns
Output high impedance toRE#Low	tIR		0	—	ns
Read command cycle	tRC		30	—	ns
RE#Access time	tREA		—	25	ns
RE#High hold time	tREH		10	—	ns
RE#High to output hold time	tRHOH		15	—	ns
RE#High to output high	tRHZ		—	100	ns

impedance					
RE#Pulse Width	tRP		15	—	ns
Ready toRE#Low	tRR		20	—	ns
Reset time (read/program/erase)	tRST		—	5/10/500	μs
WE#High toBusytime	tWB		—	100	ns
WE#High toRE#Low	tWHR		80	—	ns
Block Erase Time	tBERS		—	10	ms
Program page operation time	tPROG		—	700	μs
Page read operation time	tR		—	35	μs

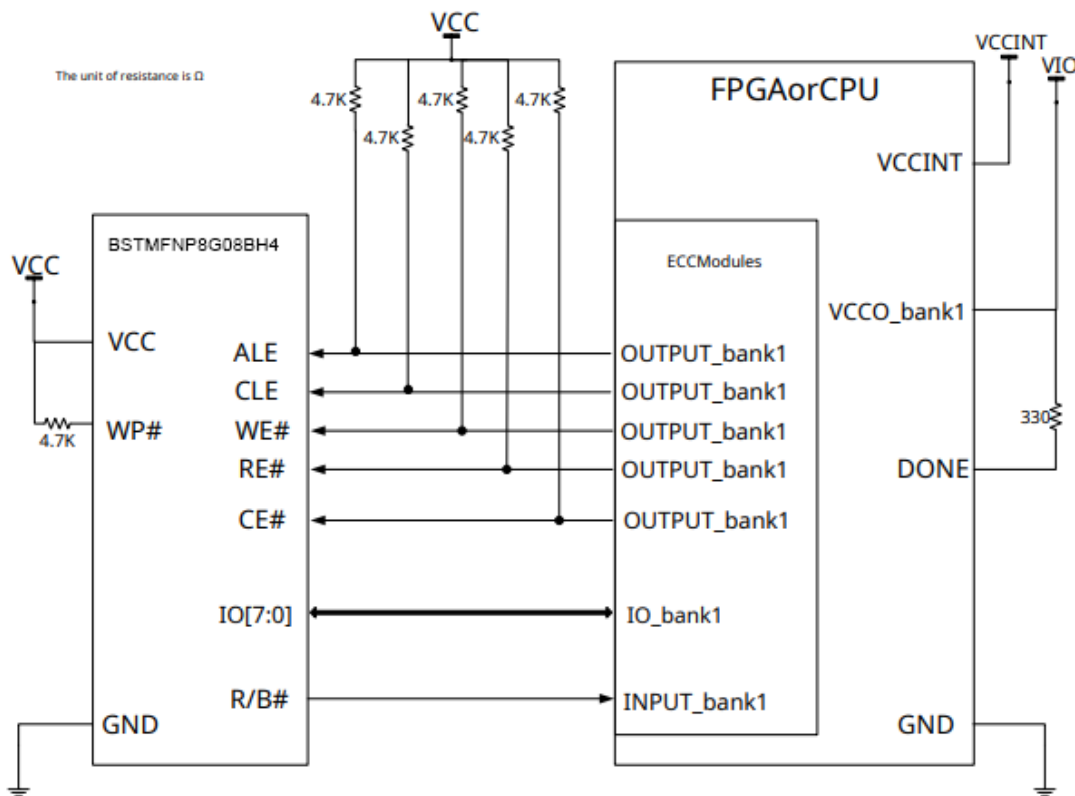
VII. Application Guide

7.1. Typical Applications

The typical application of this product is as FPGA or CPU. Data storage device, typical application is shown in the figure7-1Place please confirm before use. FPGA or CPU Is the port voltage consistent with BSTMFNP8G08BH4Match,

After confirming the match, connect according to the connection relationship shown in the figure. In addition, this product needs to be used with an external ECC,

Minimum ECC The ability requirements are8bit/512Byte.R/B#Pin Connection FPGA or CPUF or monitoring BSTMFNP8G08BH4 state, when R/B#When it is high,BSTMFNP8G08BH4InREADYstate, can receive instructions to operate. R/B#. When low,BSTMFNP8G08BH4InBUSYStatus, Input.The instruction is invalid.



Picture 7-1. Typical application diagram

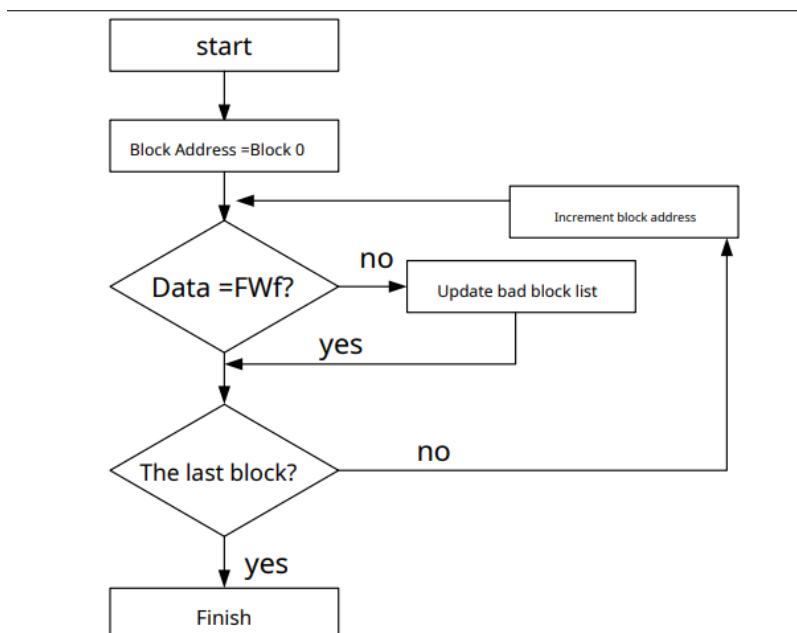
7.2. Bad Block Management

NAND FLASHThe device allows bad blocks to exist. Therefore, this product must be used with an externalECC, minimumECCThe ability requirements are8bit/512ByteThe difference between a device with some bad blocks and a device with all valid blocks is have the same quality level and the same AC and DC characteristics. Bad blocks will not affect the performance of valid blocks because the device is internally isolated from the bit line and common source line by select transistors.

All locations will be erased (FWf). The initial bad block information is written before shipment. If the first or second The first byte of the spare area of the page (if the first page is bad) does not contain FWf, which is a bad block.

Before any erase operation, the bad block information must be read because the bad block information may be erased.

To be able to identify bad blocks based on raw information, it is recommended to create a bad block table according to the following flow chart.



During the device's operating cycle, additional bad blocks may be generated. In this case, the data must be copied to a these additional bad blocks can be identified because attempts to row programming or erasing will generate errors in the status register.

The failure of a page programming operation will not affect the data in other pages in the same block, and can be repaired by re-programming.

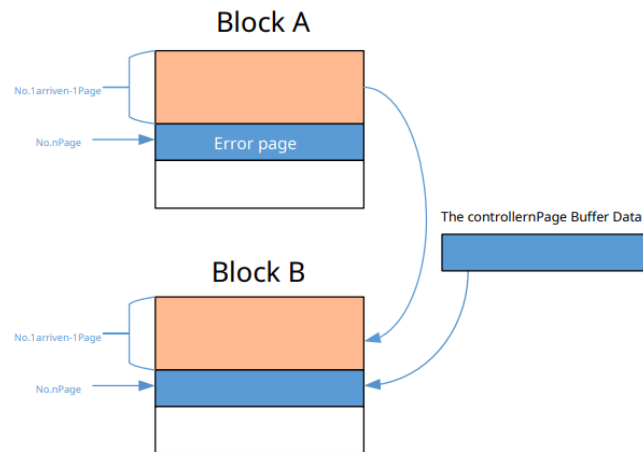
The block is replaced by programming the current data and copying the remainder of the replaced block to an available valid block.

Table 7-1.Bad Block Management Methods

Failure Mode		Management methods
Write operation failure	Erase Failure	Post-erase status confirmation→Bad block replacement
	Programming failure	Status confirmation after programming→Bad block replacement
Read operation failure	onebitRead failure	ECCcheck→ECCErrors Correction

The bad block replacement process is as follows:

- During an erase or program operation, Block 'A' No. n Page error occurred.
- Will Block 'A' No. 1~(n-1). The data of the page is copied to another free block (Block 'B') The same bit set.
- Buffer memory Block 'A' No. n Page data is copied to Block 'B' No. n Page.
- Do not erase or program to blocks by creating an "invalid block" table or other appropriate scheme "A".



VIII. Precautions

8.1. Product transportation and storage precautions

The chip storage environment temperature is: -65°C to +150°C. Use the designated anti-static packaging box to pack the product during transportation, make sure that the chip does not collide with foreign objects.

In an air-conditioned environment with temperature and humidity control, prevent the pins from oxidizing due to long-term storage, which will affect solderability.

8.2. Product unpacking and inspection

When unpacking and using the chip, please pay attention to the product logo on the chip shell. Make sure the product logo is clear.

No stains, no scratches. At the same time, pay attention to check the chip shell and pins. Make sure the shell is not damaged or scratched.

The pins are neat, without any missing or deformation.

8.3. Circuit Operation Precautions

This product is an electrostatic sensitive device and should be operated in strict accordance with the electrostatic sensitive device regulations of the relevant national standards.

Requires installation and operation.

- During the installation of this product, it is forbidden to touch or weld this type of product without anti-static wrist straps and other tools.
- Contact with the external leads of the product. Installation and use must be done in an anti-static work area (equipped with an anti-static workbench, table chair, etc.) is equipped with an ion fan and operates within the effective range of the ion fan.
- Operators must receive anti-static training and wear anti-static work clothes (including anti-static gloves or fingers).
- Do not wear protective gloves, hats, work shoes and anti-static wrist straps, and do not perform actions or operations that are likely to generate static electricity.
- Anti-static equipment (such as wrist straps and finger cots, etc.) should be tested regularly to ensure that they are properly
- Qualified anti-static facilities are used.
- Devices should be stored in containers made of conductive materials (such as special boxes for integrated circuits).
- Avoid using plastics, rubber or silk fabrics that may cause static electricity during use and transportation.
- Ensure the relative temperature and humidity in the anti-static work area.
- Use strictly in accordance with the recommended operating conditions. Using this product beyond the absolute maximum ratings may cause this

- Permanent damage to the product.
- If the system is used in situations with high temperature changes and vibration requirements, it is recommended to take reinforcement measures for the circuit.
- To improve its ability to resist mechanical vibration and thermal stress.

IX. Illustrate

9 Contact Details

Company Name: Beijing Star electronic technology Co. Ltd.

Address: Room 0806,7th Floor, No.9 Dongsanhuan Zhonglu, Chaoyang District, Beijing China.

- District Phone: +8613121851419
- Website: <https://beijing-est.cn/> e-mail: sales@beijing-est.cn

X. Disclaimer:

Our institute is only responsible for the current validity of this product manual when it is issued, and will not notify you of any version update.

For the latest information about this product, please refer to 9.2 Please contact us via the contact information in the article for consultation.

All technical information contained in this product manual is only for users to gain a preliminary understanding of this product.

If there is any discrepancy with the product detailed specifications, the product detailed specifications shall prevail.

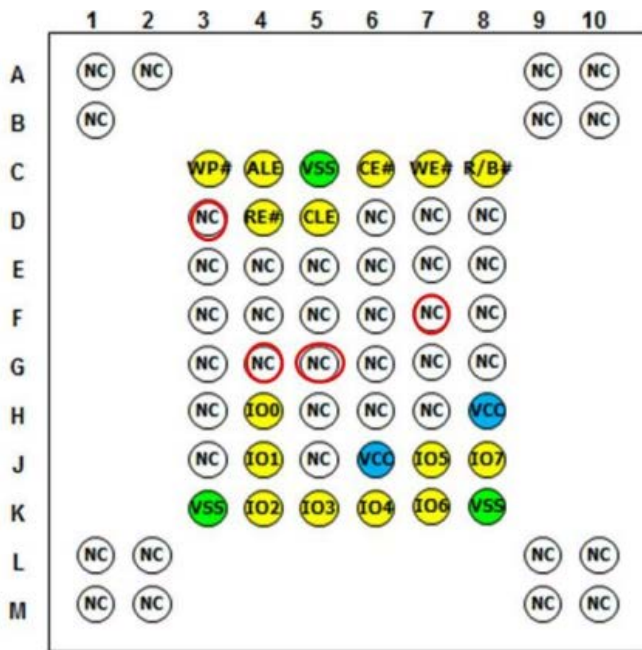
XI. AppendixA

Pin definition compared with Micron products.

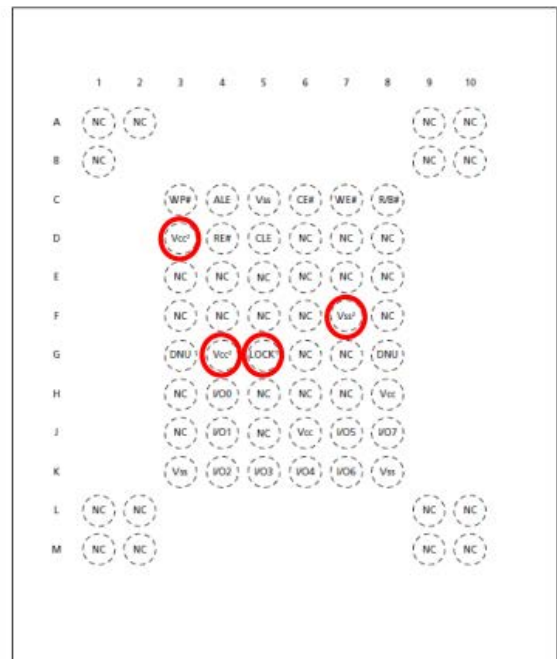
The pin definition of this product is the same as that of Micron MT29F8G08ADBCAH4. The

comparison is shown in the figure A-1. As shown, two in D3, G4, G5 and F7. There are differences in the pins. Specifically:

- Micron products D3 and G4 for power supply VCC. Pin, domestically produce dNC;
- Micron products F7 for VSSL and, domestically produce dNC;
- Micron products G5 for lock function, domestic products do not have this function, NC.



(a) Pin definition of domestic products;



(b) Micron product pin definition

Picture A-1. Pin definition and Micron MT29F8G08ADBCAH4 contrast