BSTM88512-55CB

Static Memory

Military Product Manual

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I. Product Introduction

1.1. Product Overview

BSTM88512-55CBIs a low power asynchronous single chip SRAM, the storage capacity is512K×8bits, and the access time is55ns.

Device Adoption8Bidirectional data port, can read and write8bit data. Input and output compatible TTL Level.

1.2. Product Features

The main technical indicators are as follows:

- Operating Voltage:5V±0.5V
- Storage capacity:4Mbit（512k×8bit）
- Reading speed: ≤55ns
- Input high level: ≥2.2V
- Input low level: ≤0.8V
- -Package:CDIP32
- Operating temperature: -55℃～ +125℃

- Storage temperature: -65℃～ +150℃

1.3. Product use and application range

BSTM88512-55CBThis circuit is a4MAsynchronous single port SRAM, used as a high-speed cache with the master control device,

It is widely used in communication modules.

1.4. Corresponding to the situation of replacing foreign products

BSTM88512-55CBType static memory circuit and Microsemi Company EDI88512CA55CB Circuit compatible.

See the Appendix for parameter difference comparison1.

II. Product appearance

2.1. Product size

Device Adoption32leadDIPCeramic dual in-line package, dimensions as shown in the figure1regulations.

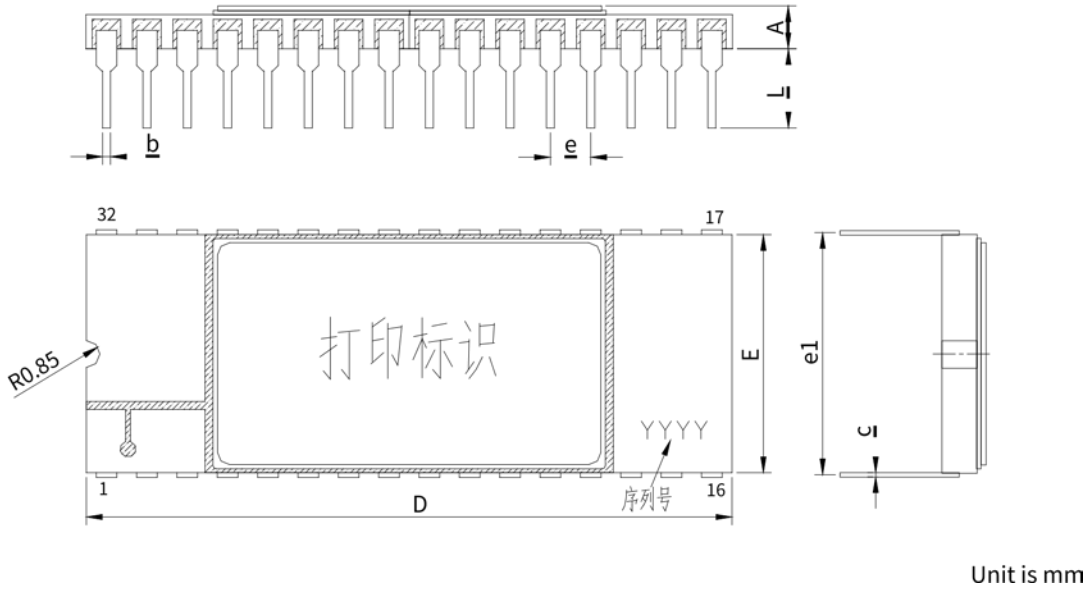
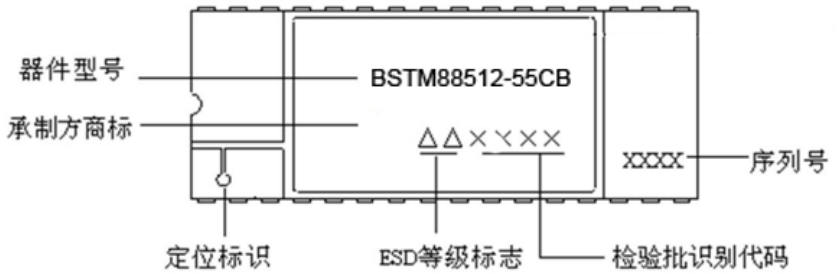


Figure 1. Dimensions

DIMENSION SYMBOLS	NUMBERVALUE		
	MINIMUM	NOMINAL	MAXIMUM
A	2.45	—	3.05
b	0.42	—	0.58
c	0.20	—	0.30
D	40.24	—	41.04
E	14.74	—	15.24
e	—	2.54	—
e1	—	15.24	—
L	4.50	—	5.50

2.2. Product photos and logo descriptions



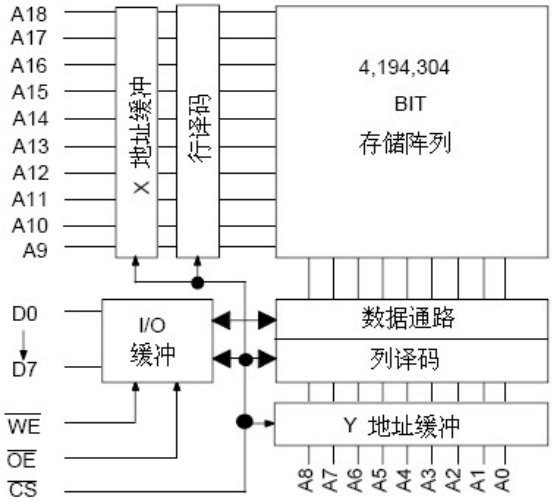
Picture 2. Device identification diagram

III. Standard Implementation

This product is in accordance with Q/FC 20925-2022 Semiconductor Integrated Circuits BSTM88512-55CB Type Static Memory Circuit All content meets the requirements GJB 597B-2012,GJB548B-2005The reliability assurance level meets the requirements of JB 597B-2012 RegulationsB Level requirements.

IV. Brief description of basic working principle

4.1. Circuit Function



Picture 3. Functional Block Diagram

The device is a low-power asynchronous single-chip SRAM, the storage capacity is512K×8bits, and the access time is55nsIt uses

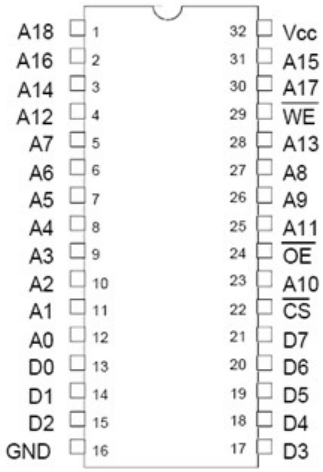
8Bidirectional data pin, can read and write8bit data. Its input and output levels are TTL Level compatible.

Truth Table

OE	CS	WE	WORKING MODE	OUTPUT
X	H	X	Low Power Mode	High resistance
H	L	H	Output Cancel	High resistance
L	L	H	Read Data	Data Output
X	L	L	Writing Data	Data Writing

4.2. Pin Description

The lead-out terminals should be arranged as shown in the figure4regulations.



Picture 4. Terminal arrangement diagram

PIN NUMBER	ACHIEVEMENTABLE	I/O	SYMBOL	PIN NUMBER	ACHIEVEMENTABL	I/O	SYMBOL
1		I	A18	17		I/O	D3
2		I	A16	18		I/O	D4
3		I	A14	19	Data Bus	I/O	D5
4		I	A12	20		I/O	D6
5		I	A7	21		I/O	D7
6	Address Bus	I	A6	22	Chip Select	I	$\overline{CS}$
7		I	A5	23	Address Bus	I	A10
8		I	A4	24	Output Enable	I	$\overline{OE}$
9		I	A3	25	Address Bus	I	A11
10		I	A2	26		I	A9
11		I	A1	27	Address Bus	I	A8
12		I	A0	28		I	A13
13	Data Bus	I/O	D0	29	Write Enable	I	WE
14	Data Bus	I/O	D1	30	Address Bus	I	A17

15		I/O	D2	31	Address Bus	I	A15
16	land	GND	GND	32	power supply	VCC	VCC

V. Extreme working conditions and recommended working conditions

5.1.Extreme working conditions

Supply voltage (VDD…..0.5V~7V

Maximum power consumption (PD…..1W

Working power consumption (PD1…..350mW

Standby power consumption (PD2…..40mW

Storage temperature range (Tsj…..65℃～150℃

Maximum lead soldering temperature (Th） （10s)…..300℃

Maximum Junction Temperature (Tj…..175℃

5.2.Recommended operating conditions

Supply voltage (VDD…..4.5V~5.5V

Working environment temperature (TA…..55℃～125℃

VI. Main technical parameters

6.1. Electrical characteristics parameters

Table 2Electrical properties

CHARACTERISTIC	SYMBOL	STRIPITEM UNLESS OTHERWISE SPECIFIED VCC=5V	LIMIT VALUE		UNIT
			MINIMUM	MAXIMUM	
Standby Supply Current (TTL）	ISB1	-55℃≤T_A≤125℃ $\overline{CS}$≥V_{IH},V_{IN}≤V_{IL},V_{IN}≥V_{IH},V_{CC} =5.5V	—	60	mA

Full standby supply current	ISB2	CS≥VCC-0.2V,VIN≤0.2V or VIN≥VCC-0.2V,VCC=5.5V	—	25	mA
Input high level voltage	VIH	—	2.2	—	V
Input low level voltage	VIL	—	—	0.8	V
Input high level current	|ILI-H|	VCC=5.5V, VIH=5.5V	—	10	μA
Input low level current	|ILI-L|	VCC=5.5V, VIH=0V	—	10	μA
Output high level voltage	VOH	IOH=-4.0mA	2.4		V
Output low level voltage	VOL	IOL=6mA	—	0.4	V
Output high level leakage current	|ILO-H|	VCC=5.5V, CS=VIH VI/O=5.5V,OE=VIH,	—	10	μA
Output low level leakage current	|ILO-L|	V=CC5.5V,CS=VIH VI/O=0V,OE=VIH	—	10	μA
Working current	ICC	CS, WE=V,IILI/O=0mA, f=18MHz,VCC=5.5V	—	225	mA
Functional testing		f=18MHz, VCC=4.5V,5V,5.5V	—	—	—
		Read Timing			
Read Cycle	tRC	See picture5	55	—	ns
Address access time	tAA	See picture5	—	55	ns
Chip select to output data valid time	tACS	See picture5	—	55	ns
Chip select to output low high impedance effective time	tCLZ	See picture5	3	—	ns
Data hold time after address change	tOH	See picture5	0	—	ns
Output enable to data output valid time	tOE	See picture5	—	30	ns
Output enable to output low high impedance effective time	tOLZ	See picture5	0	—	ns

Write Timing					
Write cycle	tWC	See picture6, picture7	55	—	ns
Chip select to write end time	tCW	See picture6, picture7	—	50	ns
Address creation time	tAS	See picture6, picture7	0	—	ns
Address valid to write end time	tAW	See picture6, picture7	—	50	ns
Write pulse width	tWP	See picture6, picture7	—	45	ns
Write recovery time	tWR	See picture6, picture7	0	—	ns
Data retention time	tDH	See picture6, picture7	0	—	ns
Write to output high impedance time	tWlZ	See picture6, picture7	0	30	ns
Data to write end time	tDW	See picture6	—	30	ns
	tDW	See picture7	—	40	ns

VII. Application Guide

7.1. Key parameter timing diagram/typical application peripherals

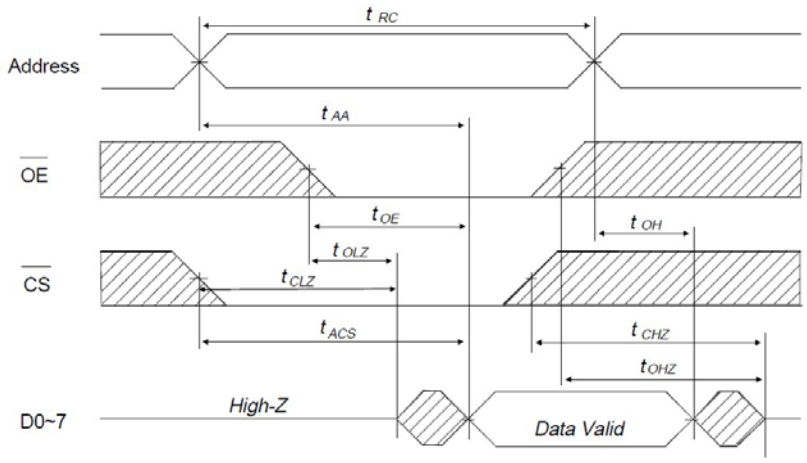


Figure 5. Read circle

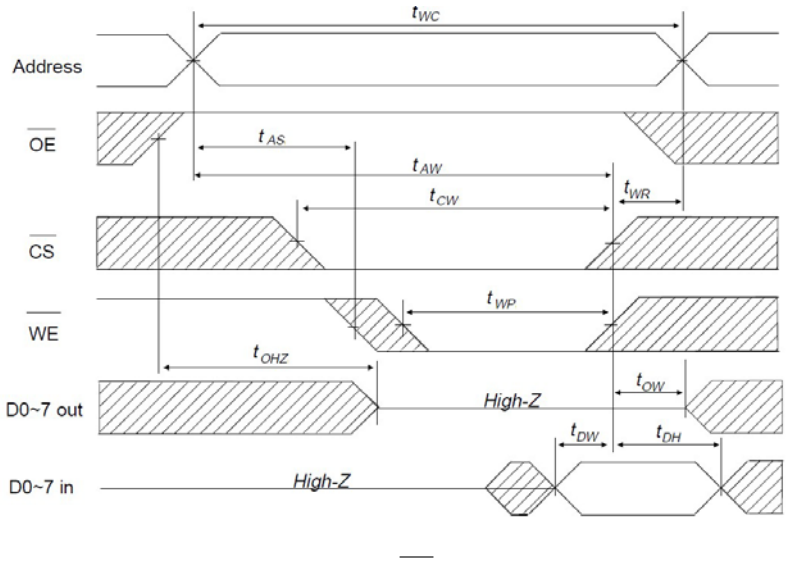


Figure 6 Write cycle 1 (CScontrol)

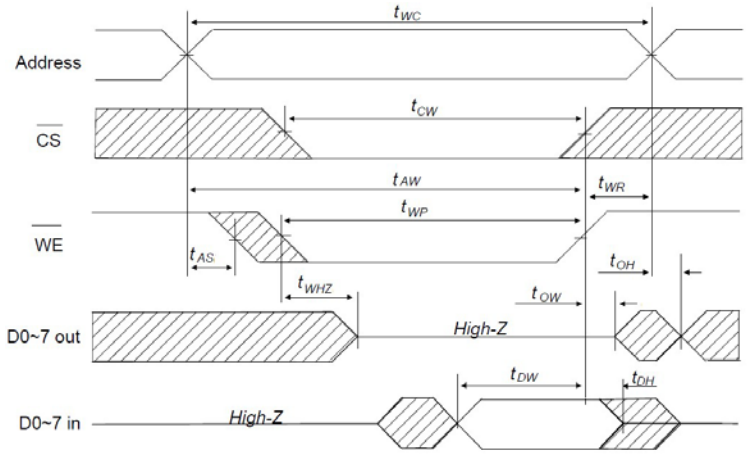


Figure 7. Write cycle 2 (VE control)

7.2. ESD characteristic

ESDThe levels are:2class,2000V 7.3

Radiation resistance none

7.4. Identification and diagnosis of common problems

This product is a static random access memory. The device data is uncertain after power-on and should not be used directly for certain deterministic data reading.

After power-on, the data writing operation should be performed, and the device reads data and verifies it based on the written data.

VIII. Precautions

8.1. Product transportation and storage precautions

The chip storage environment temperature is: -65℃～+150℃Use designated anti-static packaging boxes to package and transport products.

During transportation, ensure that the chip does not collide with foreign objects. This product should be placed in an air-conditioned environment with temperature and humidity control.

In an environment to prevent the pins from being oxidized due to long-term storage, which will affect solderability.

8.2. Product unpacking and inspection

When unpacking and using the chip, please pay attention to the product logo on the chip shell. Make sure the product logo is clear, without stains, or scratches.

At the same time, pay attention to check the chip shell and pins. Make sure the shell is not damaged, without scratches, and the pins are neat, not missing, and not deformed.

8.3. Circuit Operation Precautions

This product is an electrostatic sensitive device and should be installed in strict accordance with the electrostatic sensitive device operating requirements specified in relevant national standards and operation.

During the installation of this product, it is forbidden to touch or weld this type of product without tools such as anti-static wrist straps. Bare hands are not allowed to touch the external leads of the product.

Installation and use must be in an anti-static work area (equipped with an anti-static workbench, tables and chairs, etc.) equipped with an ion fan and operate within the

effective range of the ion blower.

Operators must receive anti-static training and wear anti-static work clothes (including anti-static gloves or finger cots, hats, work

Wear anti-static shoes and an anti-static wrist strap) and avoid any actions or operations that may easily generate static electricity.

The anti-static equipment (such as wrist straps and finger cots, etc.) should be tested regularly to ensure that qualified equipment is used before each use.

Anti-static facilities.

Devices should be stored in containers made of conductive materials (e.g., special boxes for integrated circuits).

Avoid using plastic, rubber or silk fabrics that may cause static electricity during transportation.

Ensure the relative temperature and humidity in the anti-static work area.

Use strictly in accordance with the recommended operating conditions. Using this product beyond the absolute maximum ratings may cause permanent damage to the product. bad.

If the system is used in an environment with high temperature and vibration requirements, it is recommended to take reinforcement measures on the circuit to improve its resistance to mechanical changes.

Ability to withstand mechanical vibration and thermal stress.

IX. Illustrate

9. Contact Details

Company Name: Beijing Star electronic technology Co. ltd.

Address: Room 0806,7th Floor, No.9 Dongsanhuan Zhonglu, Chaoyang District, Beijing China.

- District Phone: +8613121851419

- Website: https://beijing-est.cn/ e-mail: sales@beijing-est.cn

X. Disclaimer:

We are only responsible for the current validity of this product manual when it is issued, and we will not notify you of any version update.

For the latest information, please contact us using the contact information in Article 9.2.

All technical information contained in this product manual is only for users to have a preliminary understanding of this product.

If there is any discrepancy between the product detailed specifications, the product detailed specifications shall prevail.

XI. Appendix Parameter Comparison Table

Table 1. BSTM88512-55CBDetailed specifications andMicrosemicompanyEDI88512CA55CBDifference comparison table

	SYMBOL	FOREIGN PARAMETERS		SPECIFICATION PARAMETERS		UNIT	IN CONCLUSION
		MINIMUM	MAXIMUM	MINIMUM	MAXIMUM		
Standby Supply Current (TTL)	ISB1	—	60	—	characteristic	mA	same
Full standby supply current	ISB2	—	25	—	25	mA	same
Input high level voltage	VIH	2.2	—	2.2	—	V	same
Input low level voltage	VIL	—	0.8	—	0.8	V	same
Input high level current	|ILI-H|	—	10	—	10	μA	same
Input low level current	|ILI-L|	—	10	—	10	μA	same
Output high level voltage	VOH	2.4		2.4		V	same
Output low level voltage	VOL	—	0.4	—	0.4	V	same
Output high level leakage current	|ILO-H|	—	10	—	10	μA	same
Output low level leakage current	|ILO-L|	—	10	—	10	μA	same

Working current	ICC	—	225	—	225	mA	same
Read Cycle	tRC	55	—	55	—	ns	same
Address access time	tAA	—	55	—	55	ns	same
Output enable to data output valid time	tOE	—	30	—	30	ns	same
Write pulse width	tWP	—	45	—	45	ns	same
Write cycle	tWC	55	—	55	—	ns	same
Chip select to output data valid time	tACS	—	55	—	55	ns	same
Data hold time after address change	tOH	0	—	0	—	ns	same
Chip select to output low high impedance effective time	tCLZ	3	—	3	—	ns	same
Output enable to output low high impedance effective time	tOLZ	0	—	0	—	ns	same
Chip select to output high impedance	tZGar	0	20	0	20	ns	same

effective time							
Output enable to output high impedance effective time	tOHZ	0	20	0	20	ns	same
Chip select to write end time	tCW	—	50	—	50	ns	same
Address valid to write end time	tAW	—	50	—	50	ns	same
Address creation time	tAS	0	—	0	—	ns	same
Write recovery time	tWR	0	—	0	—	ns	same
Data retention time	tDH	0	—	0	—	ns	same
Write to output high impedance time	tWlZ	0	30	0	30	ns	same
Data to write end time	tDW	—	40	—	40	ns	same
	tDW	—	30	—	30	ns	same
Output valid until writing is completed	tWlq	0	—	0	—	ns	same