

BSTM7C185 type
8K×8bit asynchronous SRAM Circuit
Military Product Manual

Table of contents

- Product Introduction
 - Product Overview
 - Features
 - Product use and application range
 - Corresponding replacement of foreign products.
- Product appearance
 - Product Dimensions
 - Weight
 - Packaging process
 - Product Photos and Logo Descriptions
- Quality Assurance Level
- Brief description of basic working principle
 - Circuit Function Block Diagram
 - Package Pin Description....
- Extreme and recommended operating conditions
 - Extreme working conditions .Recommended operating conditions....
- Main technical parameters
 - Electrical characteristics parameters
- Application Guide.
 - Key parameter timing diagram/typical application peripherals
 - Circuit usage precautions

- Notes...
 - Product transportation and storage precautions
 - Product unpacking and inspection
 - Circuit Operation Precautions
- Illustrate.
 - After-sales service and guarantee
 - Contact information
 - Version and Disclaimer

I. Product Introduction

1.1. Product Overview

BSTM7C185It is a storage capacity of 8K×8bit Asynchronous timing single chip SRAM .The circuit consists of an address input buffer, Row decoding circuit, column decoding circuit, data input buffer, small signal readout amplifier, data output drive circuit, logic control

The circuit consists of a control module and a storage cell array. The memory can be expanded through chip select signals and tri-state output drivers.

Chip select signal CE and three-state output drivers to achieve memory expansion.

1.2. Features

- With CYPRESS Company CY7C185-45 Type circuit compatible
- Power supply voltage: 5V
- Access time: 45ns
- Dynamic power consumption: ≤ 715mW
- Static power consumption: ≤ 220mW
- Operating temperature: -55℃~125℃
- Packaging form: CDIP28

1.3. Product use and application range

It is widely used in aviation, ships, ground weapons and other systems.

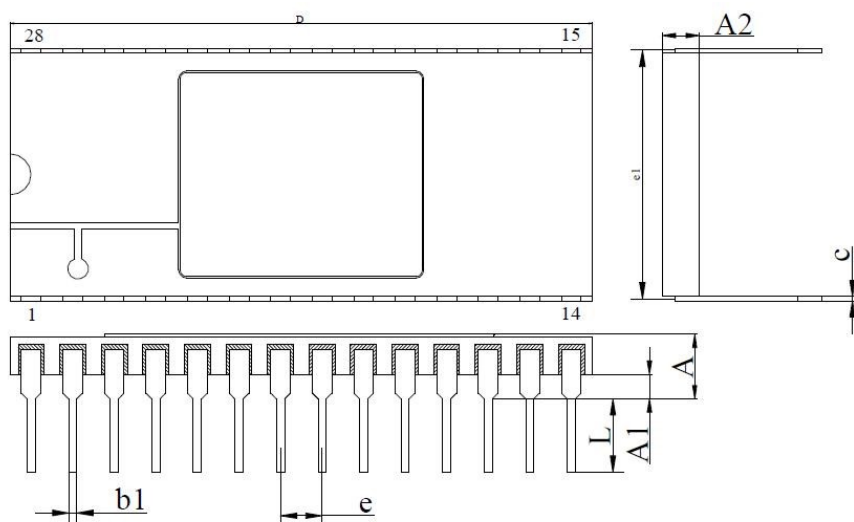
1.4. Corresponding to the situation of replacing foreign products

Benchmarking CYPRESS Company CY7C185-45 Type circuit.

II. Product appearance

2.1. Product size

BSTM7C185 type 8k×8Bit SRAM Circuit adopted 28Leaded Ceramic Double Row (DIP28) package, the circuit dimensions are as follows picture1 shown.



Picture 1. Dimensions

DIMENSION SYMBOLS	NUMERICMM		
	MINIMUM	NOMINAL	MAXIMUM
A	—	—	5.10
A1	0.51	—	—
b1	0.35	—	0.59
c	0.20	—	0.36
e	—	2.54	—
e1	—	7.62	—
L	2.54	—	5.00
Z	—	—	2.54
D	—	—	38.10

2.2. Weight

The device weight is $2.7 \pm 0.1\text{g}$.

2.3. Packaging process

Device Adoption $0.8\mu\text{m}$ CMOS Process structure: The capping process is gold-tin alloy capping process; the marking is made by metal ink pad printing Craftsmanship.

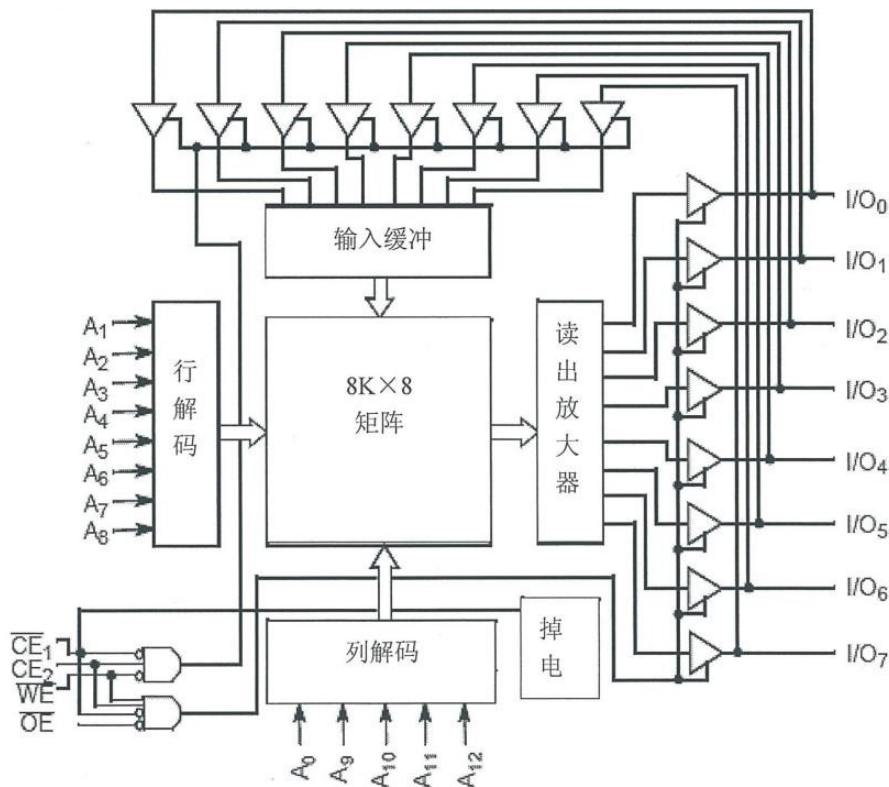
III. Quality Assurance Level

The product quality grade is GJB 597A-1996 Regulations B1 Level 1 execution, assessment standards meet Q/FC 20145-2005 Semiconductor Integrated

Circuits BSTM7C185 Static Random Access Memory Circuit Detailed Specifications" requirements.

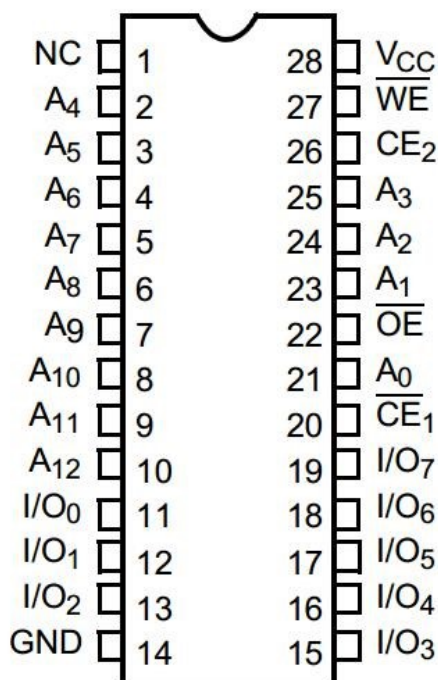
IV. Brief description of basic working principle

4.1. Circuit Function Block Diagram



Picture 3. Circuit Function Block Diagram

4.2. Package Pin Description



Picture 4. Pin Assignment Diagram

Table 1. Pin Assignment Diagram

Serial number	symbol	Function	Serial number	symbol	Function
1	NC	Empty feet	28	VCC	power supply
2	A4	Address input	27	WE	Write enable, low effective
3	A5	Address input	26	CE2	Chip select signal, high effective
4	A6	Address input	25	A3	Address input
5	A7	Address input	24	A2	Address input
6	A8	Address input	23	A1	Address input
7	A9	Address input	22	OE	Output enable, low effective
8	A10	Address input	21	A0	Address input
9	A11	Address input	20	CE1	Chip select signal, low

					effective
10	A12	Address input	19	I/O7	Data Input/Output
11	I/O0	Data Input/Output	18	I/O6	Data Input/Output
12	I/O1	Data Input/Output	17	I/O5	Data Input/Output
13	I/O2	Data Input/Output	16	I/O4	Data Input/Output
14	GND	land	15	I/O3	Data Input/Output

V. Extreme working conditions and recommended working conditions

5.1. Extreme working conditions

Table 2. Extreme working conditions

PROJECT	EXTREME WORKING CONDITIONS
Supply voltage (VCC)	-0.5V ~ +7.0V
Maximum power consumption (PD)	875mW
Storage temperature range (Tstg)	- 65°C~+150°C
Voltage (input)	(GND-0.5)V ~ + 7.0V

5.2. Recommended operating conditions

Table 3. Recommended operating conditions

PROJECT	RECOMMENDED OPERATING CONDITIONS
Supply voltage (VCC)	4.5V~5.5V
Working environment temperature (TA)	- 55°C~125°C
Input level voltage	4.5V~5.5V

VI. Main technical parameters

6.1. Electrical characteristics parameters

Table 4. Electrical characteristics parameter table

SPECIAL SEX	SYM BOL	STRIP TEM UNLESS OTHERWISE SPECIFIED $V_{CC}=5V$ $-55^{\circ}C \leq T_A \leq 125^{\circ}C$	LIMIT VALUE		UNIT
			MINIM UM	MAXI MUM	
Input high level voltage	V_{IH}		2.2	—	V
Input low level voltage	V_{IL}		—	0.8	V
Output high level voltage	V_{OH}	$I_{OH}=-4mA$	2.4	—	V
Output low level voltage	V_{OL}	$I_{OL}=8mA$	—	0.4	V
Input high level leakage current	I_{IH}	$V_I=5.0V$	- 10	10	μA
Input low level leakage current	I_{IL}	$V_I=0V$	- 10	10	μA
Output high level leakage current	I_{OZ}	$V_{OH}=5.0V$	- 10	10	μA
Output low level leakage current	I_{OZL}	$V_{OL}=0V$	- 10	10	μA
Quiescent Current1	ISB1	$V_{CC}=5.5V, CE > V_{IH}$	—	30	mA

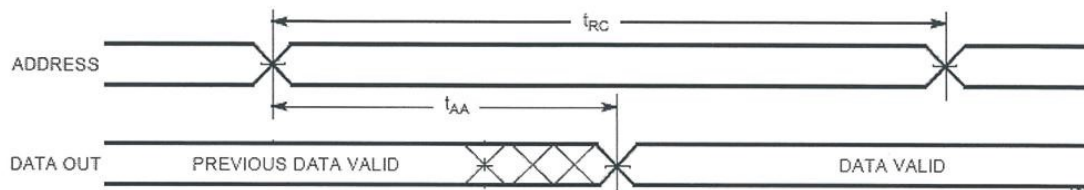
Quiescent Current ₂	ISB2	$V_{CC}=5.5V, CE > V_{CC}-0.3V$	—	20	mA
Dynamic supply current	IA	$V_{CC}=5.5V$	—	125	mA
Function Timing					
Data hold time after address change	tOHA	See picture6	3	—	ns
Chip Select1After valid until data is valid	tACE ₁	See picture7	—	45	ns
Chip Select1After valid until data is valid	tACE ₂	See picture7	—	30	ns
Read signal valid to data valid	tDOE	See picture7	—	20	ns
Read signal valid to low impedance	tLZO _E	See picture7	3	—	ns
Read signal invalid to high impedance	tHZD	See picture7	—	15	ns
Chip Select1Effective to low resistance	tLZC _{E1}	See picture7	5	—	ns

Chip Select2Effective to low resistance	tLZCE2	See picture7	3	—	ns
Chip Select1(Chip Select2) Invalid to high impedance	tHZD	See picture7	—	15	ns
Chip Select1Valid until power on	tPU	See picture	0		ns
1		7 —		25	
		8,9	40	—	
1		8,9	30	—	
2		8,9	30	—	
		8,9	30	—	
		Chip Select Invalid to power off t_{PD} See picture Write cycle t_{WC} See picture Chip Select Valid until the end of writing t_{SCE1} See picture Chip Select Valid until the end of writing t_{SCE2} See picture Address setup to write completion t_{AW} See picture After writing, the address is kept t_{HA} See picture Address Setup to Write Start t_S See picture Write signal pulse width t_{PWE} See picture Data creation to write completion t_{SD} See picture After writing, data is retained t_{HD} See picture	0	—	
		8,9			
		8,9	0	—	
		8,9	20	—	
		8,9	15	—	
		8,9	0	—	

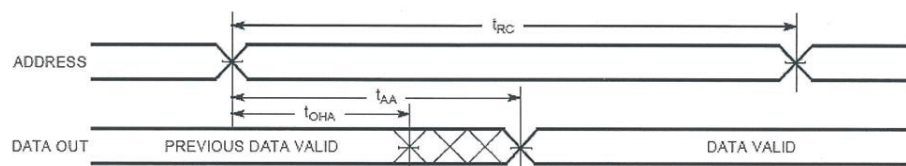
Write signal valid to high impedanc e	t _{HZW} E	See picture8	5	—	ns
Write signal invalid to low impedanc e	t _{LZW}	See picture8	—	15	ns
a)Function timing see figure6,picture7,picture8,picture9					

VII. Application Guide

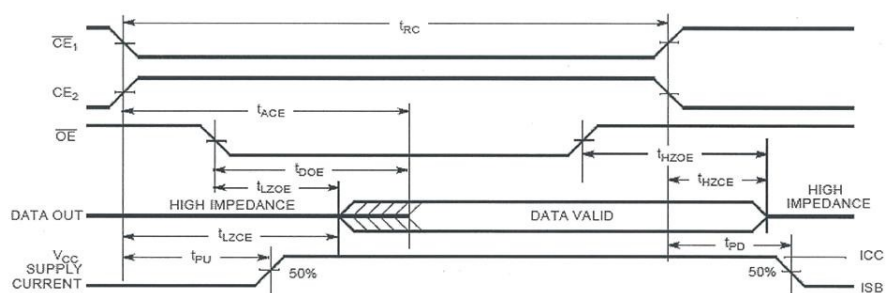
7.1. Key parameter timing diagram/typical application peripherals



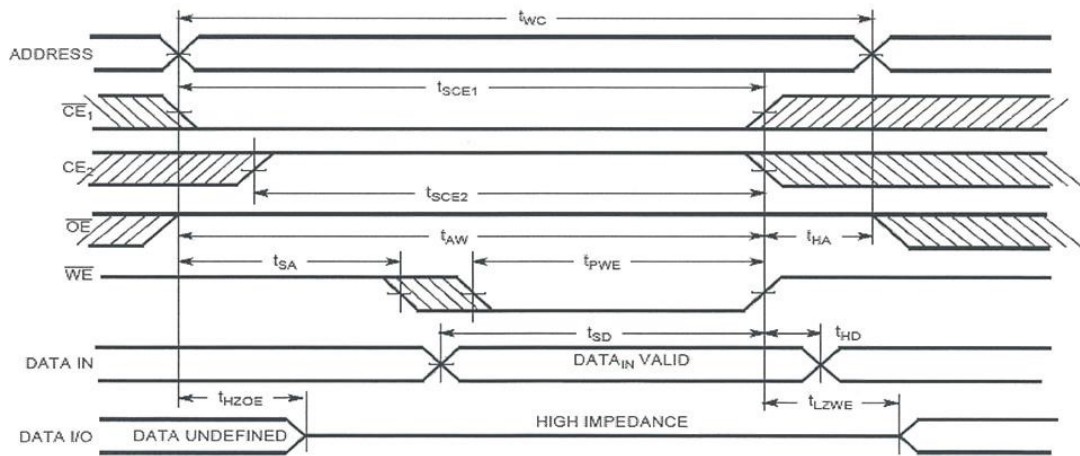
Picture 5. AC Characteristics Timing Diagram



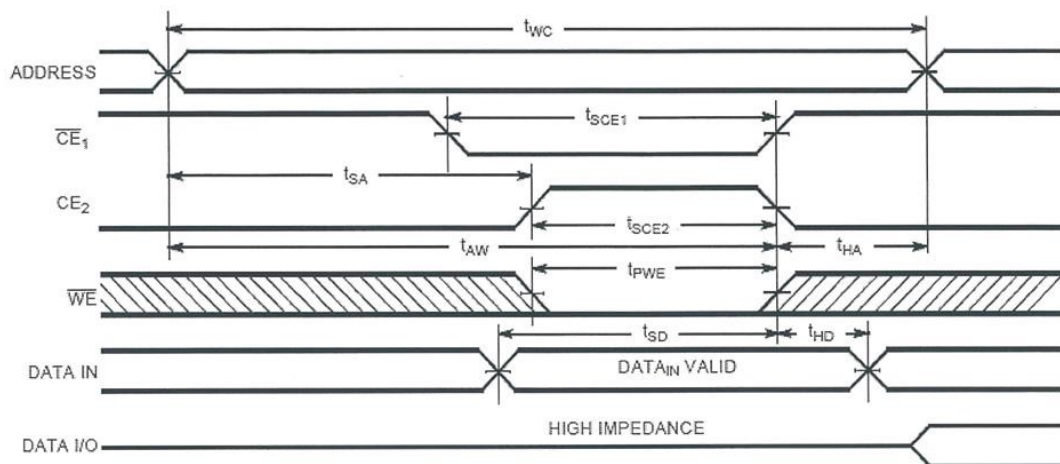
Picture 6. Functional timing diagram



Picture 7. Functional timing diagram



Picture 8. Functional timing diagram



Picture 9. Functional timing diagram

7.2. Circuit usage precautions

If a fault occurs during product use, it is recommended to use the following methods to troubleshoot:

- Check whether the power supply voltage of the product on the board meets the requirements;
- Check whether the output level of the output terminal of the interface device on the board meets the input signal level of the product.
- Require;
- Check whether the input signal in the working mode of this product meets the timing requirements;

If there is still no correct output signal, please confirm whether the product has been burned out. This product contains ESD Protective structure, anti Protection capacity exceeds 2kV (HBM), but the possibility of damage to the product by electrostatic discharge cannot be ruled out. Both the input and output ports are Easily damaged by electrostatic discharge. If the above methods still cannot eliminate the problem, please contact the development and production unit immediately.

VIII. Precautions

8.1. Product transportation and storage precautions

The product storage environment temperature is: -65°C To +150°C. Use the designated anti-static packaging box to package and transport the product. During transportation, ensure that the product does not collide with foreign objects. This product should be placed in an air-conditioned environment with temperature and humidity control to prevent the pins from oxidizing due to long-term storage, which will affect solderability.

8.2. Product unpacking and inspection

When unpacking the product, please pay attention to the product logo on the shell. Make sure the product logo is clear, without stains or scratches. At the same time, pay attention to check the product shell and pins. Make sure the shell is not damaged or scratched, and the pins are neat, not missing, and not deformed.

8.3. Circuit Operation Notes

This product is an electrostatic sensitive device and should be installed and operated in strict accordance with the operating requirements for electrostatic sensitive devices specified in relevant national standards.

During the installation of this product, it is forbidden to touch or weld this type of product without an anti-static wrist strap or other tools. The bare hands are not allowed to touch the external leads of the product.

Installation and use must be in an anti-static work area (equipped with an anti-static workbench, tables and chairs, etc.), equipped with an ion fan and operated within the effective range of the ion fan.

Operators must undergo anti-static training, wear anti-static work clothes (including anti-static gloves or finger cots, hats, work shoes and anti-static wrist straps), and avoid performing actions or operations that are likely to generate static electricity.

The anti-static equipment (such as wrist straps and finger cots, etc.) should be tested regularly to ensure that qualified anti-static equipment is used before each use.

Devices should be stored in containers made of static dissipative materials (e.g., special boxes for integrated circuits). Plastics, rubber, or silk fabrics that cause static electricity should be avoided during production, testing, use, and transportation.

Ensure the relative temperature and humidity in the anti-static work area.

9. Contact Details

Company Name: Beijing Star electronic technology Co. Ltd.

Address: Room 0806, 7th Floor, No.9 Dongsanhuan Zhonglu, Chaoyang District, Beijing China.

- District Phone: +8613121851419
- Website: <https://beijing-est.cn/> e-mail: sales@beijing-est.cn

X. Disclaimer

We are only responsible for the current validity of this product manual at the time of issuance, and will not notify you of version updates. If you need to know the latest information about this product, please refer to 9.2. Please contact us via the contact information in the article for consultation.

XI. Page

All technical information contained in this product manual is only for users to have a preliminary understanding of this product. If there is any discrepancy with the detailed product specifications, the detailed product specifications shall prevail.