BSTLN172-0618S

6-18GHz low-noise amplifier chip

Data Sheet

I. Product Introduction

BSTLN172-0618S is a low noise amplifier chip with excellent performance. The frequency range covers 6~18GHz, VD = +3.5V/+4V. At VD = +3.5V, the small signal gain is 20.5dB, the noise figure is 1.3dB, and the output 1dB compression power is 17.5dBm. This amplifier is housed in a 3×3mm surface-mount leadless plastic package. The lead pads are tin-plated, making it suitable for reflow soldering.

II. Key Technical Indicators

- Frequency range: 6-18GHz
- Small signal gain: 20.5dB
- Output 1dB compression power: 17.5dBm
- Noise figure: 1.3dB
- Input return loss: 13dB
- Output return loss: 17dB
- Power supply: +3.5V@95mA
- Chip size: 3.00mm × 3.00mm × 0.75mm

III. Functional Block Diagram

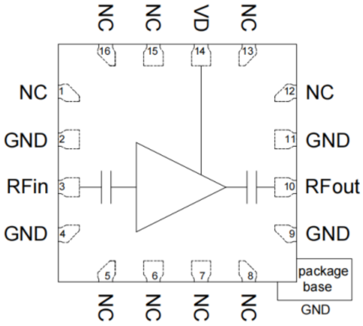


Figure 1.

IV. Electrical Performance Table (T_A = +25°C, V_D = +3.5V)

Table 1.

PARAMETER NAME	SYMBOL	MINIMUM	TYPICAL VALUES	MAXIMUM	UNIT
Frequency range	Freq	6	—	18	GHz
Small signal gain	Gain	20	20.5	—	dB
Noise Figure	NF	—	1.3	1.6	dB
Output 1dB compression power	OP1dB	16	17.5	—	dBm
Input return loss	RL_IN	10	13	—	dB
Output return loss	RL_OUT	11	17	—	dB
Quiescent operating current	IDQ	—	95	—	mA

V. Absolute Maximum Ratings

Table 2.

PARAMETER	LIMIT VALUE
Maximum operating voltage	+4V
Maximum input power	+20dBm
Storage temperature	-65℃ ~ +150℃
Operating temperature	-55℃ ~ +125℃

VI. Test curve (V_D=+3.5V)

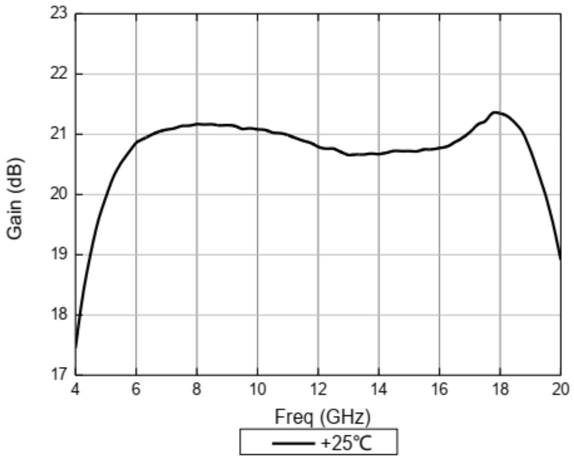


Figure 2. Small signal gain

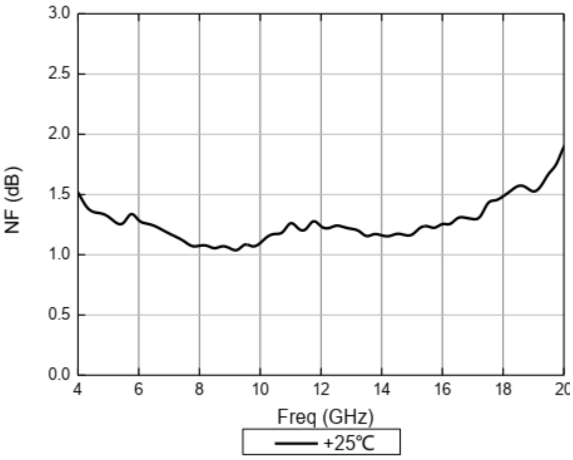


Figure 3. Noise Figure

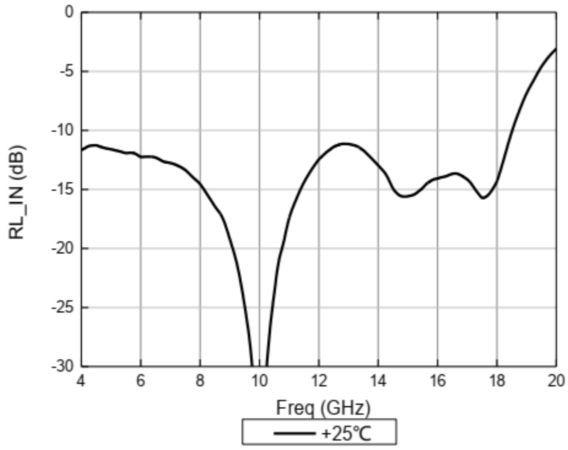


Figure 4. Input return loss

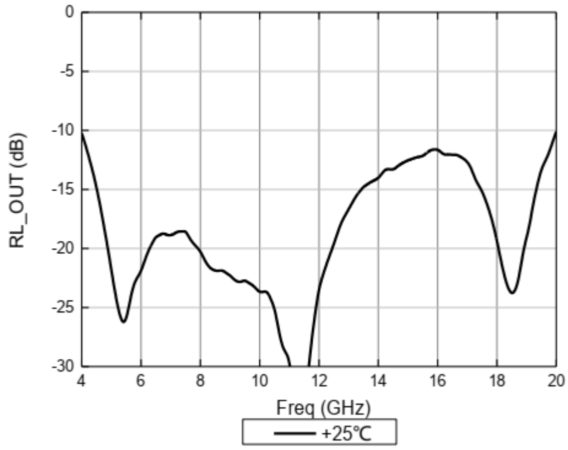


Figure 5. Output return loss

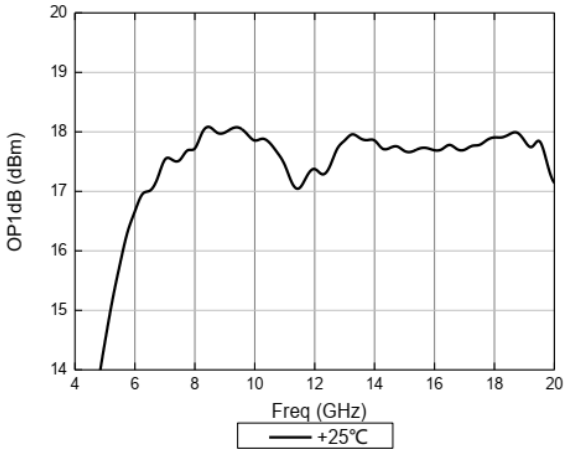


Figure 6. Output 1dB compression power

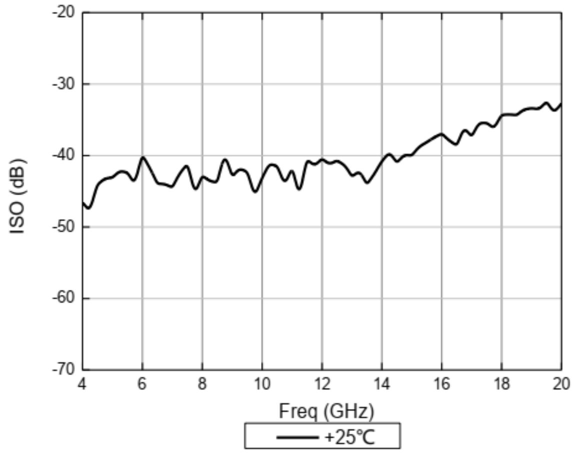
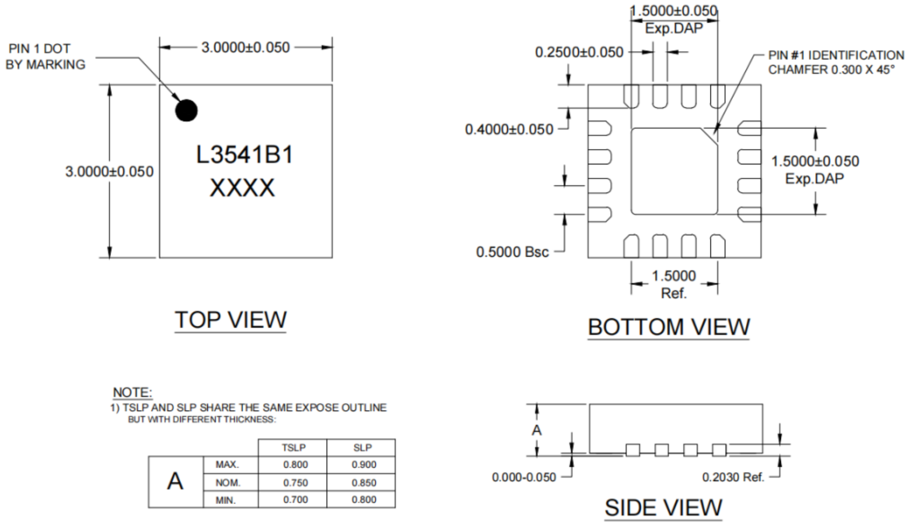


Figure 7. Reverse isolation

VII. Appearance Structure Diagram (unit: mm)



NOTE:
1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS:

		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

Figure 8.

VIII. Port Definition

Table 3.

SERIAL NUMBER	PORT NAME	DEFINITION	SIGNAL OR VOLTAGE
3	RFin	RF signal input terminal, no external DC blocking capacitor required	RF
10	RFout	RF signal output terminal, no external DC blocking capacitor required	RF
14	VD	LNA drain positive	+3.5V/+4V
2, 4, 9, 11, ePAD	GND	The bottom of the chip needs to be well grounded to RF and DC	/
other	NC	Suspended, recommended to be grounded	/

IX. Application Circuit

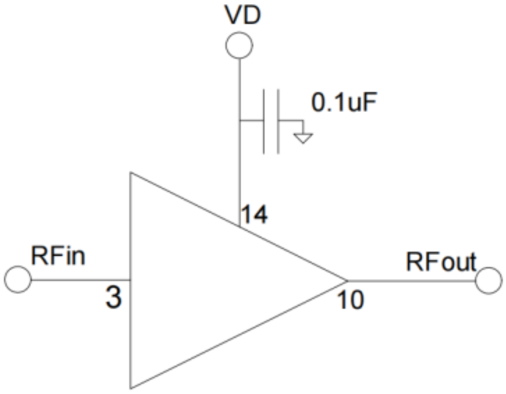


Figure 9.

X. Precautions

- Assemble and use in a clean environment;
- Sealing material: RoHS compliant low-pressure injection molding plastic;
- Lead frame material: copper alloy;
- Lead surface plating: 100% matte tin
- Maximum reflow peak temperature: 260 °C;
- This product is an electrostatic sensitive device, please be careful to prevent static electricity during storage and use;
- Store in a dry, nitrogen environment;
- Do not attempt to clean the chip surface with dry or wet chemical methods.