BSTLN150-0812

8-12GHz Low-Noise Amplifier Chip

Data Sheet

I. Product Introduction

BSTLN150-0812 is a high-performance low-noise amplifier chip with a frequency range of 8 to 12 GHz, a small-signal gain of 24 dB, a noise figure of 1.2 dB, and an output 1 dB compression power of 12 dBm.

The chip uses on-chip through-hole metallization technology to ensure good grounding, without the need for additional grounding measures, and is simple and convenient to use.

The back side is metallized and suitable for eutectic sintering or conductive adhesive bonding.

II. Key Technical Indicators

- Frequency range: 8-12GHz
- Small signal gain: 24dB
- Output 1dB compression power: 12dBm
- Noise figure: 1.2dB
- Input return loss: 25dB
- Output return loss: 14dB
- Power supply: +5V@27mA
- Chip size: 1.80mm × 1.10mm × 0.10mm

III. Functional Block Diagram

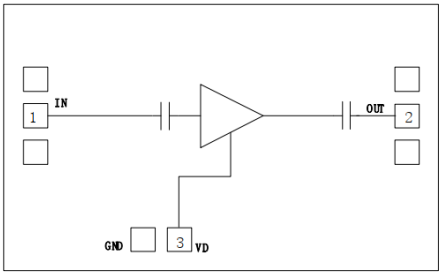

Figure 1.

IV. Electrical Performance Table (T_A = +25°C, VD = +5V)

Table 1.

PARAMETER NAME	SYMBOL	MINIMUM	TYPICAL VALUES	MAXIMUM	UNIT
Frequency range	Freq	8	—	12	GHz
Small signal gain	Gain	23.5	24	24.7	dB
Gain flatness	ΔG	—	±0.6	—	dB
Noise Figure	NF	0.9	1.2	1.4	dB
Output 1dB compression power	OP1dB	11.8	12	13	dBm
Input return loss	RL_IN	22	25	—	dB
Output return loss	RL_OUT	12	14	—	dB
Quiescent operating current	Id	—	27	—	mA

V. Absolute Maximum Ratings

Table 2.

PARAMETER	VALUE
Maximum operating voltage	+7V
Maximum input power	+20dBm
Storage temperature	-65℃ ~ +150℃
Operating temperature	-55℃ ~ +125℃

VI. Test curve (VD=+5V)

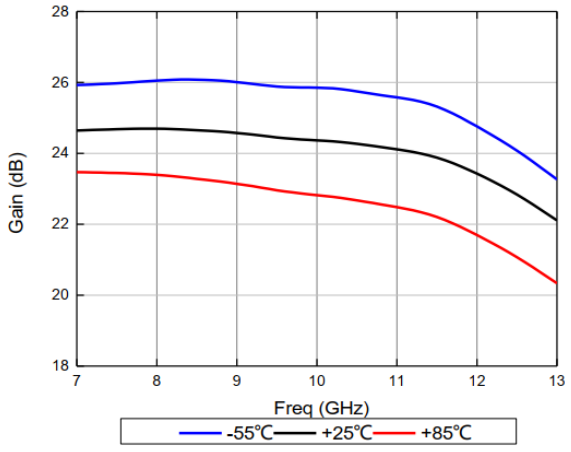

Figure 2. Small Signal Gain

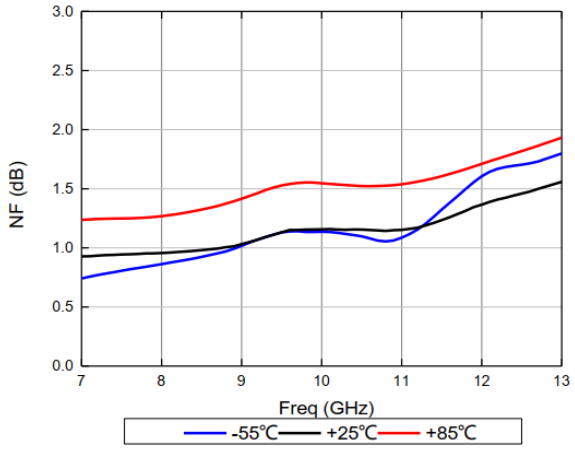

Figure 3. Noise Figure

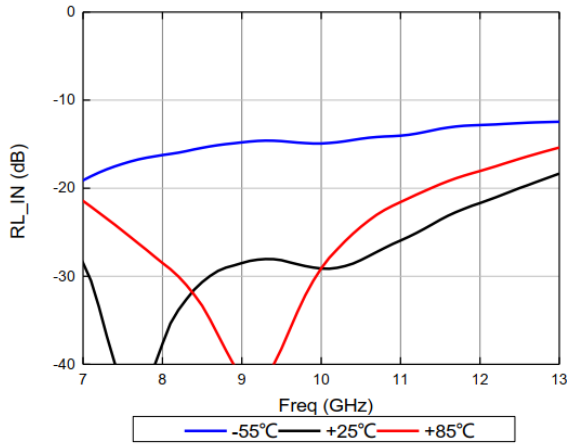

Figure 4. Input return loss

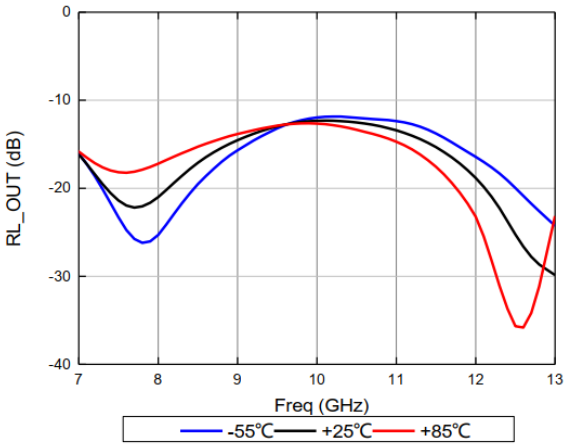

Figure 5. Output return loss

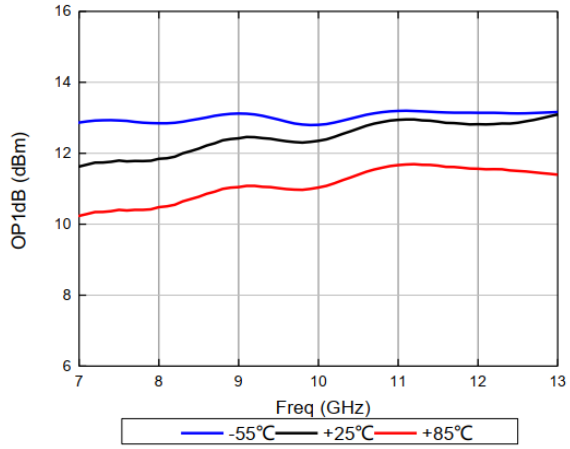

Figure 6. Output 1dB compression power

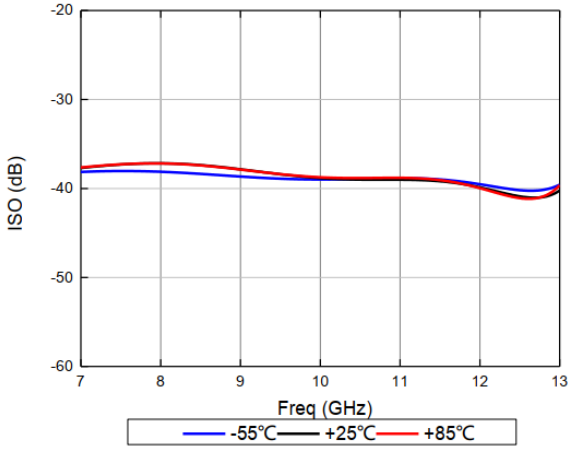

Figure 7. Isolation

VII. Chip port diagram (unit: μm)

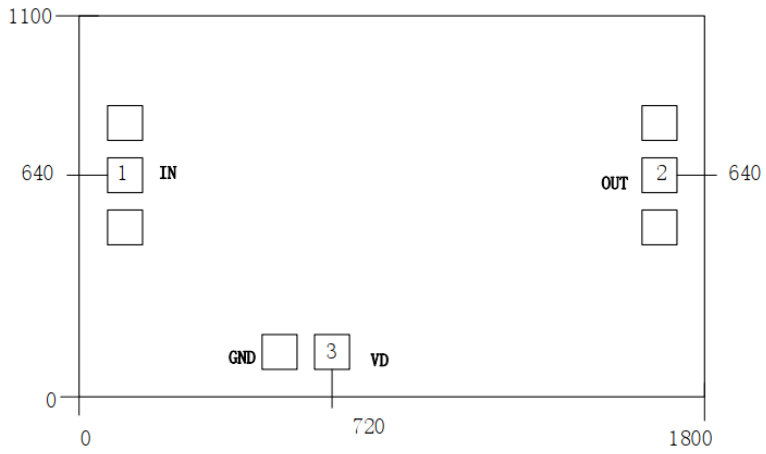

Figure 8.

VIII. Port Definition

Table 3.

SERIAL NUMBER	PORT NAME	DEFINITION	SIGNAL OR VOLTAGE
1	IN	RF signal input terminal, no external DC blocking capacitor required	RF
2	OUT	RF signal output terminal, no external DC blocking capacitor required	RF
3	VD	The LNA drain is positive, so it is recommended to add a 100pF or 1000pF capacitor.	+5V

IX. Recommended Assembly Drawing

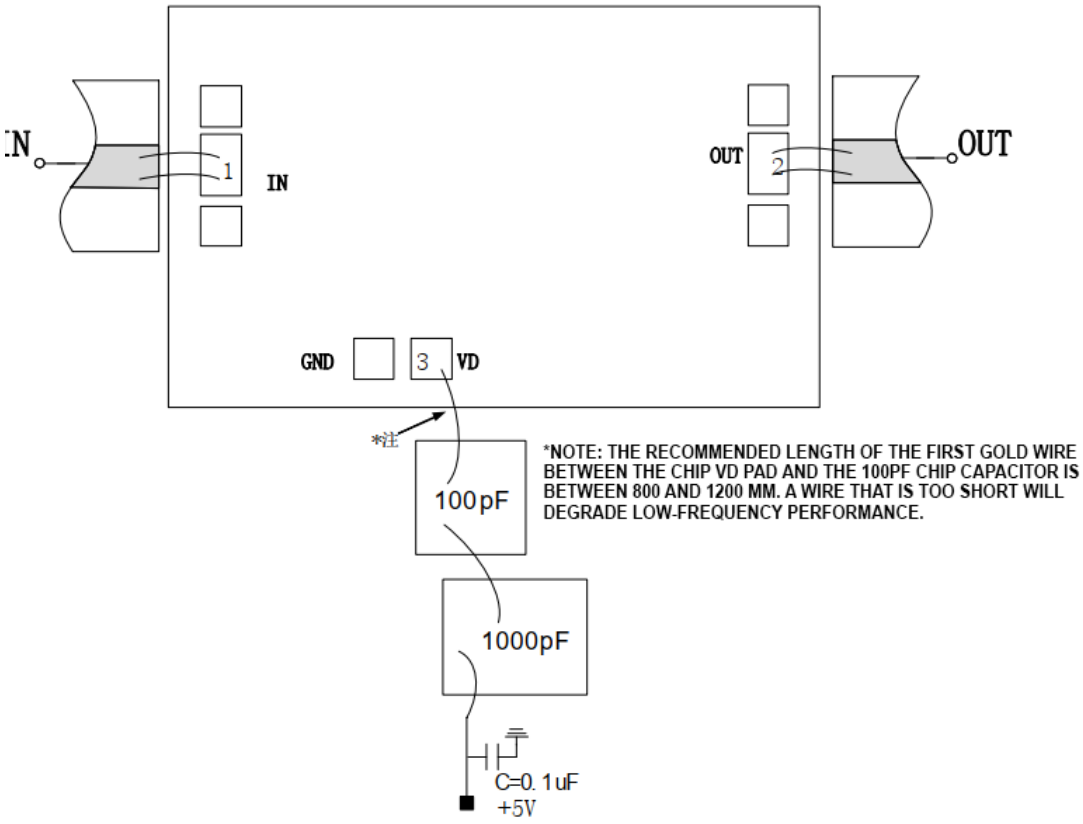

Figure 9.

X. Notes

- Assemble and use in a clean environment.
- GaAs material is very brittle and the chip surface is easily damaged (do not touch the surface), so you must be careful when using it.
- Use two bonding wires (25μm diameter gold wire) for input and output. Keep the bonding wires as short as possible and no longer than 300μm.
- The sintering temperature should not exceed 300℃ and the sintering time should be as short as possible, not exceeding 30 seconds.
- This product is an electrostatic sensitive device, please be careful to prevent static electricity during storage and use.
- Store in a dry, nitrogen environment.
- Do not attempt to clean the chip surface with dry or wet chemical methods.