BSTLN114-0713D

7-13GHz low-noise amplifier chip

I. Product Introduction

BSTLN114-0713D is a high-performance low-noise amplifier chip with a frequency range of 7 to 13 GHz, a small-signal gain of 27 dB, a noise figure of 0.7 dB, an output 1dB compression power of 13 dBm, a saturated output power of 14 dBm, and an output third-order intermodulation power of 23 dBm. This chip uses an on-chip through-hole metallization process to ensure good grounding, eliminating the need for additional grounding measures and making it easy to use.

The back side is metallized and suitable for eutectic sintering or conductive adhesive bonding.

II. Key technical indicators

- Frequency range: 7-13GHz
- Small signal gain: 27dB
- Output 1dB compression power: 13dBm
- Saturated output power: 14dBm
- Output third-order intermodulation power: 23dBm
- Noise figure: 0.7dB
- Input return loss: 15dB
- Output return loss: 13dB
- Power supply: +5V@34.7mA
- Chip size: 1.45mm × 1.00mm × 0.10mm Electrical

Table 1. Performance Table

PARAMETER NAME	SYMBOL	MINIMUM	TYPICAL VALUES	MAXIMUM	UNIT
Frequency range	Freq	7	—	13	GHz
Small signal gain	Gain	26.5	27	28	dB
Gain flatness	ΔG	—	±0.75	—	dB
Noise Figure	NF	—	0.7	0.8	dB

PARAMETER NAME	SYMBOL	MINIMUM	TYPICAL VALUES	MAXIMUM	UNIT
Output 1dB compression power	OP1dB	12	13	—	dBm
Saturated output power	Psat	13	14	—	dBm
Output third-order intermodulation power	OIP3	21	23	—	dBm
Input return loss	RL_IN	11	15	—	dB
Output return loss	RL_OUT	12	13	—	dB
Quiescent operating current	Id	—	34.7	—	mA

III. Functional Block Diagram

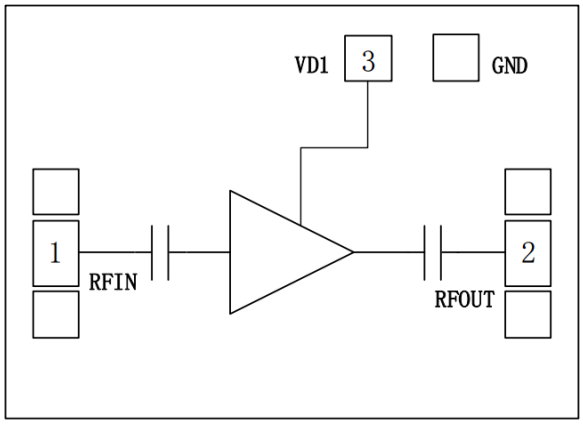

Figure 1. Functional Block Diagram

IV. Absolute Maximum Ratings

Table 2.

PARAMETER	VALUE
Maximum operating voltage	+7V
Maximum input power	+20dBm
Storage temperature	-65℃ ~ +150℃
Operating temperature	-55℃ ~ +125℃

V. Test curve (VD1=+5V)

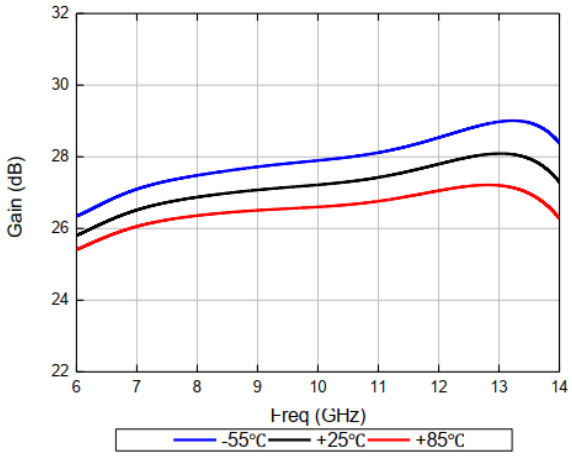

Figure 2. Small signal gain

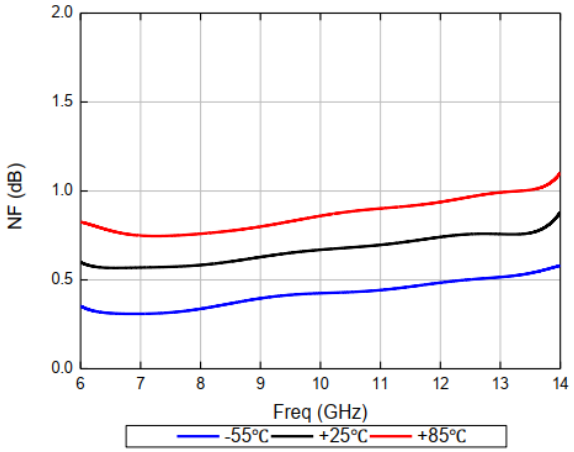

Figure 3. Noise Figure

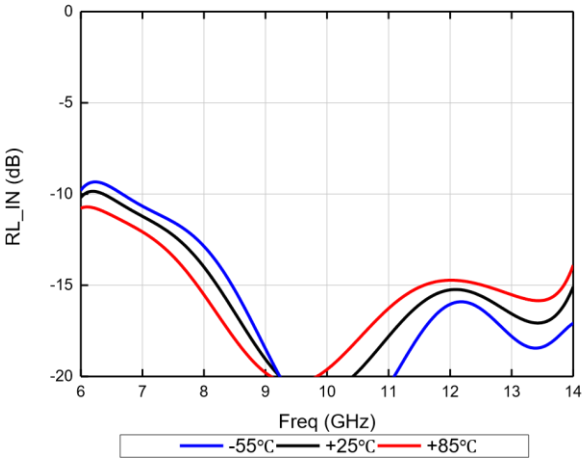

Figure 4. Input return loss

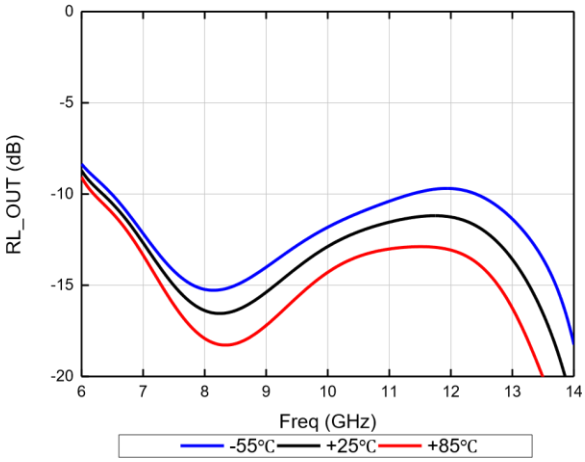

Figure 5. Output return loss

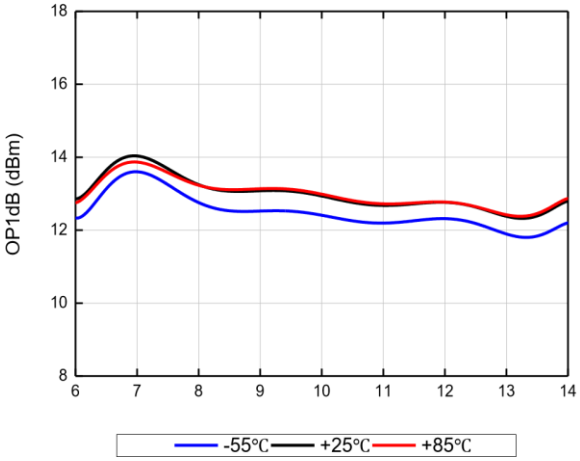

Figure 6. Output 1dB compression power

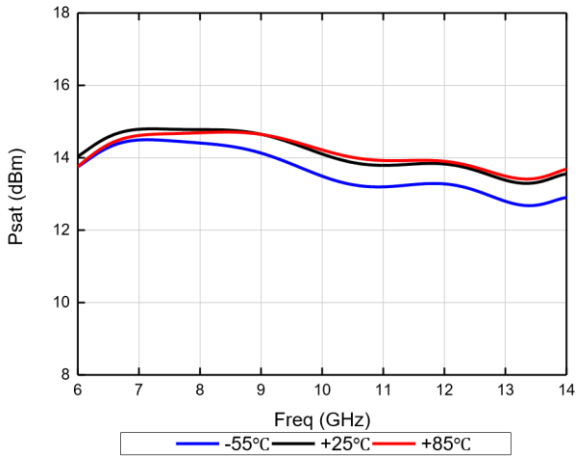

Figure 7. Saturated output power

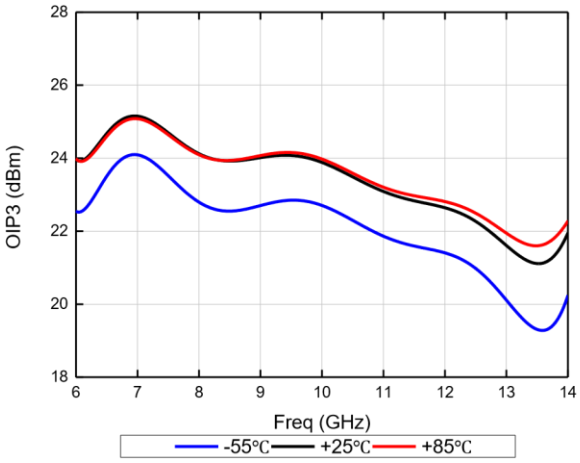

Figure 8. Output third-order intermodulation power

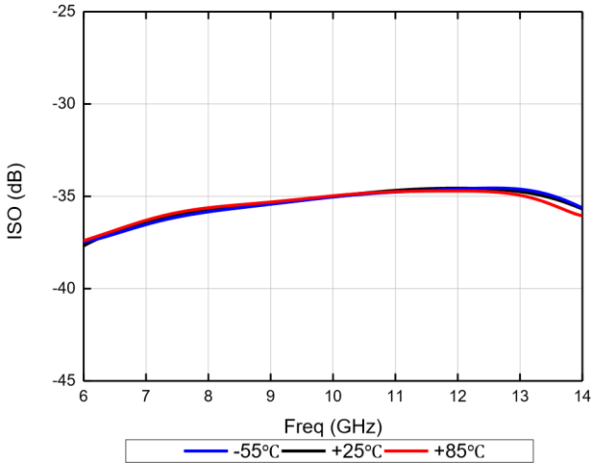

Figure 9. Reverse isolation

VI. Chip port diagram (unit: μm)

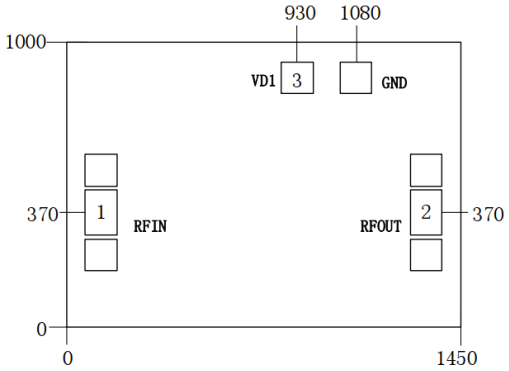

Figure 10.

VII. Port Definition

Table 3.

SERIAL NUMBER	PORT NAME	DEFINITION	SIGNAL OR VOLTAGE
1	RFIN	RF signal input terminal, no external DC blocking capacitor required	RF
2	RFOUT	RF signal output terminal, no external DC blocking capacitor required	RF
3	VD1	The LNA drain is positive, so it is recommended to add a 100pF capacitor.	+5V

VIII. Recommended assembly drawing

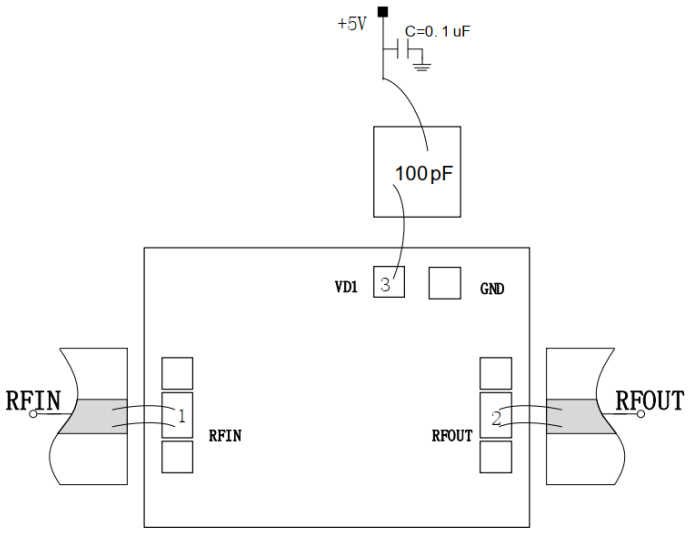

Figure 11.

IX. Precautions

- Assemble and use in a clean environment;
- GaAs material is very brittle and the chip surface is easily damaged (do not touch the surface), so you must be careful when using it;
- Two bonding wires (25μm diameter gold wire) are used for input and output, and the bonding wire length is about 400μm;
- The sintering temperature should not exceed 300 °C, and the sintering time should be as short as possible, not exceeding 30 seconds;
- This product is an electrostatic sensitive device, please be careful to prevent static electricity during storage and use;
- Store in a dry, nitrogen environment;
- Do not attempt to clean the chip surface with dry or wet chemical methods.