

BSTLN114-0713C

7-13GHz Low-Noise Amplifier Chip

Data Sheet

I. Product Introduction

The BSTLN114-0713C is a high-performance low-noise amplifier chip with a frequency range of 7 to 13 GHz, a small-signal gain of 25.5 dB, a noise figure of 0.8 dB, and an output 1 dB compression power of 9.5 dBm.

The amplifier uses a 4×4mm surface mount leadless ceramic tube shell, and the pin pad surface is gold-plated, suitable for reflow soldering installation.

II. Key Technical Indicators

Frequency range:	7-13GHz
Small signal gain:	25.5dB
 Output 1dB compression power: 	9.5dBm
Noise figure:	0.8dB
Input return loss:	17dB
Output return loss:	11dB
Power supply:	+5V@22.8mA
Chip size:	4.0mm x 4.0mm x 0.85mm



III. Functional Block Diagram

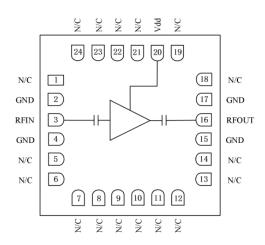


Figure 1. Functional Block Diagram

IV. Electrical Performance Table ($T_A = +25$ °C, $V_D = +5V$)

Table 1.

PARAMETER NAME	SYMBOL	MINIMUM	TYPICAL VALUES	MAXIMUM	UNIT
Frequency range	Freq	7	_	13	GHz
Small signal gain	Gain	24.5	25.5	26.5	dB
Gain flatness	ΔG	_	±1	_	dB
Noise Figure	NF	0.6	0.8	1.2	dB
Output 1dB compression power	OP1dB	7.8	9.5	10	dBm
Input return loss	RL_IN	15	17	_	dB
Output return loss	RL_OUT	8	11	_	dB
Quiescent operating current	ld	_	22.8	_	mA

V. Absolute Maximum Ratings

Table 2.

PARAMETER	LIMIT VALUE	
Maximum operating voltage	+7V	
Maximum input power	+20dBm	
Storage temperature	-65 °C ~+150 °C	
Operating temperature	-55 °C ~+125 °C	



VI. Test Curve

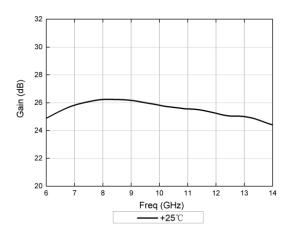


Figure 2. Small Signal Gain

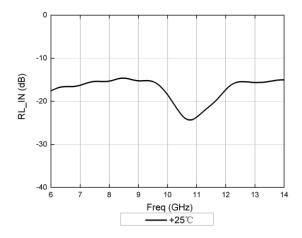


Figure 4. Input return loss

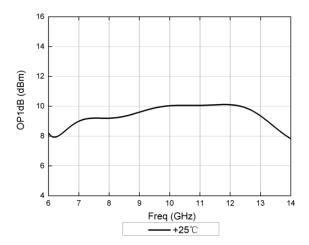


Figure 6. Output 1dB compression power

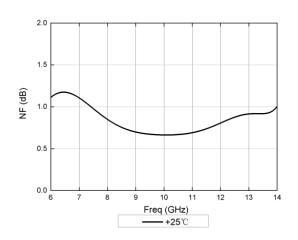


Figure 3. Noise Figure

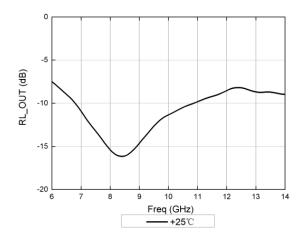


Figure 5. Output return loss

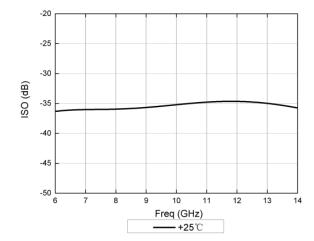


Figure 7. Isolation



VI. Appearance Structure Diagram (unit: mm)

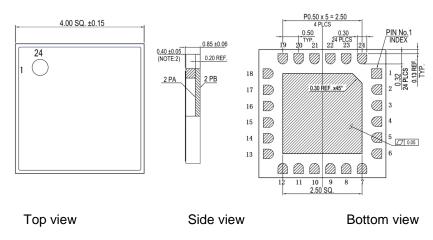


Figure 8.

VI. Port Definition

Table 3.

PORT NUMBER	PORT NAME	DEFINITION	SIGNAL OR VOLTAGE
3	RF _{IN}	RF signal input, no external DC blocking capacitor required	RF
16	RF _{OUT}	RF signal output, no external DC blocking capacitor required	RF
20	V_{dd}	Low noise drain bias	+5V
2, 4, 15, 17, ePAD	GND	The bottom of the chip needs to be well grounded to RF and DC	/
1, 5-14, 18, 19, 21-24	N/C	No welding required	1



VII. Recommended Assembly Drawing

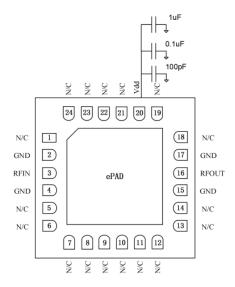


Figure 9.

VIII. Precautions

- Assemble and use in a clean environment;
- Sealing material: ceramic material that complies with ROSH standards;
- Lead frame material: copper alloy;
- Lead surface plating: gold, gold layer thickness greater than 1.5um;
- Maximum reflow peak temperature: 260°C;
- This product is an electrostatic sensitive device, please be careful to prevent static electricity during storage and use;
- Store in a dry, nitrogen environment;
- Do not attempt to clean the chip surface with dry or wet chemical methods.