

BSTGPA86-0711

7.5-10.5 GHz GaN Power Amplifier

Datasheet

I. Product Introduction

BSTGPA86-0711 is a power amplifier chip based on a 0.25 μ m GaN HEMT process. It operates in a frequency range of 7.5GHz to 10.5GHz, has a power gain greater than 25dB, a typical saturated output power of 49dBm, and a typical power-added efficiency of 40%. It can operate in pulsed mode. The chip is grounded via a backside via, and its typical operating voltage is $V_d=+28V$, $V_g=-2.6V$.

II. Key Technical Indicators

- Frequency range: 7.5GHz to 10.5GHz
- Power gain: 25dB
- Saturated output power: 49dBm
- Power added efficiency: 40%+28V@3.3A (static)
- Chip size: 3.70mm × 6.00mm × 0.10mm

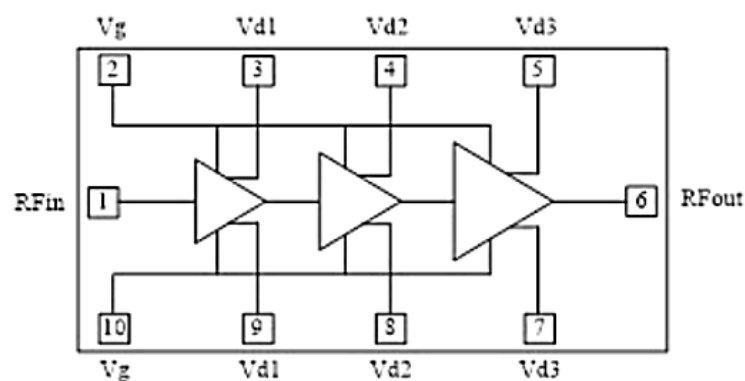


Figure 1. Functional Block Diagram

III. Application Areas

- Microwave transceiver components
- Solid-state transmitter

IV. DC parameters ($T_A = +25^\circ\text{C}$)

Table 1.

INDEX	SYMBOL	MINIMUM	TYPICAL VALUES	MAXIMUM	UNIT
Gate operating voltage	V_g	-3.0	-2.6	-2.4	V
Drain operating voltage	V_d	-	28	32	V
Static drain current	I_d	-	3.3	-	A
Dynamic drain current	I_{dd}	-	7.0	7.5	A
Dynamic gate current	I_{gg}	-	3.0	10.0	mA

V. Microwave Electrical Parameters ($T_A = +25^\circ\text{C}$, $V_d = +28\text{V}$, $V_g = -2.6\text{V}$)

Table 2.

INDEX	SYMBOL	MINIMUM	TYPICAL VALUES	MAXIMUM	UNIT
Frequency range	f	7.5~10.5			GHz
Saturated output power	P_{sat}	48.6	49.0	-	dBm
Power gain	G_p	24.6	25.0	-	dB
Power gain flatness	ΔG_p	-	-	± 0.5	dB
Power added efficiency	PAE	-	40	-	%
Linear gain	S_{21}	-	36		dB
Linear gain flatness	ΔS_{21}	-	-	± 1	dB
Input standing wave	VSWR (in)	-	1.6	2.0	-

Note: All chips have been 100% DC tested and 100% RF tested on-chip.

VI. Absolute Maximum Ratings

Table 3.

PARAMETER	SYMBOL	LIMIT VALUE
Maximum drain-source forward bias voltage	V_d	+32V
Minimum gate negative bias	V_g	-5V
Maximum input power	P_{in}	+28dBm
Storage temperature	T_{STG}	-65 °C ~ +150 °C
Maximum operating channel temperature	T_{OP}	+225 °C

VII. Typical Curve ($V_d=+28V$, $V_g=-2.6V$)

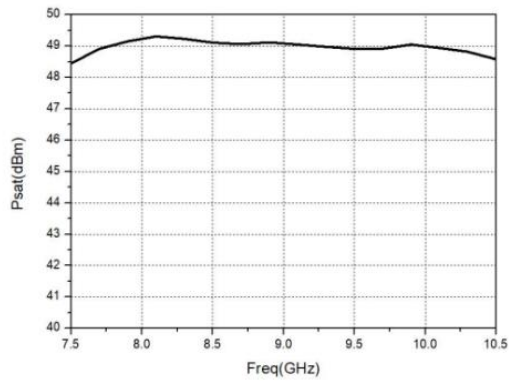


Figure 2. Saturated output power vs. frequency
($P_{in} = 24dBm$)

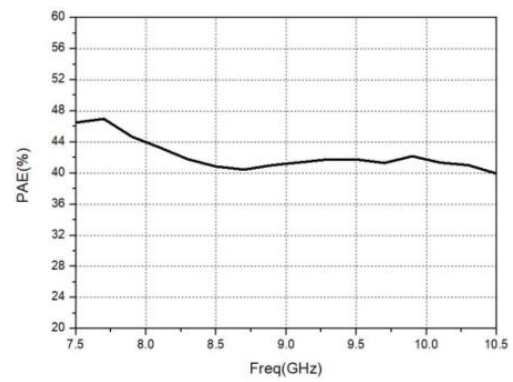


Figure 3. Additional Frequency vs. Frequency
($P_{in} = 24dBm$)

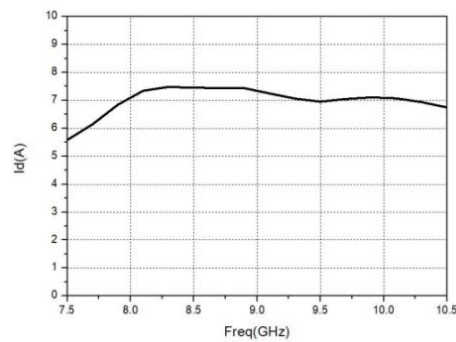


Figure 4. Dynamic Drain Current vs. Frequency ($P_{in} = 24dBm$)

VIII. Dimensions

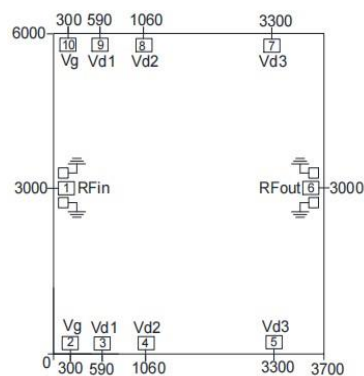


Figure 5.

Notes: Units in the Figure 5 are micrometers (μm);

Dimensional tolerance is $\pm 100\mu m$.

IX. Pressure Point Sorting Chart

Table 4.

FUNCTION SYMBOL	FUNCTIONAL DESCRIPTION	SIZE
RF _{in}	Signal input terminal	100μm×100μm
V _g	Gate power supply terminal	120μm×100μm
V _{d1}	Drain power supply terminal	120μm×100μm
V _{d2}	Drain power supply terminal	120μm×100μm
V _{d3}	Drain power supply supply terminal	250μm×100μm
RF _{out}	Signal output terminal	100μm×120μm

X. Recommended Assembly Drawing

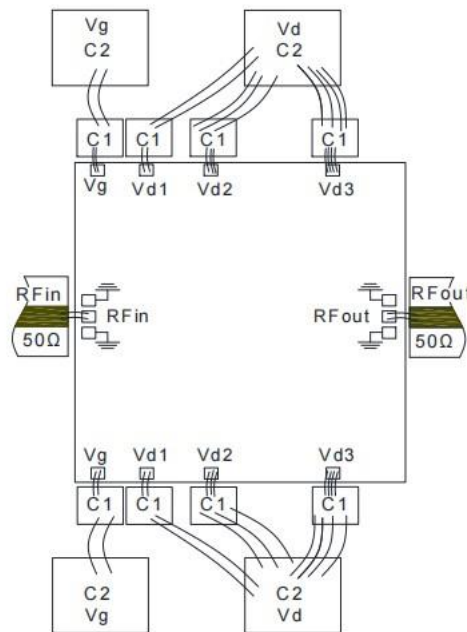


Figure 6.

Notes:

- The capacitance of the peripheral capacitor is C1=100pF, C2=1000pF. It is recommended to use single-layer ceramic capacitors, and C1 should be as close to the chip as possible, not exceeding 750μm.
- Consider bonding / sintering 125μm to 250μm low-loss, low-dielectric-constant microstrip lines on a carrier to reduce transmission loss, and control the input and output bonding wire lengths within 350μm±150μm.

XI. Precautions

- The monolithic circuit needs to be stored in a dry and clean N₂ environment;
- The chip substrate 6H-SiC material is very brittle and must be used with care to avoid damaging the chip;
- There is no insulating protective layer on the chip surface, so attention should be paid to the cleanliness of the assembly environment to avoid excessive surface contamination;
- The thermal expansion coefficient of the carrier should be close to that of 6H-SiC material, with a linear thermal expansion coefficient of $4.2 \times 10^{-6}/^{\circ}\text{C}$. It is recommended that the carrier material be CuMoCu or CuMo or CuW;
- Avoid holes between the chip and the carrier during assembly, and ensure good heat dissipation between the box and the carrier;
- It is recommended to use gold-tin solder for sintering, Au:Sn=80%:20%, sintering temperature not exceeding 300 °C, and sintering time not longer than 30 seconds. The sintering process should avoid rapid temperature changes and require gradual temperature increase and decrease;
- It is recommended to use gold wire with a diameter of 25μm to 30μm, the bonding platform chassis temperature should not exceed 250 °C, the bonding time should be as short as possible, and the bonding process should avoid rapid temperature changes;
- When power is applied, the gate voltage is increased first and then the drain voltage; when power is removed, the drain voltage is reduced first and then the gate voltage;
- The chip has DC blocking capacitors at the input and output, but the input has a DC short-circuit structure to ground;
- Pay attention to anti-static during chip use and assembly, wear a grounded anti-static bracelet, and ensure that the sintering and bonding stations are well grounded.