BSTGPA79-1826

18-26.5 GHz GaN Power Amplifier

Data Sheet

I. Product Introduction

BSTGPA79-1826 is a GaN broadband power amplifier chip with a frequency range of 18GHz~26.5GHz, a typical small signal gain of 25dB, a typical saturated output power of 41dBm, and can be used in pulse and continuous wave modes.

II. Application Areas

- Communication
- Electronic Countermeasures

III. Key technical indicators

- Frequency range: 18.0GHz~26.5GHz
- Small signal gain: 25dB
- Saturated output power: 41dBm
- PAE: 26%
- DC power supply: V_d=22V@Id=900mA (Vg=-2.1V)
- Chip size: 4.10 mm × 3.20 mm × 0.08 mm

IV. Microwave electrical parameters (T_A = +25 ◦C, V_d = 22V, I_d = 900mA)

Table 1.

INDEX	MINIMUM	TYPICAL VALUES	MAXIMUM	UNIT
Frequency range		18~26.5		GHz
Small signal gain		25		dB
Gain flatness		±0.4		dB
Saturated output power		41		dBm
Power added efficiency		26		%
Power gain		19		dB

INDEX	MINIMUM	TYPICAL VALUES	MAXIMUM	UNIT
Input / output standing wave		1.5		-
Saturation current		2.8		A

V. Absolute Maximum Ratings

Table 2.

PARAMETER	LIMIT VALUE
Drain positive voltage	24V
Negative gate voltage	-5V
Input power	27dBm
Storage temperature	-65 ℃～ +150 ℃
Operating temperature	-55 ℃～ +85 ℃

VI. Typical curve (T_A = +25 ℃, V_d = 22V, I_d = 900mA)

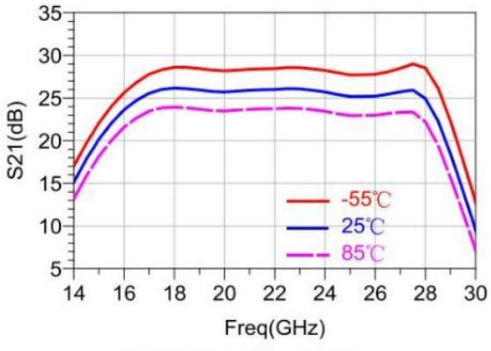

Figure 1. Small Signal Gain vs. Frequency vs. Temperature

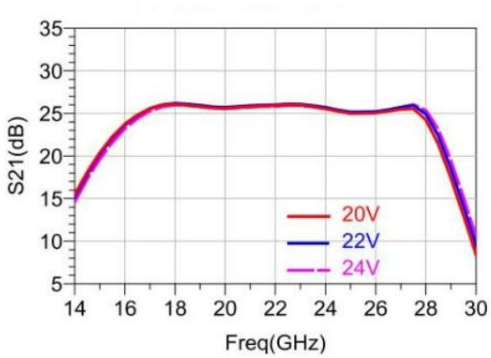

Figure 2. Small Signal Gain vs. Frequency vs. Drain Voltage

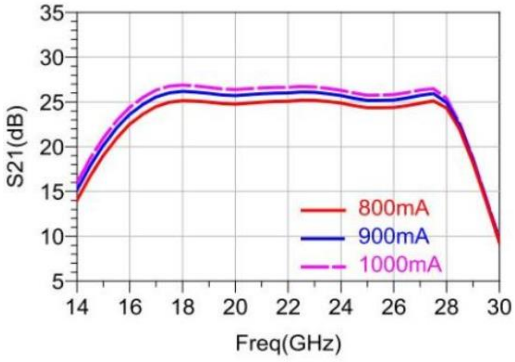

Figure 3. Small signal gain vs. frequency vs. leakage current

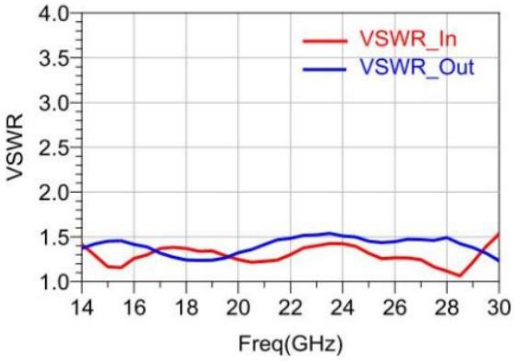

Figure 4. Input/output standing wave vs. frequency @T_a=25℃

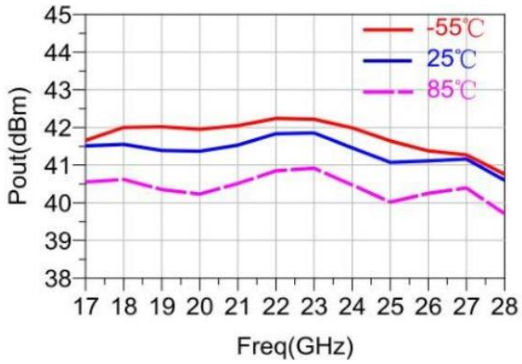

Figure 5. Saturated output power vs. frequency @P_{in}=22dBm

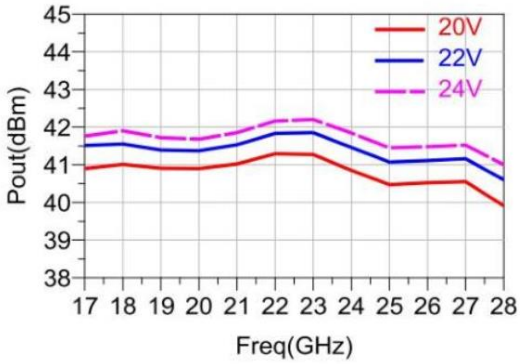

Figure 6. Saturated output power vs. frequency @P_{in}=22dBm

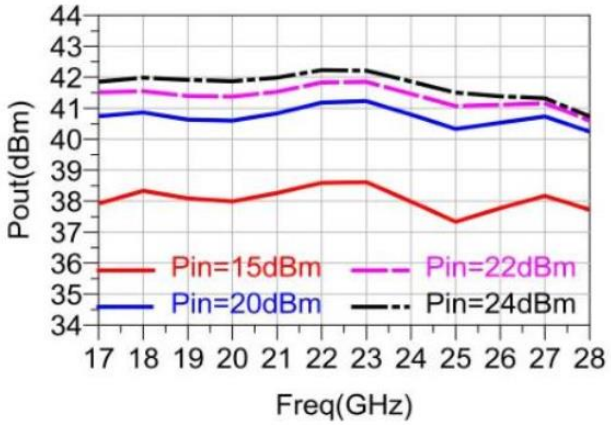

Figure 7. Saturated output power vs. frequency vs. input power

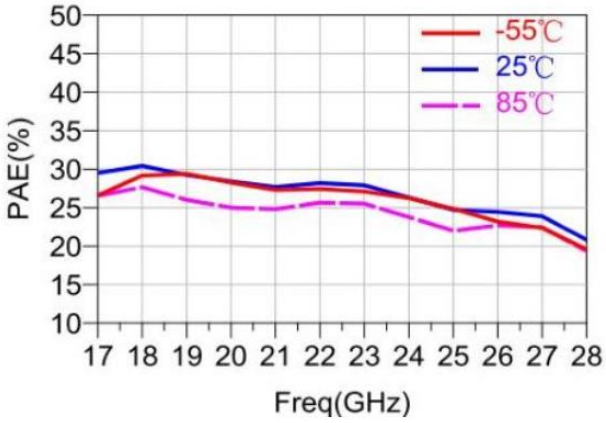

Figure 8. Power added efficiency vs. frequency @Pin=22dBm

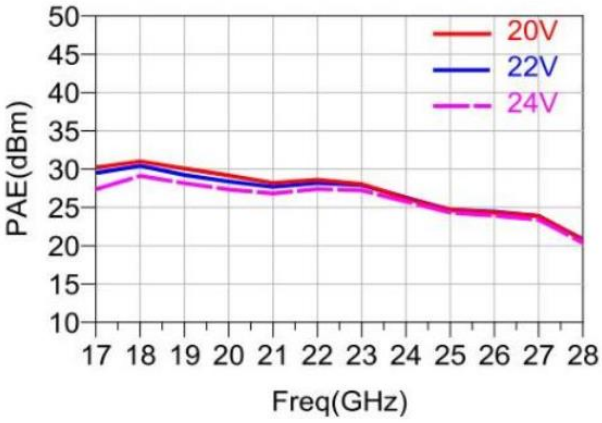

Figure 9. Power added efficiency vs. frequency @ Pin = 22dBm

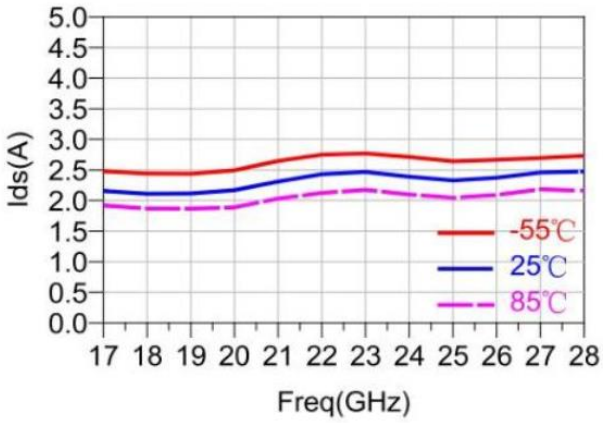

Figure 10. Saturation current vs. frequency @ Pin = 22dBm

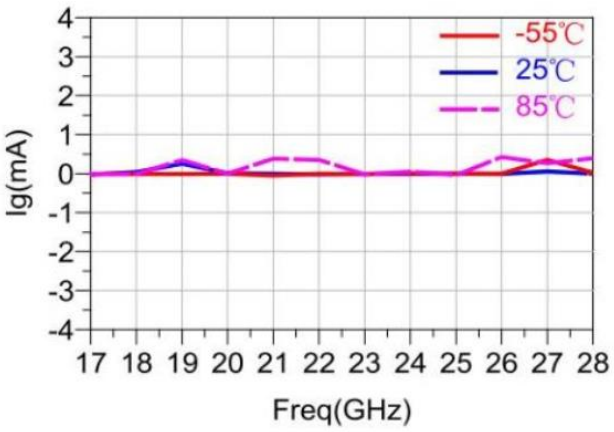

Figure 11. Gate current vs. frequency @Pin=22dBm

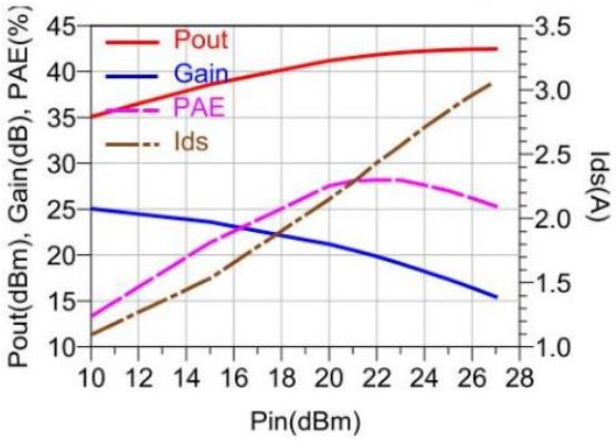

Figure 12. Output power, efficiency, gain and current vs. input power @Pin=22dBm

VII. Dimensions

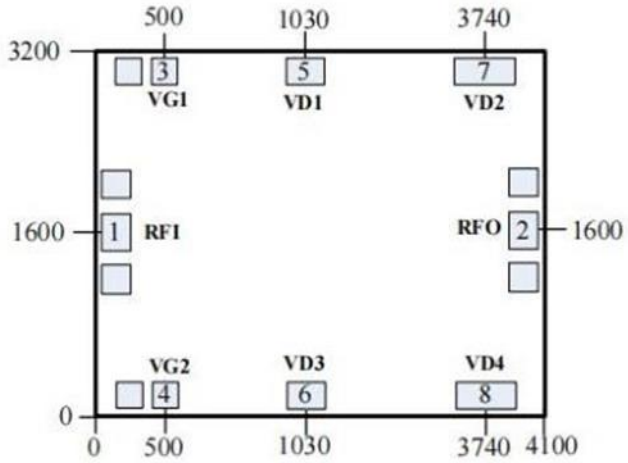

Figure 12.

Notes:

Units in the figure are micrometers (μm);

Dimensional tolerance ±50μm;

Chip thickness 80μm.

VIII. Pressure point sorting chart

SERIAL NUMBER	FUNCTION SYMBOL	FUNCTIONAL DESCRIPTION	SIZE
1, 2	RFin, RFout	RF signal input and output terminals, external 50 ohm system, no need for DC blocking capacitors	100μm×120μm
3, 4	Vg1, Vg2	The gate voltage feed terminal requires external 100pF, 1000pF and 10uF bypass capacitors	100μm×100μm
5, 6	Vd1, Vd2	Drain voltage feeder requires external 100pF, 1000pF and 10uF bypass capacitors	150μm×100μm
7, 8	Vd3, Vd4	Drain voltage feeder requires external 100pF, 1000pF and 10uF bypass capacitors	200μm×100μm

IX. Recommended assembly drawing

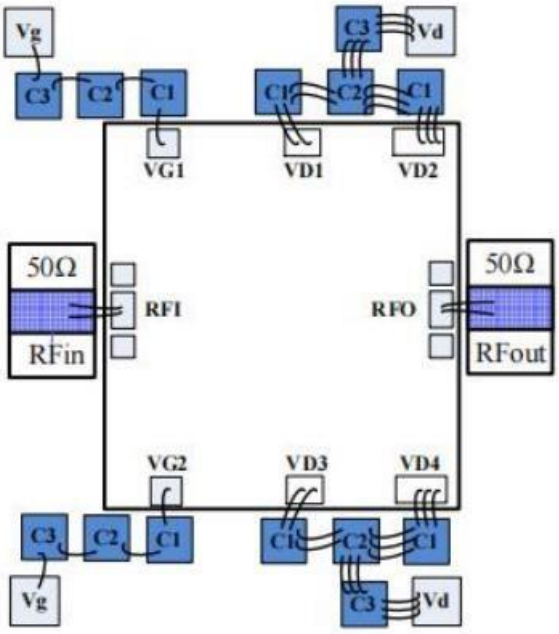

Figure 13.

Note:

The capacitance of the peripheral capacitor C1 is 100pF, the capacitance of C2 is 1000pF, and the capacitance of C3 is 10μF.

It is recommended to use a single-layer capacitor for C1, as close as possible to the chip bonding point.

X. Precautions

- Storage: The chip must be placed in a container with electrostatic protection and stored in a nitrogen environment.
- Cleaning: Bare chips must be handled in a clean environment and it is prohibited to use liquid detergents to clean the chips.
- Electrostatic protection: Please strictly comply with ESD protection requirements to avoid electrostatic damage.
- General operation: Please use a vacuum chuck or precision pointed tweezers to handle the chip. Avoid touching the chip surface with tools or fingers during operation.
- Power-on sequence: When powering on, add the gate voltage first and then the drain voltage; when powering off, remove the drain voltage first and then the gate voltage.
- Mounting: Chip mounting can be done using AuSn solder eutectic sintering or conductive adhesive. For bonding, the mounting surface must be clean and flat, and the gap between the chip and the input and output RF connection substrate must be minimized. Sintering: Use 80/20 AuSn sintering. The sintering temperature should not exceed 300 °C, the sintering time should be as short as 20 seconds, and the friction time should not exceed 3 seconds.
- Bonding process: When bonding conductive adhesive, dispense as little glue as possible, and refer to the information provided by the conductive adhesive manufacturer for curing conditions.
- Bonding Procedure: Unless otherwise specified, use two bonding wires (25μm diameter gold wire) for RF input and output, keeping the wires as short as possible. Thermosonic bonding temperature is 150 °C, using the lowest possible ultrasonic energy. For ball bonding, use a wedge pressure of 40-50 gf; for wedge bonding, use a wedge pressure of 18-22 gf.