

## **BSTGPA13-0812**

### **8-12 GHz GaN Power Amplifier**

#### **Data Sheet**

### **I. Product Introduction**

BSTGPA13-0812 is a monolithic driver amplifier chip fabricated using a 0.25μm GaN HEMT process. It operates in the 8GHz to 12GHz frequency range, boasts a power gain greater than 14dB, a typical saturated output power of 29dBm, and a typical power-added efficiency of 15%. It can operate in both pulsed and continuous-wave modes. The chip is grounded via a backside via and operates from a single power supply with a typical operating voltage of +28V. This chip is widely used in radar, communications, and electronic countermeasures.

### **II. Application Areas**

- Communication
- Radar
- Electronic Countermeasures

### **III. Key technical indicators**

- |                           |                             |
|---------------------------|-----------------------------|
| • Frequency range:        | 8GHz~12GHz                  |
| • Power gain:             | 14dB                        |
| • Saturated output power: | 29dBm                       |
| • Power added efficiency: | 15%                         |
| • Power supply:           | +28V@ 0.17A (static)        |
| • Chip size:              | 1.95 mm × 1.35 mm × 0.08 mm |

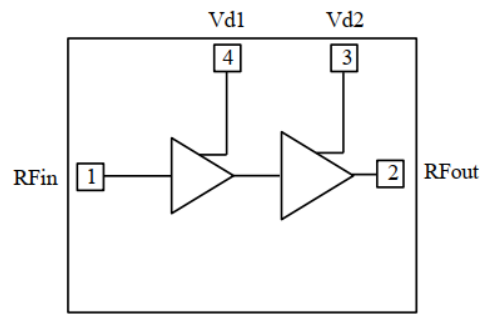


Figure 1. BSTGPA13-0812 Functional Block Diagram

#### IV. DC parameters ( $T_A = + 25\text{ }^{\circ}\text{C}$ )

Table 1.

| INDEX                   | SYMBOL   | MINIMUM | TYPICAL VALUES | MAXIMUM | UNIT |
|-------------------------|----------|---------|----------------|---------|------|
| Drain operating voltage | $V_d$    | -       | 28             | -       | V    |
| Static drain current    | $I_d$    | 160     | 170            | 190     | mA   |
| Dynamic drain current   | $I_{dd}$ | 160     | 170            | 190     | mA   |

#### V. Microwave electrical parameters ( $T_A = +25\text{ }^{\circ}\text{C}$ , $V_d = + 28\text{V}$ )

Table 2.

| INDEX                  | SYMBOL          | MINIMUM | TYPICAL VALUES | MAXIMUM   | UNIT |
|------------------------|-----------------|---------|----------------|-----------|------|
| Frequency range        | $f$             | 8~12    |                |           | GHz  |
| Saturated output power | $P_{sat}$       | -       | 29             | -         | dBm  |
| Power gain             | $G_p$           | 13      | 14             | -         | dB   |
| Power gain flatness    | $\Delta G_p$    | -       | $\pm 0.5$      | -         | dB   |
| Power added efficiency | PAE             | -       | 15             | -         | %    |
| Linear gain            | $S_{21}$        | -       | 16             | -         | dB   |
| Linear gain flatness   | $\Delta S_{21}$ | -       | -              | $\pm 0.5$ | dB   |
| Input standing wave    | VSWR(in)        | -       | 1.5            | 2         |      |

Note:

- 1) All chips have been 100% DC tested and 100% RF tested on-chip;
- 2) Unless otherwise specified, the test conditions for the curves in this manual are:  $V_d = +28\text{V}$

## VI. Absolute Maximum Ratings

Table 3.

| PARAMETER                                    | SYMBOL | LIMIT VALUE      |
|----------------------------------------------|--------|------------------|
| Maximum drain-source voltage                 | Vd     | +32V             |
| Maximum input power (CW)                     | Pp     | 18dBm            |
| Storage temperature                          | TSTG   | -65 °C ~ +150 °C |
| Maximum operating channel temperature        | Top    | +225 °C          |
| Load impedance mismatch (burnout resistance) | Z0     | -                |

## VII. Typical curve ( $V_d=+28V$ )

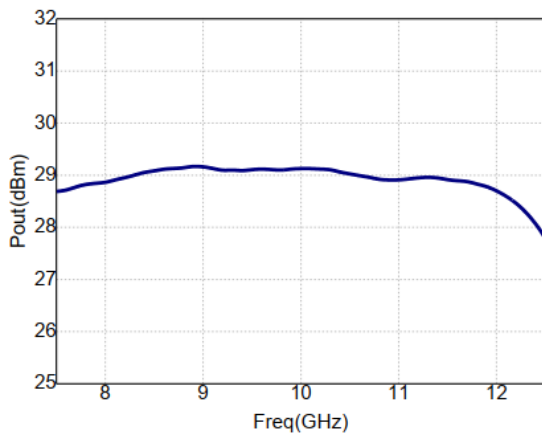


Figure 2. Saturated output power vs. frequency

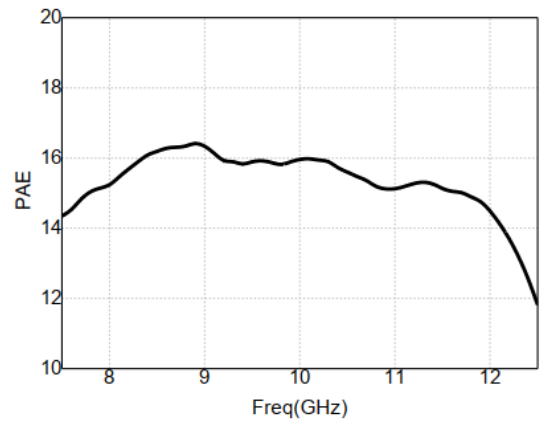


Figure 3. PAE vs. Frequency

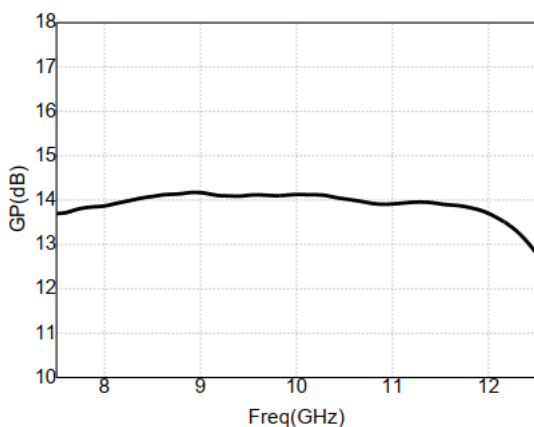


Figure 4. Gain vs. Frequency

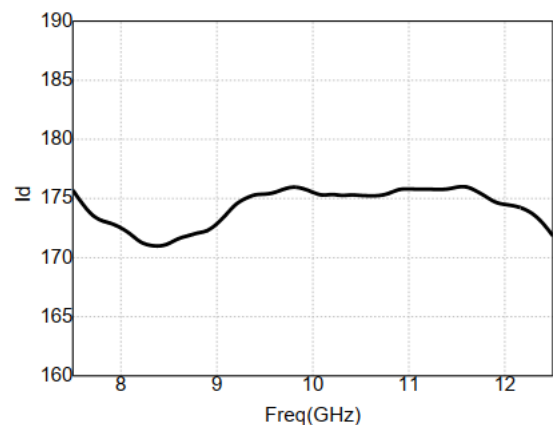


Figure 5. Dynamic Current vs. Frequency

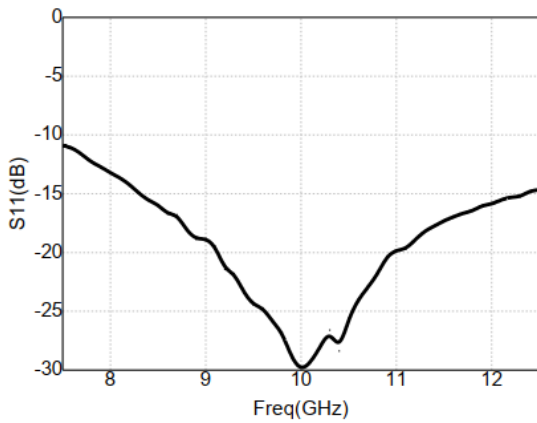


Figure 6. S11 vs. Frequency

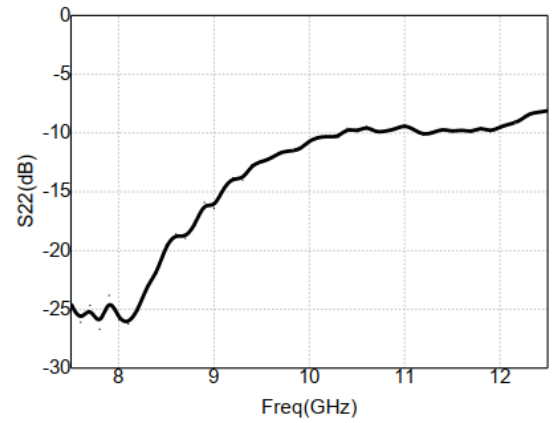


Figure 7. S22 vs. Frequency

## VIII. Dimensions and Pressure Point Sorting Diagram

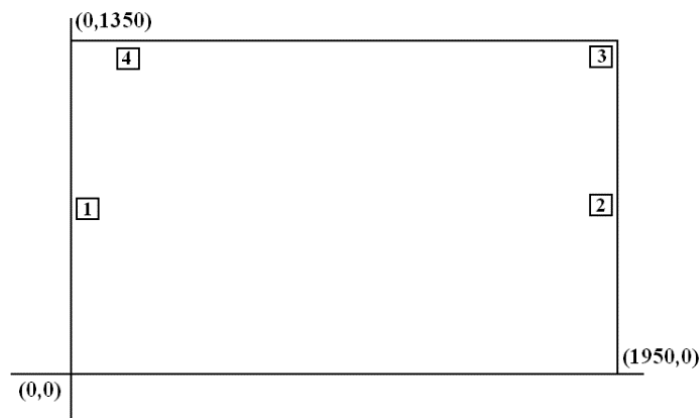


Figure 8.

Table 4.

| SERIAL NUMBER | SYMBOL            | FUNCTION                    | SIZE        | LOCATION         |
|---------------|-------------------|-----------------------------|-------------|------------------|
| 1             | RF <sub>in</sub>  | Signal input terminal       | 100μm×100μm | (80μm, 680μm)    |
| 2             | RF <sub>out</sub> | Signal output terminal      | 100μm×100μm | (1870μm, 680μm)  |
| 3             | V <sub>D2</sub>   | Drain power supply terminal | 100μm×100μm | (1890μm, 1240μm) |
| 4             | V <sub>D1</sub>   | Drain power supply terminal | 100μm×100μm | (230μm, 1260μm)  |

Note: The unit in the figure is micrometer (μm); the external dimension tolerance is ±100μm.

## IX. Recommended assembly drawing

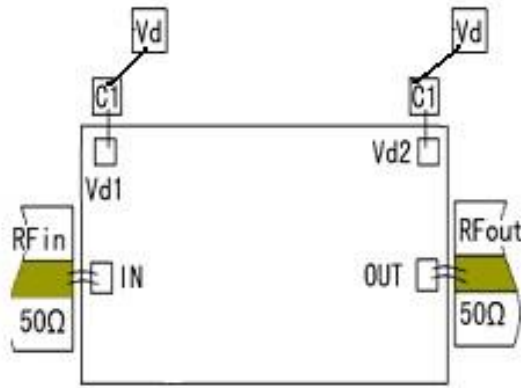


Figure 9.

### Notes:

- The capacitance of the external capacitor is  $C_1 = 1000\text{pF}$ . It is recommended to use a single-layer ceramic capacitor.  $C_1$  should be as close to the chip as possible, not exceeding  $750\mu\text{m}$ .
- Consider bonding / sintering  $125\mu\text{m}$  to  $250\mu\text{m}$  low-loss low-dielectric constant microstrip lines on the carrier to reduce transmission loss and input and output bonding. The length of the gold wire is controlled within  $350\mu\text{m} \pm 150\mu\text{m}$ .

## X. Precautions

- Storage: The chip must be placed in a container with electrostatic protection and stored in a nitrogen environment.
- Cleaning: Bare chips must be handled in a clean environment and it is prohibited to use liquid detergents to clean the chips.
- Electrostatic protection: Please strictly comply with ESD protection requirements to avoid electrostatic damage.
- General operation: Please use a vacuum chuck or precision pointed tweezers to handle the chip. Avoid touching the chip surface with tools or fingers during operation.
- Power-on sequence: When powering on, add the gate voltage first and then the drain voltage; when powering off, remove the drain voltage first and then the gate voltage.
- Mounting operation: Chip mounting can be done by AuSn solder eutectic sintering or conductive adhesive; bonding process, the mounting surface must be clean and flat, and the gap between the chip and the input and output RF connection line substrate must be as small as possible.

- Sintering process: Use 80/20 AuSn for sintering. The sintering temperature should not exceed 300 °C. The sintering time should be as short as possible, not exceeding 20 seconds, and the friction time should not exceed 3 seconds.
- Bonding process: When bonding conductive adhesive, dispense as little glue as possible, and refer to the information provided by the conductive adhesive manufacturer for curing conditions.
- Bonding Procedure: Unless otherwise specified, use two bonding wires (25μm diameter gold wire) for RF input and output, keeping the wires as short as possible. Thermosonic bonding temperature is 150 °C, using the lowest possible ultrasonic energy. For ball bonding, use a wedge pressure of 40-50 gf; for wedge bonding, use a wedge pressure of 18-22 gf.