

## BSTFGPA02-0204Q

### 2.7-3.5 GHz GaN Internally Matched Power Amplifier

#### Data sheet

#### I. Product Introduction

BSTFGPA02-0204Q is a GaN HEMT chip with an operating frequency range of 2.7 GHz to 3.5 GHz. It has a typical saturated output power of 56 dBm and a power gain greater than 13 dB.

BSTFGPA02-0204Q is an internally matched power tube for standard.

It is suitable for the communication frequency band and provides the best power and gain performance in 50 ohm system.

#### II. Key technical indicators

- Frequency range: 2.7GHz to 3.5GHz
- Power gain: 13dB
- Saturated output power: 56dBm
- Power added efficiency: 50%
- Package: CMW025B

#### III. Application Areas

- Microwave transceiver components
- Solid-state transmitter

#### IV. Electrical performance table ( $T_A = +25\text{ }^{\circ}\text{C}$ )

Table 1.

| PARAMETER NAME         | TEST CONDITIONS                                                                            | MINIMUM | TYPICAL VALUES | MAXIMUM | UNIT |
|------------------------|--------------------------------------------------------------------------------------------|---------|----------------|---------|------|
| Saturated output power | $f=2.7 \sim 3.5\text{GHz}$<br>$V_{GS}$ = a point between -2 and -4V<br>$V_{DS}=44\text{V}$ | 56      | 56.5           | -       | dBm  |
| Power gain             |                                                                                            | 13      | 13.5           | -       | dB   |
| Additional efficiency  |                                                                                            | 50      | 55             | -       | %    |

| PARAMETER NAME              | TEST CONDITIONS                                                     | MINIMUM | TYPICAL VALUES | MAXIMUM | UNIT |
|-----------------------------|---------------------------------------------------------------------|---------|----------------|---------|------|
| Power gain flatness         | $I_{DS} = (0.2 \sim 0.5) I_{DSS}$ Pulse width 300us, duty cycle 10% | -       | -              | 1.5     | dB   |
| pinch-off voltage           | $V_{DS} = 6V, I_{DS} \leq 80mA$                                     | -4      | -              | -2      | V    |
| Gate-source reverse current | $V_{DS} = 0V, V_{GS} = -10V$                                        | -       | -              | 10      | mA   |

## V. Absolute Maximum Ratings

Table 2.

| PARAMATER                     | VALUE           |
|-------------------------------|-----------------|
| Source-drain voltage $V_{DS}$ | 60V             |
| Gate-source voltage $V_{GS}$  | -5V             |
| Storage temperature           | -65 °C ~+175 °C |
| Channel temperature           | 200 °C          |

## VI. Typical curve ( $V_d=+44V, V_g=-2.9V, 10\%$ duty cycle)

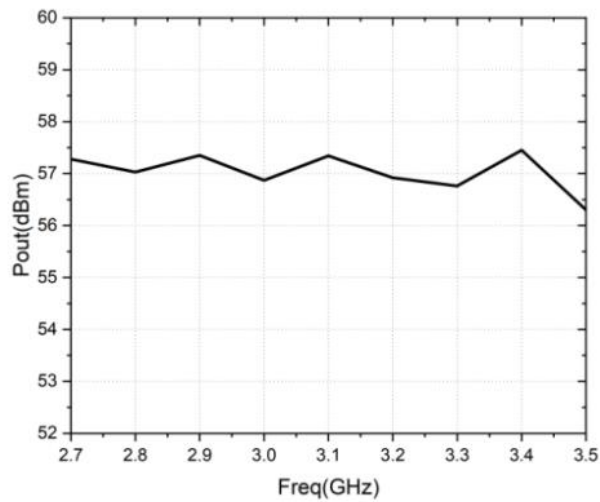


Figure 1. Saturated output power vs. frequency  
( $P_{in}=43dBm$ )

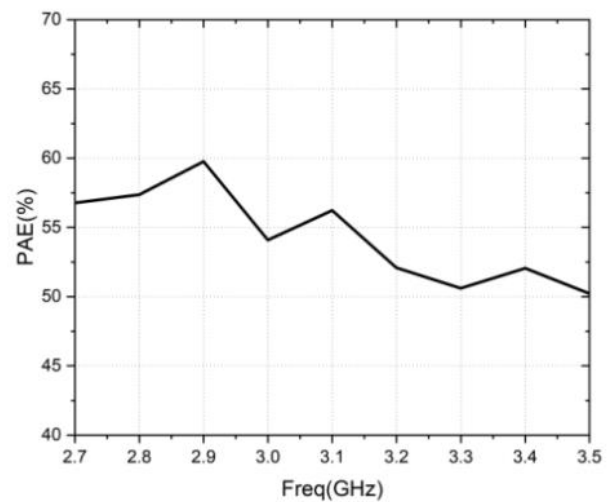


Figure 2. Additional efficiency vs. frequency  
( $P_{in}=43dBm$ )

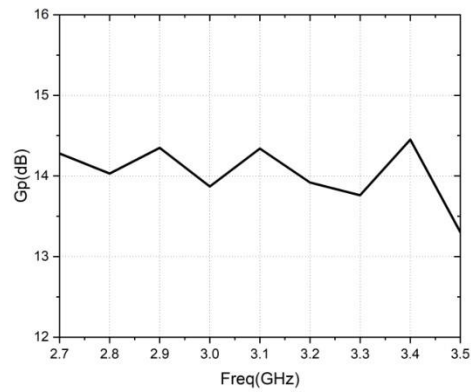


Figure 3. Power Gain vs. Frequency ( $P_{in} = 43\text{dBm}$ )

## VII. Overall dimensions (mm)

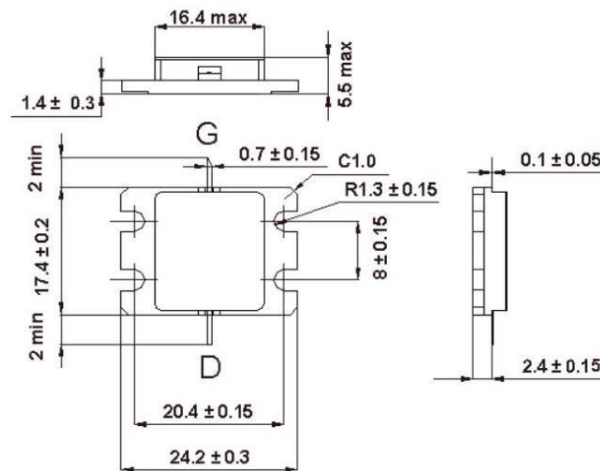


Figure 4.

## VIII. Typical application circuit

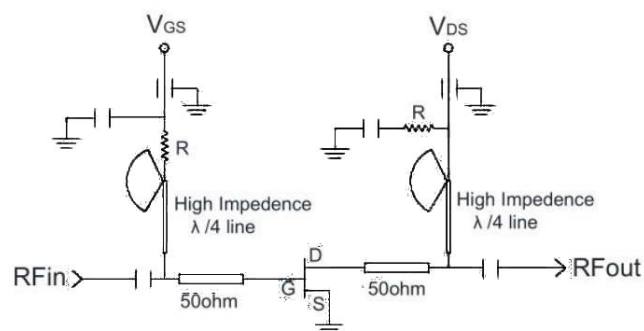


Figure 5.

## IX. Precautions

- Storage: The chip must be placed in a container with electrostatic protection and stored in a nitrogen environment.
- Cleaning: Bare chips must be handled in a clean environment and it is prohibited to use liquid detergents to clean the chips.
- Electrostatic protection: Please strictly comply with ESD protection requirements to avoid electrostatic damage.
- General operation: Please use a vacuum chuck or precision pointed tweezers to handle the chip. Avoid touching the chip surface with tools or fingers during operation.
- Power-on sequence: When powering on, add the gate voltage first and then the drain voltage; when powering off, remove the drain voltage first and then the gate voltage.
- Mounting operation: Chip mounting can be done by AuSn solder eutectic sintering or conductive adhesive; bonding process, the mounting surface must be clean and flat, and the gap between the chip and the input and output RF connection line substrate must be as small as possible.
- Sintering process: Use 80/20 AuSn for sintering. The sintering temperature should not exceed 300 °C. The sintering time should be as short as possible, not exceeding 20 seconds, and the friction time should not exceed 3 seconds.
- Bonding process: When bonding conductive adhesive, dispense as little glue as possible, and refer to the information provided by the conductive adhesive manufacturer for curing conditions.
- Bonding Procedure: Unless otherwise specified, use two bonding wires (25μm diameter gold wire) for RF input and output, keeping the wires as short as possible. Thermosonic bonding temperature is 150 °C, using the lowest possible ultrasonic energy. For ball bonding, use a wedge pressure of 40-50 gf; for wedge bonding, use a wedge pressure of 18-22 gf.