BSTEPC1

Data sheet

Ver.1.00

I. Product Overview

BSTEPC1 configures SRAM-based programmable devices in serial mode through 4 pins, and can increase capacity through cascading, with a maximum of 16 cascades. Devices such as APEX 20K, Mercury, ACEX 1K and FLEX series can be configured using BSTEPC1.

II. Product features

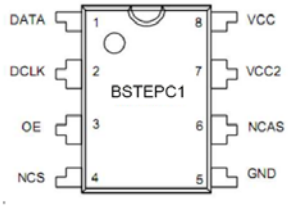
The supply voltage is 5V, the configuration current is low and the quiescent current is close to zero.

- Using advanced flash technology, its storage time can exceed 100 years and the number of erase and write times is 20,000 times.
- Only 4 pins are needed for configuration, and data is sent serially.
- The configuration capacity can be easily expanded in a cascaded manner, up to 16M.
- Supports Quartus II and MAX+PLUS II development tools, but requires a dedicated programmer.

III. Detailed Functional Description

The package used by BSTEPC1 is CDIP8. Figure 1 below is the pin arrangement diagram of the chip package.

The functional description of each pin of BSTEPC1 is shown in Table 1.



Picture 1. BSTEPC1 Pinout diagram

Table 1. BSTEPC1 pin function table

Pin Name	Pin Type	Functional Description
\DATA	Bidirectional	Data sending end, this pin is tri-stated when OE is low or nCS or the chip has sent all data.
DCLK	Bidirectional	If the master chip is in PS mode, this pin is the output clock and controls the clock signal of the target device and the slave chip; if the slave chip is in PS mode or in AS mode, this pin is the input function, and the internal logic function is controlled by the external clock. The internal register is valid on the rising edge of the clock, and the next bit of data is sent to the DATA pin on the rising edge. After the configuration is completed or when OE is low, this pin is low.
OE	Open drain, bidirectional	Output enable (high active), and reset (low active). When OE is low, the internal registers are reset, and when it is high, the address counter and DATA pin are allowed to operate.
nCS	enter	Chip select signal, low effective. When the chip select is effective, the address counter and DATA pin start to work under clock control. The master and slave of the chip are determined by the high and low of this pin after reset. If it is high, it is the master chip, and if it is low, it is the slave chip.
nCASC	Output	Cascade signal pin, low effective. When the address counter reaches the maximum value, this pin is pulled low. In cascade mode, this pin is connected to the nCS pin of the next level configuration chip to enable the next level configuration chip.
VCC2	enter	Programming multiplexing pin, grounded in programming mode and connected to power in user mode
VCC	power supply	Power input pin
GND	land	Ground pin

3.1. Power-On Reset

BSTEPC1 has a power-on delay module inside. During the initial power-on period, the module will generate a power-on reset signal with a maximum of 200ms to wait for the power supply voltage to stabilize. Except for configuring FLEX8000, all power-on delays are controlled by BSTEPC1. When configuring a FLEX 8000 device, the power-on reset delay signal is controlled by the FLEX8000 internally, which is typically 100ms and a maximum of 200ms.

3.2. Error detection circuit

BSTEPC1 has an internal error detection circuit, which is only valid when configured with Mercury, APEX20K, ACEX1K, FLEX10K or FLEX6000.

During configuration, the error detection circuit detects the change of the chip's nCS pin (which is connected to the CONF_DONE pin of the PLD device). After completing the configuration, HEDEPC1 will use 16 clock cycles to wait for the PLD device to send the CONF_DONE signal (high active). If nCS becomes high during these 16 cycles, the configuration is terminated and the configuration is considered correct; if it becomes high after these 16 cycles, it is considered a configuration error; if it is before these 16 cycles (that is, data configuration is in progress), it is also considered a configuration error.

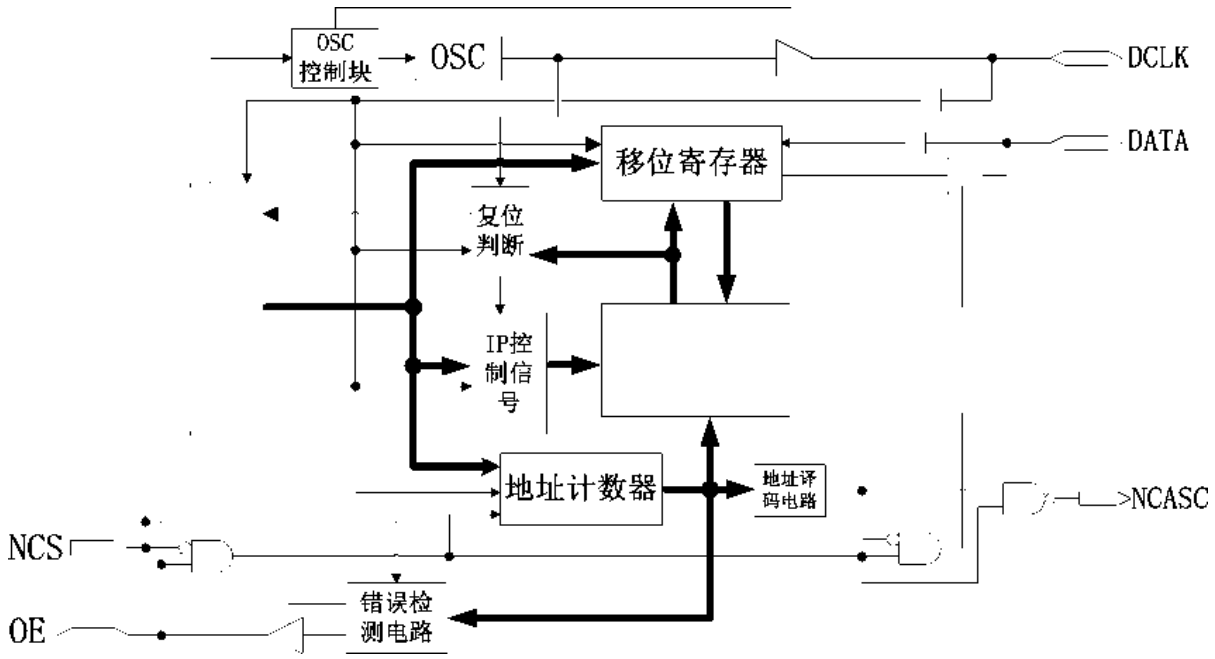
After the above error occurs, BSTEPC1 will reset by pulling its OE pin low. Since all OE pins (PLD devices and cascaded BSTEPC1) are connected together, all devices

If the user sets the automatic reconfiguration function through the development software, reconfiguration will start after the reset is completed.

If the PLD (Programmable Logic Device) device detects a CRC error, it will pull its nSTATUS pin low. Since this signal is connected to the OE pin of BSTEPC1, BSTEPC1 will be reset and then reconfigured (the automatic reconfiguration function does not need to be set at this time).

3.3. Configuration

BSTEPC1 can directly configure its corresponding target chip through 4 ports (DCLK, DATA, OE and nCS) without the need for an external intelligent controller. Figure 2 is a block diagram of the internal structure of BSTEPC1. When configuring FLEX8000, its internal error detection and clock do not work (the OE pin in the figure is an open-drain structure).



Picture 2. BSTEPC1 Functional Block Diagram

The OE and nCS pins of BSTEPC1 control the tri-state of the DATA pin and control the enable of the address counter and OSC. When OE is low, BSTEPC1 resets the address counter and sets the DATA pin to tri-state. The nCS pin controls the output of BSTEPC1. When OE goes high to complete the reset, if nCS is also high at this time, the chip will not work, the address counter is not enabled, and the DATA pin is still tri-state. When nCS goes low, the address counter starts counting and the DATA pin starts outputting. No matter what state nCS is in, as long as OE is pulled low, BSTEPC1 will be reset and the DATA pin will be tri-state.

When OE becomes high and nCS is low, BSTEPC1 starts to send data. Since OE is an open-drain structure and the OEs of all chips are connected together, OE becomes high because all chips release the control of OE and are pulled high by the pull-up resistor. nCS is controlled by the target chip.

When BSTEPC1 has sent all the data, it will pull down the nCASC pin (this pin is used for cascading) and set the DATA pin to tri-state. This will prevent signal conflicts with the cascaded chips. After the configuration is completed correctly, BSTEPC1 will enter the IDLE state.

When using BSTEPC1 for configuration, the connection modes between it and the target

chip are AS (Active serial) and PS (Passive serial). In AS mode, the target chip provides the clock and control signals, while in PS mode, the configuration chip (such as BSTEPC1) provides the clock and control signals.

3.3.1. Typical Configuration

- Single-chip configuration using PS mode

  As shown in Figure 3, this is a typical connection method for the configuration of BSTEPC1. The pull-up resistor of the target chip marked in the figure is 1KΩ (the pull-up resistor value varies according to different target chips, please refer to the user manual of each target chip for details), nCEO is floating, and all cascade pins are floating due to the single-chip configuration.

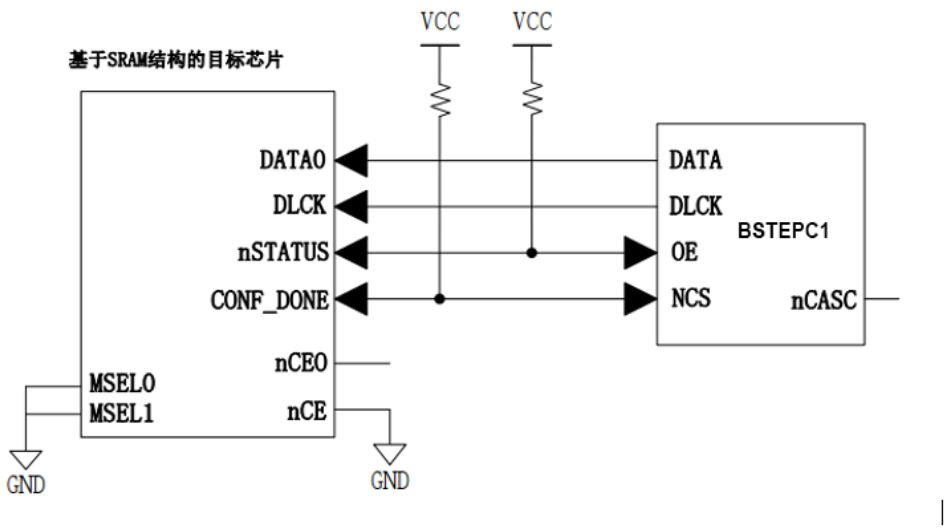


Figure 3. Connection method of BSTEPC1 configuration

As shown in the figure above, DLCK, OE and nCS of BSTEPC1 generate the configured address counter and the three-state control signal of the DATA pin. The data is transmitted to the DATA pin through serial-to-parallel conversion inside BSTEPC1, and then sent serially to the data receiving end DATA0 pin of the target chip.

- Cascade configuration using PS mode configuration

  If the data of the target chip exceeds the capacity of one BSTEPC1, then two or more BSTEPC1s are required to complete the configuration. They are connected in cascade, that is, the nCASC pin of the previous chip is connected to the nCS

pin of the next chip, and the other pins (DATA, DCLK and OE) are all connected together. The specific connection method is shown in Figure 4.

When the target chip is configured in cascade configuration, the configuration chips are connected in master-slave mode. The chip that connects all signals to the target chip is called the master chip (configuration chip 1 in Figure 4), and the other configuration chips are called slave chips. In PS mode, the clocks of all chips (including the target chip) are provided by the master chip. During configuration, the data is first provided by the master chip. After the master chip sends the data, it provides a cascade signal to its next level chip through its nCASC pin (such as configuration device 2 in Figure 4). After the next level chip sends the data, it provides a cascade signal to its next level through its nCASC pin, and so on until all data are sent.

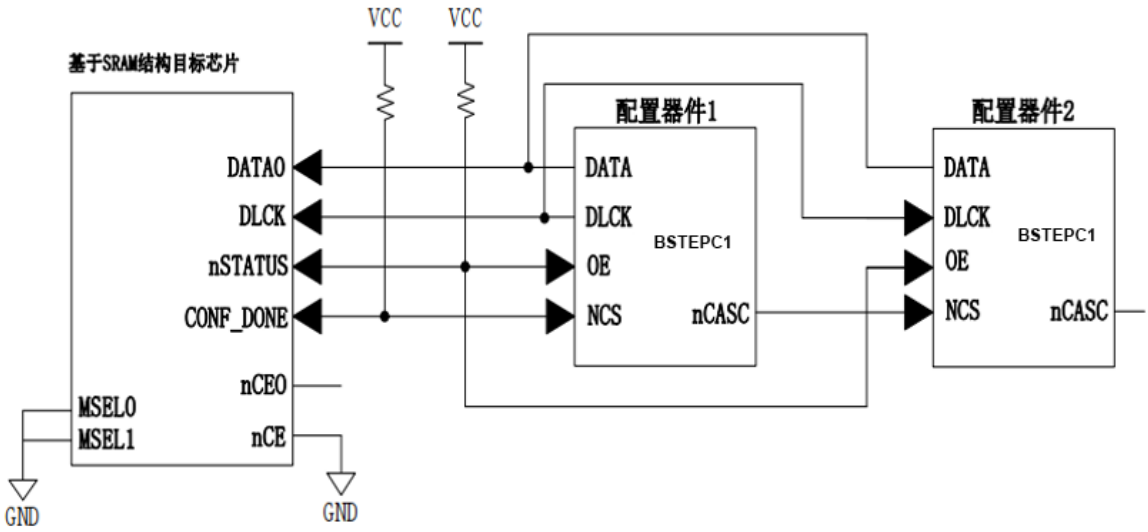


Figure 4. Cascade configuration connection mode of BSTEPC1

- Configuring FLEX8000 (AS mode)

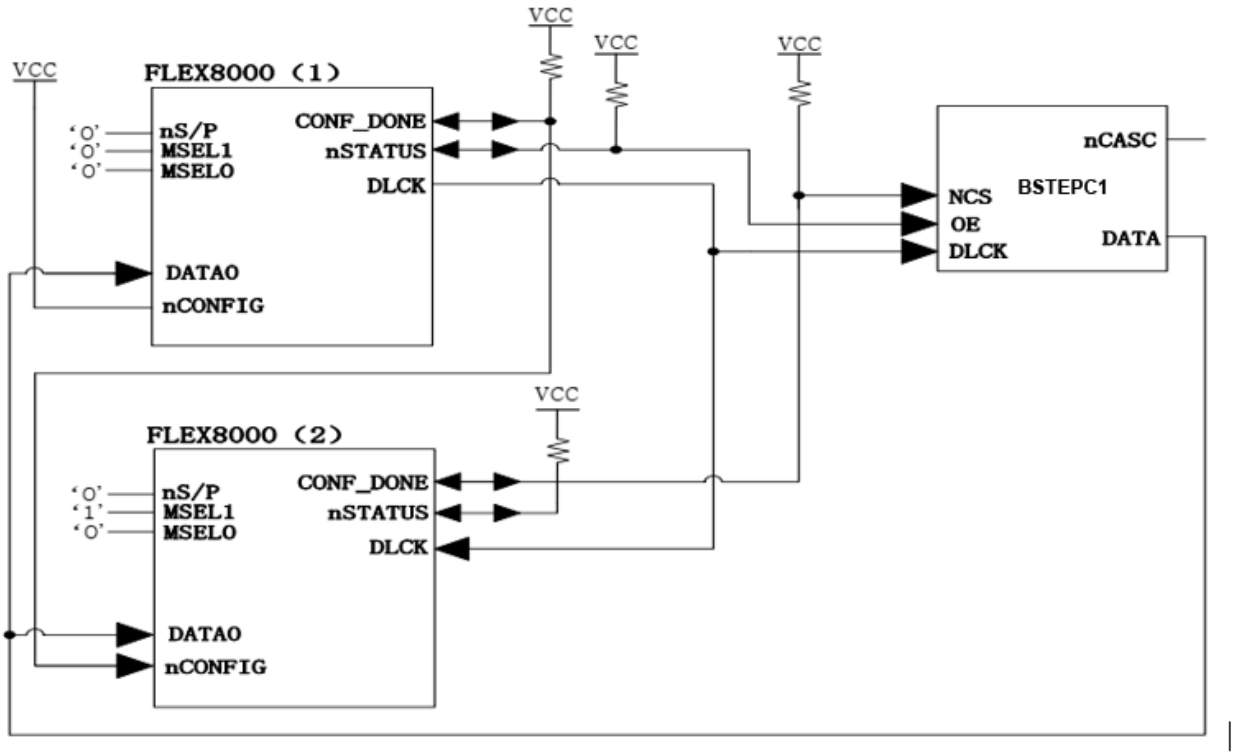
  FLEX8000 is configured in AS mode, and the clock required for configuration is provided by FLEX8000 through its internal OSC. BSTEPC1 can configure FLEX8000, and can also replace EPC1441, EPC1213, EPC1064 and EPC1064V to configure FLEX8000 (that is, the POF of these configuration chips can be

written into BSTEPC1 for configuration). Since the capacity of BSTEPC1 is larger than the above configuration chips, one chip can be used to configure multiple FLEX8000s.

The connection method for configuring FLEX8000 is shown in Figure 5, where one BSTEPC1 is used to configure two FLEX8000s. The connection of FLEX8000 is cascaded, and the CONF_DONE signal is given by the last FLEX8000.

If only one FLEX8000 needs to be configured, just remove the FLEX8000 (2) in Figure 5 and connect the CONF_DONE of the FLEX8000 to the nCS pin of BSTEPC1.

All pull-up resistors in Figure 5 are 1KΩ and should be connected to the same supply voltage VCC as BSTEPC1.



- Configure timing and parameters

  The configuration timing waveform of BSTEPC1 is shown in Figure 6, and the configuration timing parameters are shown in Table 2 and Table 3.

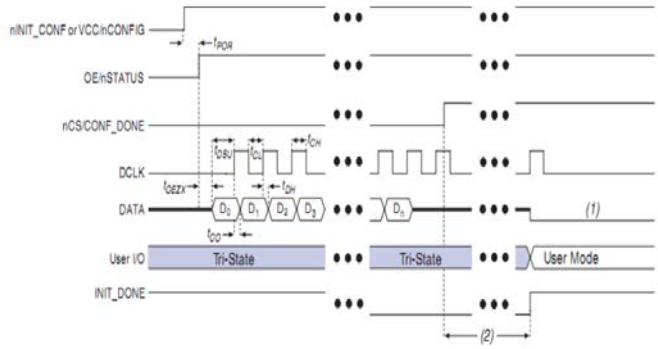


Figure 6. BSTEPC1 configuration sequence

Note:

- After configuration is completed, DATA will be pulled low by the configuration device.
- The initialization time of the target device. For details, please refer to the relevant device manual.

Table 2. EPC1 configuration timing parameters (except FLEX8000)

symbol	parameter	Minimum	Typical Value	Maximum	unit
tCE	Output delay from OE high to the first clock			200	ns
oeLh	OE goes high to data output enable time			50	ns
tCO	DCLK to data output delay			20	ns
oeLh	DCLK high level time (master chip)	30	50	75	ns
TKM	DCLK low level time (master chip)	30	50	75	ns
f	Clock frequency	6.7	10	16.7	MHZ
tSCH	DCLK high time (slave chip)	30			ns
tSCL	DCLK low level time (slave chip)	30			ns
tCASC	DCLK rising edge to nCASC			20	ns
tC	nCS to U nCASC Cascade Delay			10	ns
f	DCLK to data enable time			20	ns
T8C	OE low to clock invalid time			20	ns
TnRCAS	OE Low to U nCASC Delay			25	ns
tN	OE level reset time	100			ns

Table 3. FLEX8000 configuration timing parameters

Symbol	Parameter	Minimum	Maximum	unit
oeLh	OE high to data output enable time		50	ns
tX	nCS low to data output enable time		50	ns
tX	nCS high to data output three-state time		50	ns
tCSS	Setup time from nCS low to the first clock rising edge	50		ns
tC	nCS low hold time for DCLK rising edge	0		ns
tD	Data setup time for clock rising edge	50		ns
tD	Data hold time for clock rising edge	0		ns
tCO	Delay from clock to data output		75	ns
tCK	Clock cycle	100		ns
f	Clock frequency		8	MHZ
tCL	DCLK low level time	50		ns
tCH	DCLK high time	50		ns
XOt	OE low or nCS high to data output three-state time		50	ns
oeLh	OE minimum reset pulse width	100		ns
tCASC	The delay from the last DCLK+1 to nCASC going low		50	ns
tX	The last DCLK+1 to data tri-state delay		50	ns
tCEOUT	Delay time from nCS going high to nCASC going high		100	ns

IV. Application

Table 4. BSTEPC1 product usability

Operating temperature	model
-55℃~ 125℃ (military)	BSTEPC1

V. Electrical properties

5.1. Maximum rated operating conditions

Table 5. Maximum Rating Conditions

Symbol	Prameter	Minimum	Maximum	unit
VCC	Supply voltage	-2.0	7.0	V
VI	DC input voltage	-2.0	7.0	V

IMAX	DC VCC or GND current		50	m A
IOUT	DC output current	-25	25	m A
PD	Power dissipation		250	m W
TSTG	Storage temperature	-65	150	℃
TAMB	Ambient temperature	-65	135	℃
TJ	Junction temperature		135	℃

5.2. Recommended working conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Minimum	Maximum	unit
VCC	Supply voltage	4.5	5.5	V
VI	Input voltage	-0.3	VCC+0.3	V
VO	Output voltage	0	VCC	V
TA	Operating temperature	-55	125	℃
R	Input rise time		20	ns
Tf	Input Fall Time		20	ns

5.3. DC working conditions

Table 7. DC working conditions

Symbol	Parameter		Minimum	Maximum	unit
VIH	Input high level		2.0	VCC+0.3	V
VIL	Output low level		-0.3	0.8	V
VOH	High level TTL output	IOH=-4mA dc	2.4		V
VOL	Output low level	IOL=4mA dc		0.4	V
II	Input leakage current	VI = VCC or GND	-10	10	uA
IOZ	Three-state output off-state current	VO=VCC or GND	-10	10	uA

5.4. Supply current ICC

Table 8. Power supply current

Symbol	Parameter	Minimum	Typical Value	Maximum	unit
ICC0	VCC static supply current		50	100	uA
ICC1	VCC Configuration Current		30	50	mA

VI. Package Specifications

BSTEPC1 chooses NTK CDIP8 custom tube shell. The device adopts 8-lead ceramic CDIP8 package. The following figure 7 is the package size diagram. The size is stipulated in table 9.

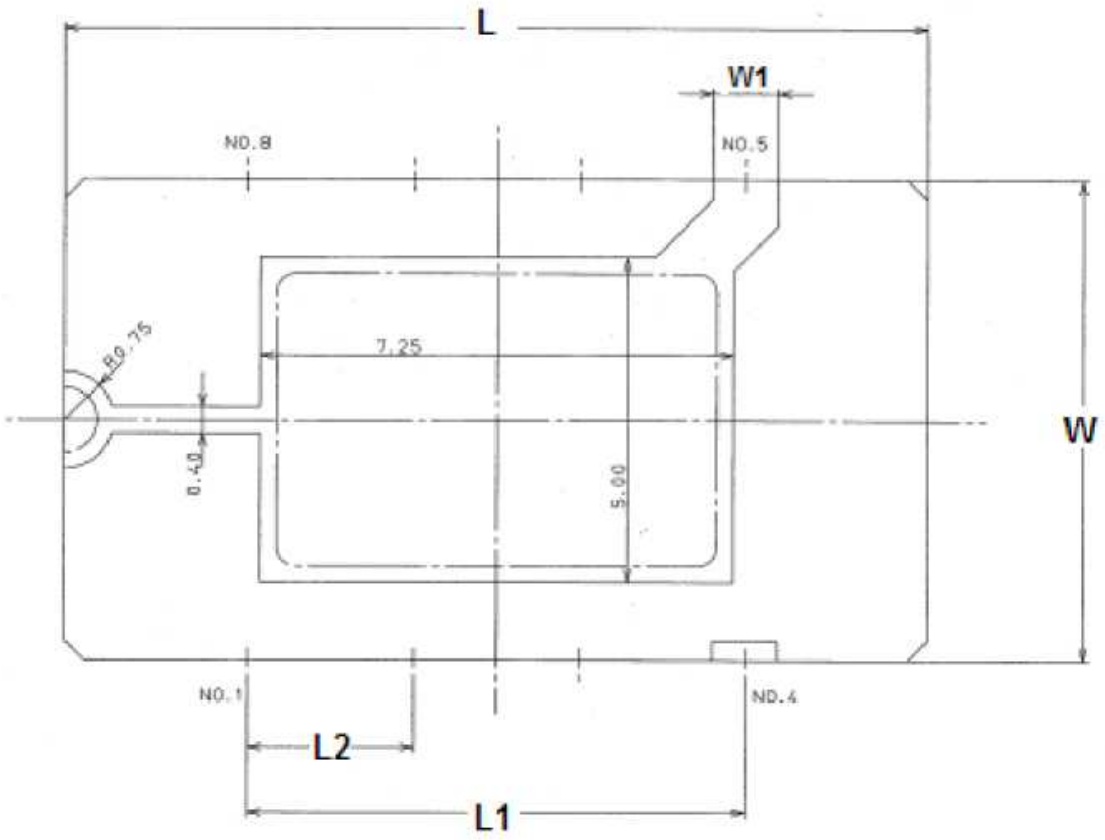


Figure 7. BSTEPC1 package specifications

Table 9. Package Dimensions

Symbol	Describe	TypicalValue
L	Packagelength	13.21mm
L1	Maximumspacingbetweenfourpins	7.62mm
L2	Twopinspacing	2.54mm
W	Packagewidth	7.37mm
W1	Pinwidth	1.0mm