BSTDA02-0614C

6.5-13.5GHz driver amplifier chip

I. Product Introduction

BSTDA02-0614C is a driver amplifier chip with excellent performance, covering a frequency range of 6.5~13.5GHz. The small signal gain is 21dB, the saturated output power is 25dBm, the saturated power added efficiency is 32%, and the saturated dynamic current is 220mA.

The driver adopts 4×4mm surface mount leadless ceramic tube shell, and the surface of the pin pad is gold-plated, which is suitable for reflow soldering installation.

II. Main Parameters

2.1. Functional Block Diagram

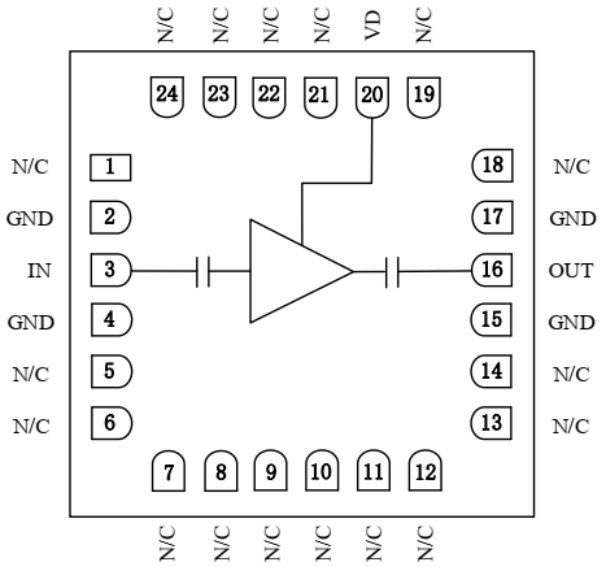


Figure 1.

2.2. Key technical indicators

- Frequency range: 6.5-13.5GHz
- Small signal gain: 21dB
- Input return loss: 15dB
- Output return loss: 13dB
- Saturated output power: 25dBm

- Saturated power added efficiency: 32%
- Power supply: +5V@145mA
- Chip size: 4.0mm × 4.0mm × 0.85mm

Table 1. Electrical performance table (TA = +25℃, VD = +5V)

PARAMETER NAME	SYMBOL	MINIMUM	TYPICAL VALUE	MAXIMUM	UNIT
Frequency range	Freq	6.5	—	13.5	GHz
Small Signal Gain	Gain	18	21	—	dB
Output 1dB compression power	OP1dB	22.5	24.5	—	dBm
Saturated output power	Psat	23	25	—	dBm
Output third-order intermodulation @Pout=+7dBm	OIP3	31	34	—	dBm
Power added efficiency @P1dB	PAE	23	29	—	%
Saturated power added efficiency	PAE	24	32	—	%
Noise Figure	NF	—	5	7	dB
Input return loss	RL_IN	—	15	—	dB
Output return loss	RL_OUT	—	13	—	dB
Dynamic current @P1dB	IDD	—	210	230	mA
Saturation dynamic current	IDD	—	220	240	mA
Static operating current	IDQ	—	145	150	mA

2.3. Absolute maximum ratings

Table 2.

PARAMETER	VALUE
Maximum operating voltage	+6V
Maximum input power	+13dBm
Storage temperature	-65℃~+150℃
Operating temperature	-55℃~+125℃

III. Test curve

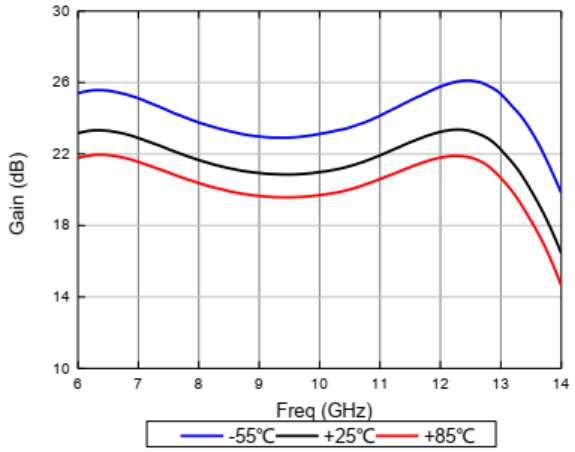


Figure 2. Small signal gain

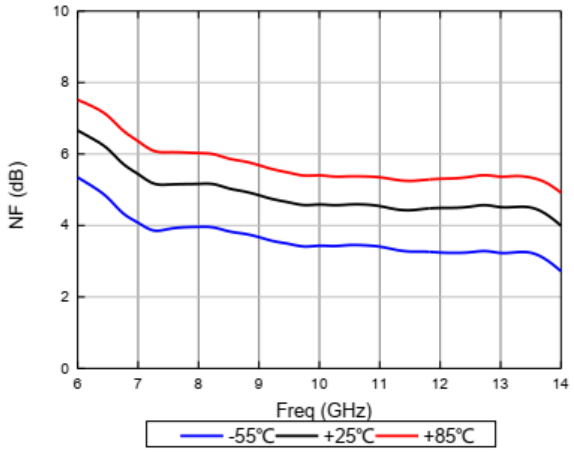


Figure 3. Noise figure

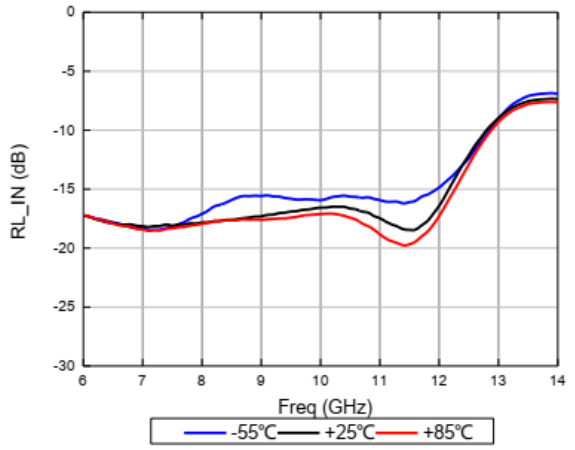


Figure 4. Input return loss

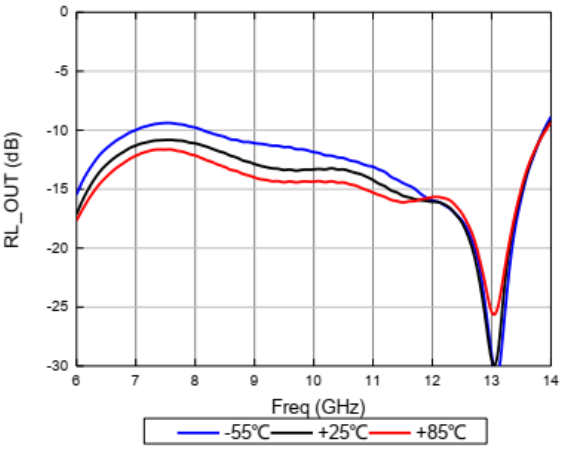


Figure 5. Output return loss

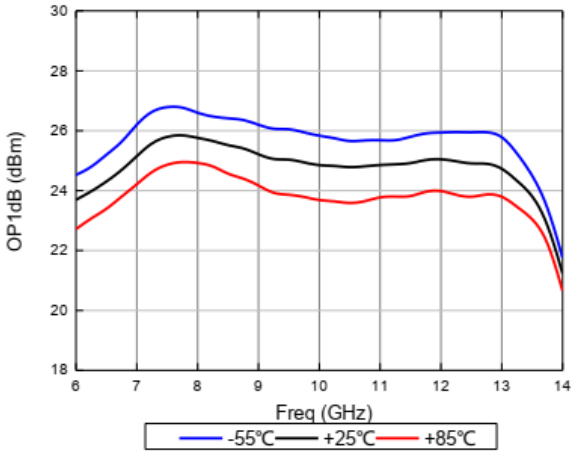


Figure 6. Output 1dB compression power

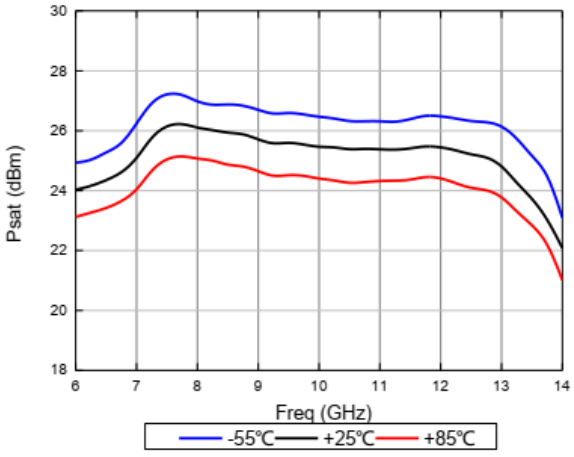


Figure 7. Saturated output power

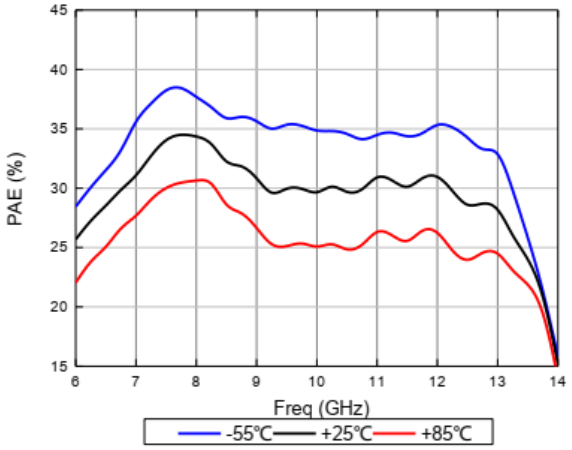


Figure 8. Power added efficiency@P1dB

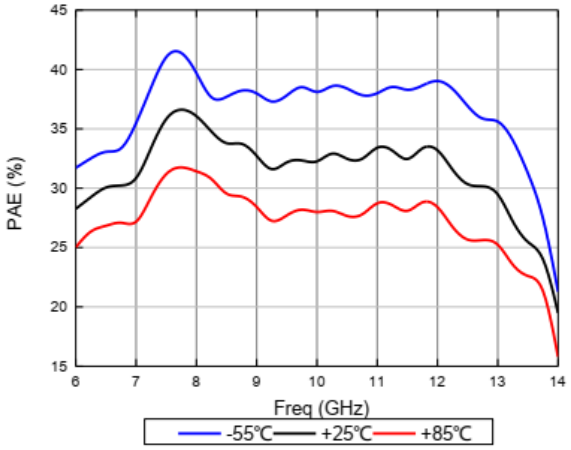


Figure 9. Saturated power added efficiency

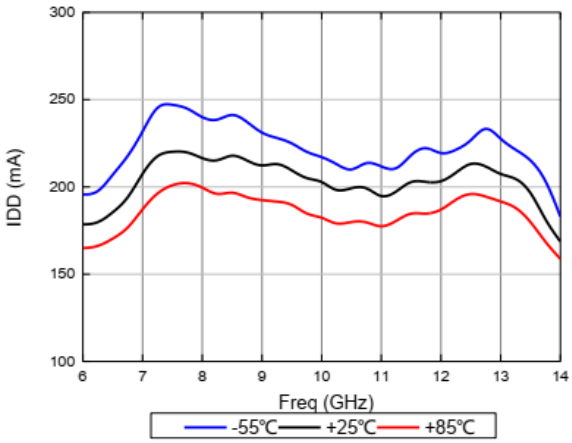


Figure 10. Dynamic current @P1dB

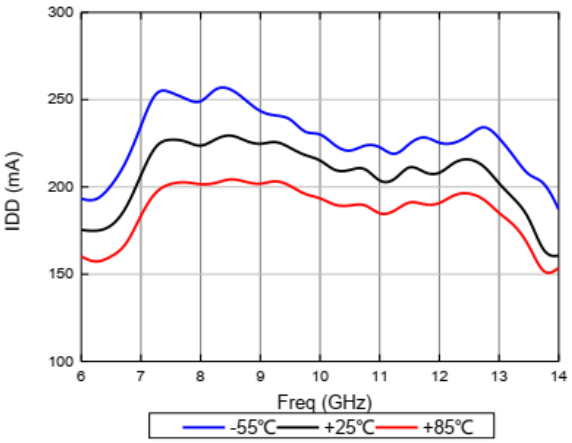


Figure 11. Saturation dynamic current

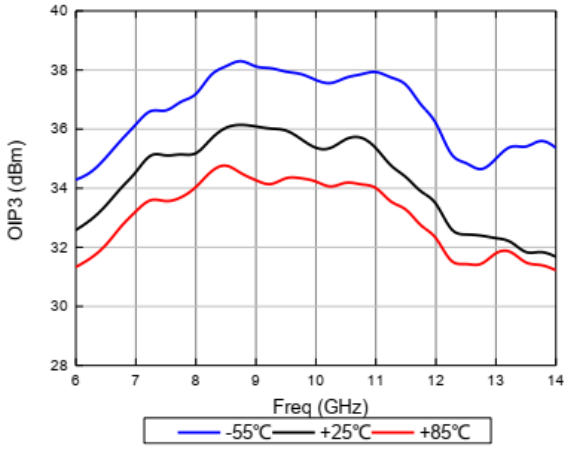


Figure 12. Output third-order intermodulation @Pout=+7dBm

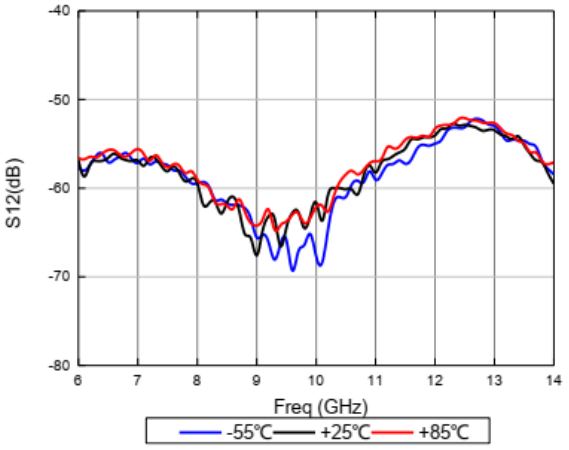
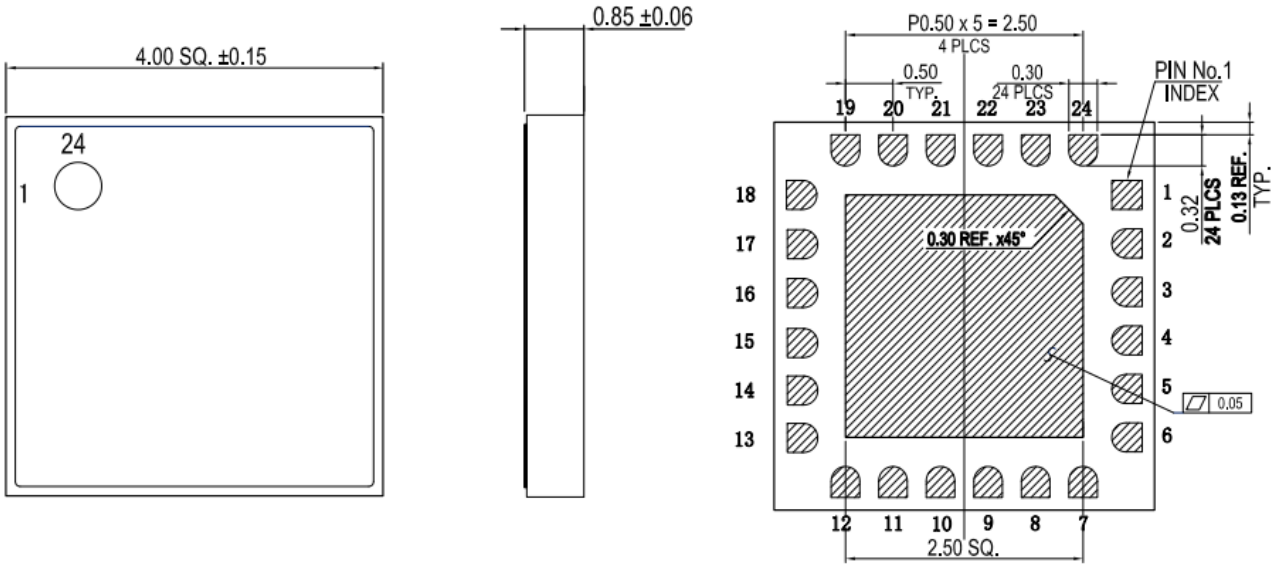


Figure 13. Reverse isolation

IV. Appearance structure diagram (unit: mm)



TOP VIEW SIDE VIEW BOTTOM VIEW

Figure 14.

V. Pin Definition

Table 3

PORT NUMBER	PORT NAME	DEFINITION	SIGNAL OR VOLTAGE
3	IN	RF signal input, integrated DC blocking capacitor	RF
16	OUT	RF signal output, integrated DC blocking capacitor	RF
20	VD	Drive the positive drain	+5V
2, 4, 15, 17, ePAD	GND	The bottom of the chip needs to be well grounded to RF and DC	/
1, 5~14, 18, 19, 21~24	N/C	Floating,recommended to be grounded	/

VI. Recommended assembly drawing

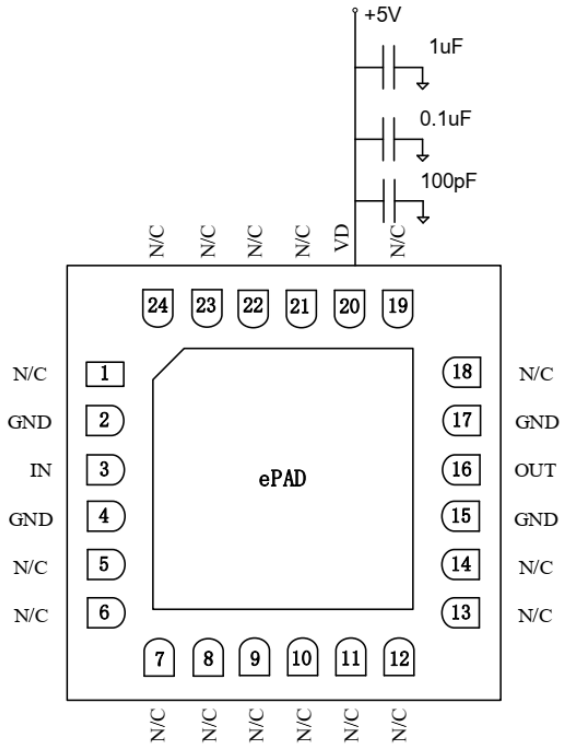


Figure 15.

VII. Precautions

- Assemble and use in a clean environment;
- Sealing material: Ceramic material that meets ROSH standards;
- Lead frame material: copper alloy;
- Lead surface plating: gold, gold layer thickness greater than 1.5um;
- Maximum reflow peak temperature: 260 ℃;
- This product is an electrostatically sensitive device, please be careful to prevent static electricity during storage and use;
- Store in a dry, nitrogen environment;
- Do not attempt to clean the chip surface with dry or wet chemical methods.