BSTCH28Dxx

DC/DC Converter

Data Sheet v.1.0

I. Scope

This specification defines the detailed requirements for hybrid integrated circuits BSTCH28D05, BSTCH28D12 and BSTCH28D15 type DC/DC converters (hereinafter referred to as circuits).

II. Referenced Files

The relevant clauses in the following documents, through reference, become clauses of this specification. For dated or version-referenced documents, subsequent amendments (excluding errata) do not apply to this specification; however, parties using this specification are encouraged to explore the possibility of using the latest version. For undated or version-referenced documents, the latest version applies.

- GB/ T 15138-1994 Outline dimensions of film integrated circuits and hybrid integrated circuits
- GB/T 1804-2000 General tolerances for linear and angular dimensions where no tolerance is specified.
- GJB 548 B-2005 Test methods and procedures for microelectronic devices
- GJB 2438A- 2002 Hybrid Integrated Circuit General Specification

III. Require

3.1. General Principles

The circuit shall comply with all requirements specified in this specification and GJB 2438A-2002. In case of any inconsistency between the requirements of this specification and the general specification, this specification shall prevail.

3.2. Design, Structure and Dimensions

Process Structure

This circuit uses thick-film hybrid integrated circuit technology and is packaged in a fully sealed metal casing.

3.2.2. Product Weight

Product weight: No more than 15g.

3.2.3. Absolute Maximum Rated Value

• Input voltage (V_I)	52V;
• Lead soldering temperature (T_h)	300℃(10s);
• Storage temperature range (T_{stg})	-65℃ ～ 150℃.

3.2.4. Recommended Working Conditions

• Input voltage range (V_I)	12V ～ 50V;
• Operating temperature range (T_c)	-55℃ ～ 125℃.

3.2.5. External Dimensions

The external dimensions shall conform to the provisions of GB/T 15138 and Figure 1.

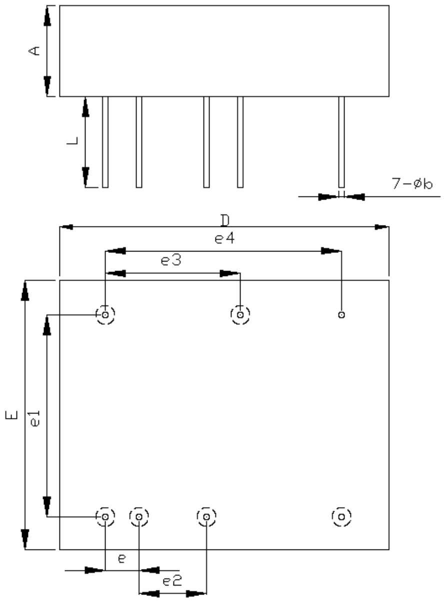

Figure 1. External Dimensions

Table 1

The unit is millimeters

DIMENSIONS SYMBOLS	NUMERICAL		
	MINIMUM	**MINIMUM**	**MINIMUM**
A	-	-	6.90
ϕb	0.40	-	0.50
D	-	-	24.87
E	-	-	20.42
E	-	2.54	-
e_1	-	15.24	-
e_2	-	5.08	-
e_3	-	10.16	-
e_4	-	17.78	-
L	6.61	-	7.11
Notes: 1. Unspecified tolerances shall comply with GB/T m-level execution in 1804-2000; 2. The interchangeability dimensions of e, e1 to e4 are guaranteed by the housing manufacturing process and are not subject to assessment requirements in this specification.			

3.2.6. Arrangement of leads

The lead-out terminals should be arranged as specified in Figure 2.

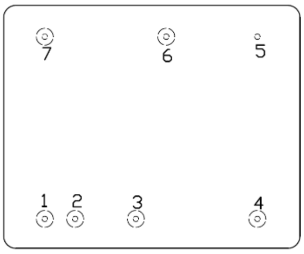

Figure 2. Arrangement of lead-out ends (top view)

Table 2

Lead-out serial number	symbol	Function	Lead-out serial number	symbol	Function
1	V_I	Input positive	5	CASE	Case
2	GND_I	Input common	6	V_{O-}	Output negative
3	V_O	Output positive	7	INH	Inhibit
4	GND_O	Output common	-	-	-

3.3. Electrical Properties

The electrical characteristics shall conform to the specifications in Table 1.

Table 3a. Electrical characteristics (BSTCH28D05)

CHARACTERISTIC	SYMBOL	CONDITION (UNLESS OTHERWISE SPECIFIED) -55°C ≤ T_C ≤ 125°C V_I = 28V±0.5 V, C_L = 0.1μF)	GROUP A GROUPING	LIMIT VALUE		UNIT
				MINIMUM	MAXIMUM	
Output voltage	V_{O1}	V_I =12V ~ 50V, I_{O1} = I_{O2} =150mA	1	4.95	5.05	V
			2,3	4.80	5.20	
	V_{O2}		1	-5.05	-4.95	
			2,3	-5.20	-4.80	
Output current	I_{O1} I_{O2}	V_I = 12V～50V	1,2,3	-	150	mA
Output ripple voltage (Peak-to-peak value)	V_{RIP1}	I_{O1} = I_{O2} =150mA, BW≤ 20MHz	1	-	50	mV
	V_{RIP2}		2,3	-	60	
Voltage regulation	S_{V1} S_{V2}	V_I =12V→50V, I_{O1} = I_{O2} =150mA	1,2,3	-	50	mV
Current regulation	S_{I1} S_{I2}	I_{O1} = I_{O2} = 0mA → 150mA, both outputs change simultaneously.	1,2,3	-	50	mV
Input current	I_I	No load, prohibit the connection of the terminal to the input ground terminal.	1,2,3	-	10	mA
		No load, no open circuit allowed		-	20	
Input ripple current (peak-to-peak value)	I_{RIP}	BW ≤ 20MHz, I_{O1} = I_{O2} =150mA	1	-	30	mA
			2,3	-	40	
efficiency	η	I_{O1} = I_{O2} = 150mA	1	70	-	%
			2,3	65	-	
Insulation resistance	R_I	Apply 500VDC between the input/output terminals or between any of the leads (except for terminal 5) and the casing. T_A = 25℃	1	100	-	MΩ
Short-circuit power consumption	P_D	Output short circuit	1,2,3	-	4	W
Startup threshold	VION	Input voltage from 0V → 12V	1,2,3	6.5	11.8	V
Capacitive load [a]	C_{L1} C_{L2}	It has no effect on DC parameters, T_A = 25℃	4	-	500	μF
Switching frequency	f_S	I_{O1} = I_{O2} = 150mA	4,5,6	325	475	kHz

Output voltage change (peak value) during load transients [bc]	V_{LT1} V_{LT2}	50% load → Full load or Full load → 50% load Each output has a balanced load.	4,5,6	-300	300	mV
Recovery time of output voltage during load transients (bcd)	t_{LT1}	50% load → Full load or Full load → 50% load Each output has a balanced load.	4	-	500	μs
	t_{LT2}		5,6	-	1000	
Output voltage change (peak value) during input voltage transients [be]	V_{VT1} V_{VT2}	Input voltage V_I: 12V→ 50V, $I_{O1} = I_{O2}$ = 150mA	4,5,6	-400	400	mV
Output voltage recovery time during input voltage transient [bde]	t_{VT1}	Input voltage V_I: 12V→ 50V, $I_{O1} = I_{O2}$ = 150mA	4	-	850	μs
	t_{VT2}		5,6	-	1200	
Startup delay [f]	t_{d1} t_{d2}	Input voltage V_I: 0V→28V, $I_{O1} = I_{O2}$ = 150mA	4,5,6	-	20	ms
Start-up overshoot (peak value)	V_{TO1} V_{TO2}	Input voltage V_I: 0V→28V, $I_{O1} = I_{O2}$ = 150mA	4,5,6	-	25	mV

a. Capacitive load can be any value from 0 to the maximum limit, without affecting DC parameters;
b. This parameter is guaranteed by design and is only tested during the initial quality conformity inspection and design or process changes.
c. The jump time of the load should be greater than 10μs;
d. The recovery time refers to the time from the start of the jump until the output voltage returns to within ±1% of the corresponding stable value;
e. The jump time of the input voltage should be greater than 10μs;
f. The start-up delay time can be calculated either from the power supply transition or from when the grounded prohibition terminal is disconnected.

Table 3b. Electrical characteristics (BSTCH28D12)

CHARACTERISTIC	**SYMBOL**	**CONDITION (UNLESS OTHERWISE SPECIFIED) -55°C ≤ T_C ≤ 125°C V_I = 28V±0.5 V, C_L = 0.1μF)**	**GROUP A GROUPING**	**LIMIT VALUE**		**UNIT**
				MINIMUM	**MAXIMUM**	
Output voltage	V_{O1}	V_I =12V ~ 50V, $I_{O1} = I_{O2}$ =63mA	1	11.88	12.12	V
			2,3	11.52	12.48	
	V_{O2}		1	-12.12	-11.88	
			2,3	-12.48	-11.52	
Output current	I_{O1} I_{O2}	V_I = 12V～50V	1,2,3	-	63	mA
Output ripple voltage (Peak-to-peak value)	V_{RIP1}	$I_{O1} = I_{O2}$ =63mA, BW≤ 20MHz	1,2,3	-	100	mV
	V_{RIP2}		1,2,3	-	100	
Voltage regulation	S_{V1} S_{V2}	V_I =12V→50V, $I_{O1} = I_{O2}$ =63mA	1,2,3	-	50	mV

CHARACTERISTIC	SYMBOL	CONDITION (UNLESS OTHERWISE SPECIFIED) $-55°C \leq T_C \leq 125°C$ $V_I = 28V \pm 0.5$ V, $C_L = 0.1μF$)	GROUP A GROUPING	LIMIT VALUE		UNIT
				MINIMUM	MAXIMUM	
Current regulation	S_{I1} S_{I2}	$I_{O1} = I_{O2}$ = 0mA → 63mA, both outputs change simultaneously.	1,2,3	-	50	mV
Input current	I_I	No load, prohibit the connection of the terminal to the input ground terminal.	1,2,3	-	10	mA
		No load, no open circuit allowed		-	20	
Input ripple current (peak-to-peak value)	I_{RIP}	BW ≤ 20MHz, $I_{O1} = I_{O2}$ =63mA	1	-	30	mA
			2,3	-	40	
efficiency	η	$I_{O1} = I_{O2}$ = 63mA	1	72	-	%
			2,3	67	-	
Insulation resistance	R_I	Apply 500VDC between the input/output terminals or between any of the leads (except for terminal 5) and the casing. T_A =25℃	1	100	-	MΩ
Short-circuit power consumption	P_D	Output short circuit	1,2,3	-	4.5	W
Startup threshold	V_{ION}	Input voltage from 0V → 12V	1,2,3	6.5	11.8	V
Capacitive load [a]	C_{L1} C_{L2}	It has no effect on DC parameters, T_A = 25℃	4	-	200	μF
Switching frequency	f_s	$I_{O1} = I_{O2}$ = 63mA	4,5,6	325	475	kHz
Output voltage change (peak value) during load transients [bc]	V_{LT1} V_{LT2}	50% load → Full load or Full load → 50% load Each output has a balanced load.	4,5,6	-300	300	mV
Recovery time of output voltage during load transients (bcd)	t_{LT1}	50% load → Full load or Full load → 50% load Each output has a balanced load.	4	-	400	μs
	t_{LT2}		5,6	-	800	
Output voltage change (peak value) during input voltage transients [be]	V_{VT1} V_{VT2}	Input voltage V_I: 12V→ 50V, $I_{O1} = I_{O2}$ = 63mA	4,5,6	-600	600	mV
Output voltage recovery time during input voltage transient [bde]	t_{VT1}	Input voltage V_I: 12V→ 50V, $I_{O1} = I_{O2}$ = 63mA	4	-	600	μs
	t_{VT2}		5,6	-	1200	
Start-up overshoot (peak value)	V_{TO1} V_{TO2}	Input voltage V_I: 0V→28V, $I_{O1} = I_{O2}$ = 63mA	4,5,6	-	50	mV
Startup delay [f]	t_{d1} t_{d2}	Input voltage V_I: 0V→28V, $I_{O1} = I_{O2}$ = 63mA	4,5,6	-	20	ms

a. Capacitive load can be any value from 0 to the maximum limit, without affecting DC parameters;
b. This parameter is guaranteed by design and is only tested during the initial quality conformity inspection and design or process changes.
c. The jump time of the load should be greater than 10μs;

CHARACTERISTIC	SYMBOL	CONDITION (UNLESS OTHERWISE SPECIFIED) -55°C ≤ T_C ≤ 125°C V_I = 28V±0.5 V, C_L = 0.1μF)	GROUP A GROUPING	LIMIT VALUE		UNIT
				MINIMUM	MAXIMUM	
d. The recovery time refers to the time from the start of the jump until the output voltage returns to within ±1% of the corresponding stable value; e. The jump time of the input voltage should be greater than 10μs; f. The start-up delay time can be calculated either from the power supply transition or from when the grounded prohibition terminal is disconnected.						

Table 3c. Electrical characteristics (BSTCH28D15)

CHARACTERISTIC	SYMBOL	CONDITION (UNLESS OTHERWISE SPECIFIED) -55°C ≤ T_C ≤ 125°C V_I = 28V±0.5 V, C_L = 0.1μF)	GROUP A GROUPING	LIMIT VALUE		UNIT
				MINIMUM	MAXIMUM	
Output voltage	V_{O1}	V_I =12V ~ 50V, I_{O1} = I_{O2} =50mA	1	14.85	15.15	V
			2,3	14.40	15.60	
	V_{O2}		1	-15.15	-14.85	
			2,3	-15.60	-14.40	
Output current	I_{O1} I_{O2}	V_I = 12V～50V	1,2,3	-	50	mA
Output ripple voltage (Peak-to-peak value)	V_{RIP1}	I_{O1} = I_{O2} =50mA, BW≤ 20MHz	1,2,3	-	100	mV
	V_{RIP2}		1,2,3	-	100	
Voltage regulation	S_{V1} S_{V2}	V_I =12V→50V, I_{O1} = I_{O2} =50mA	1,2,3	-	50	mV
Current regulation	S_{I1} S_{I2}	I_{O1} = IO2 = 0mA → 50mA, both outputs change simultaneously.	1,2,3	-	50	mV
Input current	I_I	No load, prohibit the connection of the terminal to the input ground terminal.	1,2,3	-	10	mA
		No load, no open circuit allowed		-	20	
Input ripple current (peak-to-peak value)	I_{RIP}	BW ≤ 2 0MHz, I_{O1} = I_{O2} =50mA	1	-	30	mA
			2,3	-	40	
Efficiency	η	I_{O1} = I_{O2} = 50mA	1	72	-	%
			2,3	67	-	
Insulation resistance	R_I	Apply 500VDC between the input/output terminals or between any of the leads (except for terminal 5) and the casing. T_A = 25℃	1	100	-	MΩ
Short-circuit power consumption	P_D	Output short circuit	1,2,3	-	4.5	W
Startup threshold	V_{ION}	Input voltage from 0V → 12V	1,2,3	6.5	11.8	V
Capacitive load [a]	C_{L1} C_{L2}	It has no effect on DC parameters, T_A = 25℃	4	-	200	μF
Switching frequency	f_S	I_{O1} = I_{O2} = 50mA	4,5,6	325	475	kHz

CHARACTERISTIC	SYMBOL	CONDITION (UNLESS OTHERWISE SPECIFIED) -55°C ≤ T_C ≤ 125°C V_I = 28V±0.5 V, C_L = 0.1μF)	GROUP A GROUPING	LIMIT VALUE		UNIT
				MINIMUM	MAXIMUM	
Output voltage change (peak value) during load transients [bc]	V_{LT1}	50% load → Full load or Full load → 50% load Each output has a balanced load.	4,5,6	-300	300	mV
	V_{LT2}					
Recovery time of output voltage during load transients (bcd)	t_{LT1}	50% load → Full load or Full load → 50% load Each output has a balanced load.	4	-	400	μs
	t_{LT2}		5,6	-	800	
Output voltage change (peak value) during input voltage transients [be]	V_{VT}	Input voltage V_I: 12V→ 50V, $I_{O1} = I_{O2}$ = 50mA	4,5,6	-600	600	mV
Output voltage recovery time during input voltage transient [bde]	t_{VT}	Input voltage V_I: 12V→ 50V, $I_{O1} = I_{O2}$ = 50mA	4	-	600	μs
			5,6	-	1200	
Start-up overshoot (peak value)	V_{TO1}	Input voltage V_I: 0V→ 28V, $I_{O1} = I_{O2}$ = 50mA	4,5,6	-	50	mV
	V_{TO2}					
Startup delay [f]	t_{d1}	Input voltage V_I: 0V→ 28V, $I_{O1} = I_{O2}$ = 50mA	4,5,6	-	20	ms
	t_{d2}					

a. Capacitive load can be any value from 0 to the maximum limit, without affecting DC parameters;
b. This parameter is guaranteed by design and is only tested during the initial quality conformity inspection and design or process changes.
c. The jump time of the load should be greater than 10μs;
d. The recovery time refers to the time from the start of the jump until the output voltage returns to within ±1% of the corresponding stable value;
e. The jump time of the input voltage should be greater than 10μs;
f. The start-up delay time can be calculated either from the power supply transition or from when the grounded prohibition terminal is disconnected.

3.4. Electrical Testing Requirements

Electrical testing requirements should be in the groupings specified in Table 4.

Table 4. Electrical Testing Requirements

Test conditions	Group (According to GJB 2438A-2002 Table C11)
Final electrical test (after aging)	A1[a], A 2, A 3, A4, A5, A6
A test requirements	A1, A 2, A 3, A4, A5, A6
C Endpoint Electrical Test	A1

[a] PDA is suitable for A1 grouping

IV. Quality Assurance Regulations

4.1. Sampling and Inspection

Unless otherwise specified, sampling and inspection procedures shall be in accordance with Appendix F of GJB 2438A-2002 and the provisions of this specification.

4.2. Screening

Before qualification and quality consistency inspection, all circuits should be screened according to the provisions of C.4 in GJB 2438A-2002 and Table 5 of this specification.

Table 5. Screening

TEST	GJB 548B-2005		REQUIRE
	METHOD	STRIP ITEM	
Internal visual inspection	2017		100%
Temperature Cycle	1010	Condition C, -65^{0}_{-10}℃～-150^{+15}_{0}℃ 10 times, t1 = 30min ±1min, t2 ≤1min	100%
constant acceleration	2001	Acceleration 29400m/$s^{2,}$ Y1 direction, 1min	100%
PIND	2020	Condition A	100%
Aging	1015	T_C = 125°C, 160h (Aging diagram see Figure 4)	100%
Final electrical test	-	Should comply with the requirements of Table 2	100%
seal a. Detailed leak inspection b. Rough leak detection	1014	Detailed inspection test conditions A1, pressure: 310kPa, time: 10h, R_1 ≤5×10^{-3} (Pa·$cm^{3)}$/s (He) Rough test conditions C1, pressure: 310kPa, time: 8h	100%
External visual inspection	2009		100%

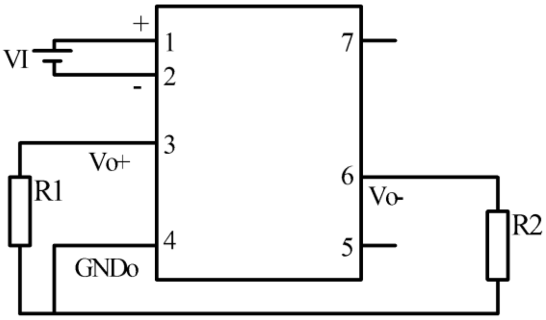

Figure 3. Flowchart of aging and steady-state life test

V_I = 28V±0.5V

BSTCH2805DR_1=R_2=34Ω±1Ω

BSTCH2812DR_1=R_2=192Ω±1Ω

BSTCH2815DR_1=R_2=300Ω±1Ω

4.3. Identification and Testing

The identification and testing shall be conducted in accordance with the provisions of this standard, and the tests performed shall meet the requirements of Groups A, B, C, and D of this standard. The minimum number of samples required for Group A testing shall not be less than the sum of the number of samples specified for Groups B, C, and D.

4.4. Quality Consistency Inspection

4.4.1. Overview

Quality consistency inspection shall be carried out in accordance with the provisions of C.5 in GJB 2438A-2002 and this specification, and the inspection shall conform to the A, B, C and D group inspections specified in this specification.

4.4.2. Group A Test

Group A testing shall be conducted in accordance with the provisions of Table C.11 in GJB 2438A-2002 and Table 6 of this specification; when the required sample size exceeds the batch size, 100% testing shall be performed.

Table 6. Group A test

GROUPING	PARAMETER	NUMBER OF SAMPLES (NUMBER OF RECEPTIONS)
1	Static test at 25℃	116(0)
2	Static test at 125℃	76(0)
3	Static test at -55℃	45(0)
4	Dynamic test at 25℃	116(0)
5	Dynamic test at 125℃	76(0)
6	Dynamic test at -55℃	45(0)

4.4.3. Group B test

Group B inspection shall be conducted in accordance with the provisions 2438Aof C in GJB-2002 5.3.2and Table 7 of this specification.

Table 7. Group B test

GROUPING	TEST	GJB 548B-2005		SAMPLE SIZE (NUMBER OF RECEIVED)
		METHOD	CONDITION	
1	External dimensions and Product weight	2016	Complies with Article 3.2.5 It complies with the provisions of clause 3.2.2.	2 (0)
3	Solvent resistance [a]	2015	—	3 (0)
4	Internal visual inspection and Structural inspection	2014	—	1 (0)
5	Bond strength a) Hot-press welding b) Ultrasonic welding	2011	D	2 (0)
6	Chip shear strength	2019	—	2 (0)
7	Solderability	2003	Solder temperature 245℃ 5℃± Water vapor aging 8h	1 (0)
9	ESD [b] Electrical parameters ESDS Electrical parameters	3015	Group A1 2000V Group A1	3 (0)
10	Surge resistance test [c]	This specification Appendix B	At 25 ℃ and full load, surge voltage is 80V and time is 1s.	
a. This test item is not applicable to laser marking products; b. ESD is only performed during qualification testing or design changes; c. Group B10 will be conducted before Group B9.				

4.4.4. Group C Test

Group C tests shall 2438Abe conducted in accordance with the provisions of Table C.14 and below in GJB-2002.

Table 8. Group C test

GROUPING	TEST	GJB 548B-2005		SAMPLE SIZE (NUMBER OF RECEIVED)
		METHOD	CONDITION	
1	External visual inspection	2009	—	5 (0)
	Temperature Cycling	1010	Same as table 3	
	Constant acceleration	2001	Same as table 3	
	Seal	1014	Same as table 3	
	PIND	2020	Same as table 3	
	Visual inspection	1010	—	

GROUPING	TEST	GJB 548B-2005		SAMPLE SIZE (NUMBER OF RECEIVED)
		METHOD	CONDITION	
	End-point electrical test	—	It should meet the requirements of Table 2 of this specification.	
2	Steady-state lifetime	1005	T_C = 125°C, 1000h (Experimental flowchart shown in Figure 3)	5 (0)
	End-point electrical test	—	It should meet the requirements of Table 2 of this specification.	
3	Internal water vapor content	1018	100°C	3 (0) or 5 (1)

4.4.5. Group D Test

Group D testing shall be 2438Aconducted in accordance with the provisions of Table C.15 in GJB-2002 and the following provisions. Group D testing may use non-conforming electrical products or sealed empty shells that have been screened in the same inspection batch.

Table 9. Group D Test

GROUPING	TEST	GJB 548B-2005		SAMPLE SIZE (NUMBER OF RECEIVED)
		METHOD	CONDITION	
1	thermal shock	1011	C, 15 cycles	5 (0)
	Stability baking	1008	150°C, 1 h	
	Lead wire strength	2004	B2 (Leader fatigue)	1 (0)
	Seal	1014	Same as table 3	5 (0)
2	Moisture resistant	1004	—	5 (0)
3	Salt spray	1009	Condition A	5 (0)
4	Insulation resistance	1003	500V, maximum 80 nA	3 (0)

4.5. Test Methods

Unless otherwise specified, electrical parameters shall be tested in accordance with SJ20646 "Test Methods for Hybrid Integrated Circuit DC/DC Converters" and Appendix A.

4.6. Surge Resistance Test

Surge resistance testing shall be conducted in accordance with Appendix B.

V. Delivery preparation

Packaging requirements shall comply with the provisions of Clause 5.1 of GJB 2438A-2002.

VI. Explanation

6.1. Intended Use

Circuits conforming to this specification are intended for use in the design of new equipment and for logistical support of existing equipment.

6.2. Order Document Content

The contents of contracts and purchase orders should comply with GJB. The provisions of Article 2438A6.2 of 2002.

6.3. Quality Control Level

Product quality control 2438Ashall be carried out in accordance with the H-level requirements in GJB-2002.

Appendix A. (Normative Appendix)

Test methods

A.1. Testing Instruments

Table A.1. Test Instruments

NAME	QUANTITY	REMARK
DC power supply	2	
Digital multimeter	4	
Oscilloscope	1	Four-channel
Electronic load	1	Dual-path
surge generator	1	
Insulation resistance tester	1	

A.2. Test Fixture Connection Diagram

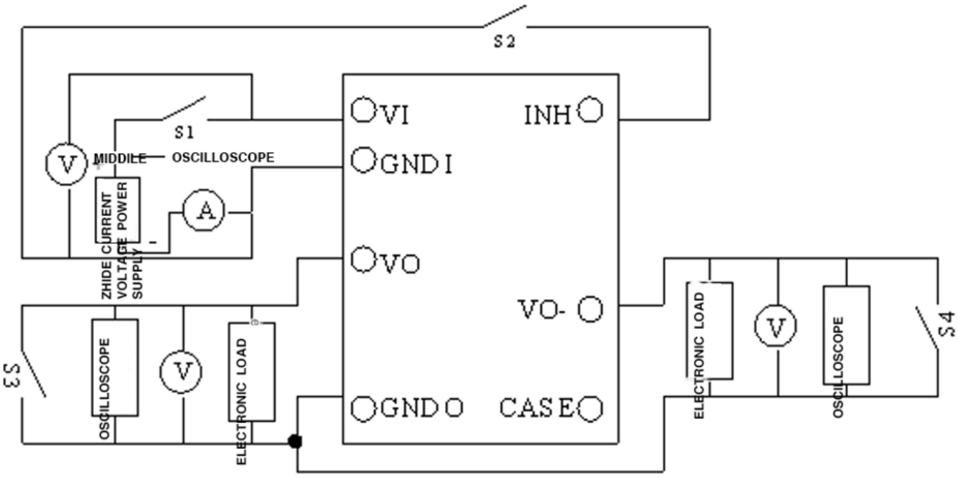

Figure A.1. Connection diagram of the test fixture

A.3. Test Method

A.3.1. Output voltage (V_O)

A.3.1.1. Test conditions

- V_I = 12 V ~ 50 V;

The electronic load is adjusted to a constant output current I0.

A.3.1.2. Test program

- Connect the device under test (DUT) to the test system;

- Set switch S1 as shown in Figure A.1 to the ON position to apply the specified DC input voltage to the DUT input terminal;
- Directly measure the output voltage V_O.

A.3.2. Output current (I_O)

A.3.2.1. Test conditions

A.3.2.2. Test program

- Connect the device under test (DUT) to the test system;
- Set switch S1 as shown in Figure A.1 to the ON position to apply the specified DC input voltage to the DUT input terminal;
- Read the output current value directly.

A.3.3. Output ripple voltage (VRIP)

A.3.3.1. Test conditions

- V_I = 28V ± 0.5V;

The electronic load is adjusted to a constant output current I0.

A.3.3.2. Test program

With switch S1 in the ON position, use an analog oscilloscope at the 20MHz setting to measure the peak-to-peak value of the output ripple voltage, which is the output ripple voltage. Connect C1=0.1μF to the test point, and keep capacitor C1 as close as possible to the oscilloscope probe (Figure A.2).

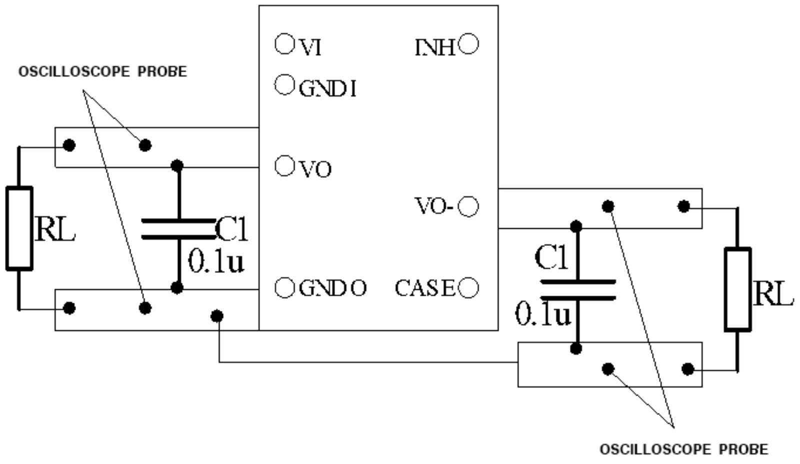

Figure A.2. Output ripple test diagram

A.3.4. Voltage regulation (SV)

A.3.4.1. Test conditions

Same as A.3.1.1.

A.3.4.2. Test program

- a) Connect the DUT to the test system;
- b) Set switch S1 as shown in Figure A.1 to the ON position, so that the specified DC input voltage of 28V is applied to the input terminal of DUT;
- c) The output voltage at this time is V0;
- d) Repeat steps b) and c), adjusting the DUT input voltage to 12V and 50V respectively, and measure the output voltage at different input voltages, denoted as V_{ON} and V_{OM} respectively.
- e) Calculate the voltage regulation degree according to formula (1):

$$S_V = \left| V_{ON} - V_{OM} \right| \tag{1}$$

A.3.5. Current Regulation (SI)

A.3.5.1. Test conditions

Same as A.3.3.1.

A.3.5.2. Test program

- Connect the DUT to the test system;
- Set switch S1 as shown in Figure A.1 to the ON position;
- The output voltage at this time is measured to be V_{0L};
- The electronic load is adjusted to a constant output current I_0, and the output voltage is V_{0H};
- Calculate the current regulation according to formula (2):

$$S_I = \left| V_{OL} - V_{OH} \right| \tag{2}$$

A.3.6. Input Current (I I))

A.3.6.1. Test conditions

$V_I = 28V \pm 0.5V$;

A.3.6.2. Test Program

- Connect the DUT to the test system;
- Set the preset value of the electronic load to 0;
- Set switch S1 to the ON position and S2~S4 to the OFF position as shown in Figure A.1. The input current at this time is the input current when the inhibit terminal is open.
- d) Set switches S1 and S2 to the ON position and S3 to the OFF position as shown in Figure A.1. The input current at this time is the input current when the inhibit terminal is connected to the input ground terminal.

A.3.7. Input Ripple Current (I_{RIP})

A.3.7.1. Test Conditions

Same as A.3.3.1.

A.3.7.2. Test Program

- Connect the DUT to the test system;
- Set switch S1 to the ON position and switches S2 to S4 to the OFF position as shown in Figure A.1;
- When testing with an oscilloscope, set the bandwidth to ≤20MHz, select a high-impedance probe, choose an appropriate coupling method, adjust the X and Y axis resolution knobs to appropriate positions, and adjust the oscilloscope trigger level to an appropriate position; the peak-to-peak value of the ripple current measured by the current probe at the input terminal is the input ripple current I_{RIP}.

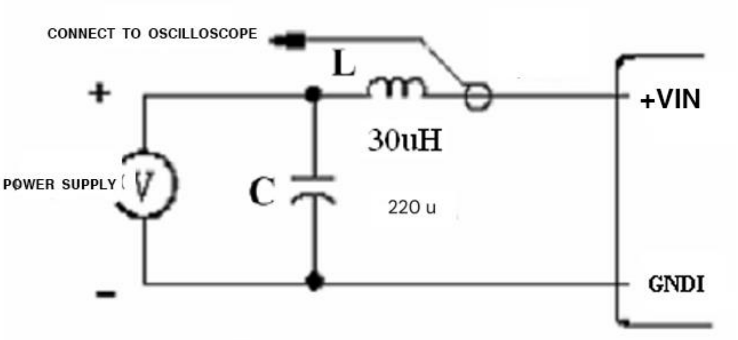

Figure A.3. Ripple current test method

A.3.7.3. Precautions

- Set the oscilloscope voltage to 20 mA/div;

- When testing this item, an LC filter can be connected to the input terminal, as shown in Figure A.3;
- The current probe should be placed as close as possible to the product pins.

A.3.8. Efficiency (η)

A.3.8.1. Test Conditions

Same as A.3.3.1.

A.3.8.2. Test Procedure

With switch S1 in the ON position, under specified test conditions, measure the input voltage V_I and input current II. Measure the output voltage and current at the output terminal: V_0 and I_0, respectively. The efficiency is:

$$\eta = \frac{V_O \times I_O}{V_I \times I_I} \times 100\% \qquad (3)$$

A.3.9. Insulation resistance (R_I)

A.3.9.1. Test Conditions

The insulation resistance tester has a voltage V = 500V.

A.3.9.2. Test Procedure

a D_C voltage of 500V between the input and output terminals, or between any lead (except pin 5) and the casing, for 3 seconds, and measure the insulation resistance value using an insulation resistance tester.

A.3.10. Short -circuit power consumption (PD)

A.3.10.1. Test conditions: Connect the external circuit as shown in Figure A.1.

Same as 3.1.1.

A.3.10.2. Test Procedure

- Connect the DUT to the test system;
- S1 as shown in Figure A.1 to the ON position;
- After the product is operating stably, turn switches S3 and S4 to the ON position and measure the input voltage V_I and input current I_I respectively. The short - circuit power consumption is:

$$P_D = V_I \times I_I \qquad (4)$$

A.3.10.3. Precautions

- The short-circuit time should not exceed 5 seconds;
- Repeated short-circuit operations should be avoided.

A.3.11. Start-up Threshold (V_{ION})

A.3.11.1. Test Conditions

Same as A.3.3.1.

A.3.11.2. Test Procedure

- Connect the DUT to the test system;
- Set switch S1 as shown in Figure A.1 to the ON position;
- Adjust the input voltage downwards until the output voltage becomes 0, then adjust the input voltage upwards and record the input voltage when the output is normal. This is the start-up threshold V_{ION}.

A.3.12. Capacitive Load (C_L)

A.3.12.1. Test Conditions: Connect the External Circuit as Shown in Figure A.1.

Same as 3.1.1.

A.3.12.2. Test Program

- Connect the DUT to the test system;
- Connect the output to a capacitor of the specified capacitance value and set the switch S1 shown in Figure A.1 to the ON position;
- The output voltage should meet the specifications after stable operation.

A.3.13. Switching Frequency (f_S)

A.3.13.1. Test conditions: Connect the external circuit as shown in Figure A.1.

Same as 3.1.1.

A.3.13.1. Test program

a) Connect the DUT to the test system;

b) Set switch S1 as shown in Figure A.1 to the ON position;

c) Measure the frequency corresponding to the output ripple voltage with an oscilloscope, which is the switching frequency fs.

A.3.14. Output Voltage Change During Load Transients (V_{LOR})

A.3.14.1. Test conditions: Connect the external circuit as shown in Figure A.1.

- Input voltage V_I = 28V ± 0.5V, supplied by a DC regulated power supply.
- Switches S1 to S4 are in the OFF position.

A.3.14.2. Test Program

- Connect the OUT to the test system;
- Set the initial load voltage, load rate, and load current of the electronic load: specify the current value and set the operating mode of the electronic load to dynamic output;
- Adjust the X and Y knobs of the oscilloscope channel to the appropriate positions, select single or normal DC coupling mode and trigger mode, and select the appropriate voltage bias and trigger level;
- Set switch S1 as shown in Figure A.1 to the ON position;
- When the output load changes abruptly, the maximum change in output voltage is V LOR, as shown in Figure A.4.

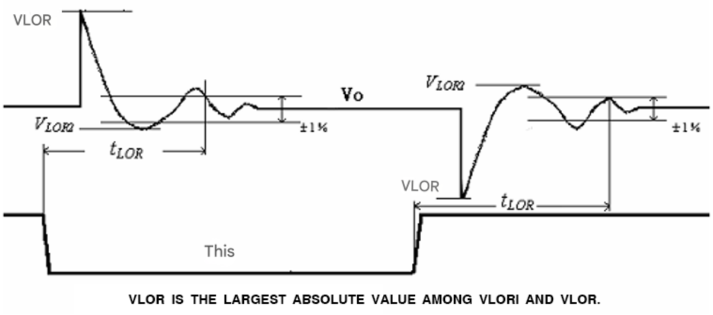

Figure A.4 Output voltage response V_{LOR} during load transient, output voltage recovery time t_{LOR}

A.3.14.3. Precautions

- To reduce the influence of other factors on the test results, it is best to remove the voltmeters and ammeters at the input and output terminals;
- The load current jump loading time is greater than 10μs and less than 40% of the output voltage recovery time during load transients. Generally, it is taken as 20 to 50 times the switching transistor's duty cycle.
- The output current can be no-load, half-load, full-load, or other values, while the input voltage is generally the rated input voltage.

A.3.15. Output Voltage Recovery Time During Load Transients

A.3.15.1. Test Conditions:

Same as 3.14.1

A.3.15.2. Test program

Same as 3.14.2

When the output load changes, the time it takes for the output voltage to recover to its stable value within ±1% of the load range is read from the waveform on the oscilloscope as t_{LOR}, as shown in Figure A.4.

A.3.15.3. Precautions

- Same A.3.14.3;
- The maximum change in output voltage may be less than 1 %, in which case the recovery time is 0.

A.3.16. Output voltage change (V_{VOR}) during input voltage transients

A.3.16.1. Test conditions: Connect the external circuit as shown in Figure A.1.

- Input voltage V_{IL} = 1.2V, V_{IH} = 5.0V.
- Adjust the electronic load to a constant current value as specified;
- Switches S1 to S4 are in the OFF position.

A.3.16.2. Test program

- Connect the OUT to the test system;
- Set the voltage rise rate and output voltage V_{IL} of power supply 1, and the voltage rise rate and output voltage V_{IH} of power supply 2.
- Adjust the X and Y knobs of the oscilloscope channel to the appropriate positions, select single or normal DC coupling mode and trigger mode, and select the appropriate voltage bias and trigger level;
- The output power supply is applied to the input terminal through the analog integrated tester UCS, -500Mand the jump device makes the input voltage VIL and VIH. The transitions between these states are shown in Figure A.5.
- When the input voltage jumps between its maximum and minimum values, the maximum change in the output voltage is V OR, as shown in Figure A.6.

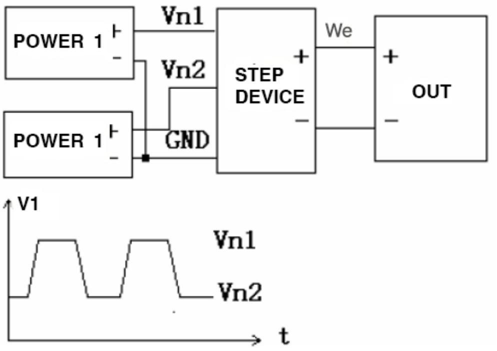

Figure A.5. Input jump device diagram

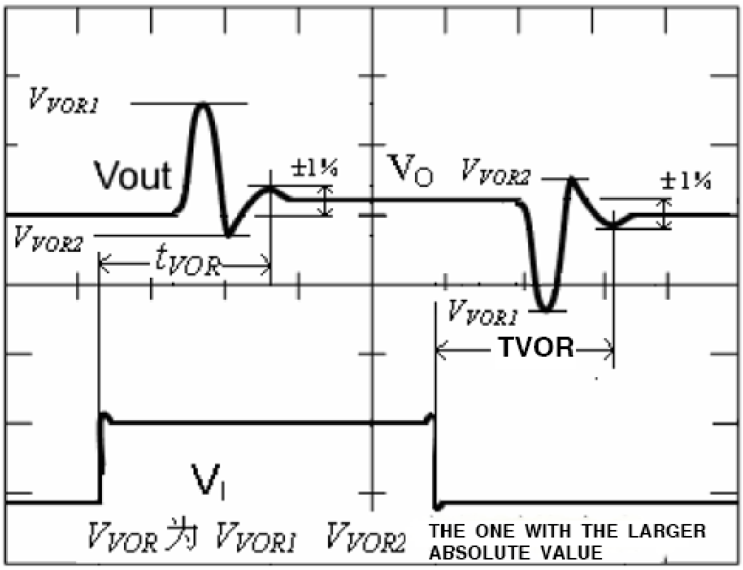

Figure A.6 Output voltage response (peak value) during input voltage transient, V_{OR}, output voltage recovery time. t_{VOR}

A.3.16.3. Precautions

- To reduce the influence of other factors on the test results, it is best to remove the voltmeters and ammeters at the input and output terminals;
- The step change time of the input voltage should be greater than 10μs;
- V_{IH} and V_{IL} are generally the maximum input voltage and minimum input voltage, respectively. I_O can be full load, no load, or other values.
- To avoid overvoltage and undervoltage as shown in the figure generated by the jump device, a capacitor of appropriate capacity can be connected in parallel at the input terminal;

- To eliminate interference, a capacitor of appropriate size can be connected in parallel at the output terminal, but the output main voltage variation curve must not be changed.
- The measurement point is the same as the ripple test measurement point.

A.3.17. Output Voltage Recovery Time During Input Voltage Transients (t_{VOR})

A.3.17.1. Test conditions:

Same as 3.16.1

A.3.17.2. Test Procedure

Same as 3.16.2

t_{VOR} is the time taken for the output voltage to return to its stable value within ± 1 % of the input voltage when the input voltage jumps between its maximum and minimum values, as shown in Figure A.6.

A.3.17.3. Precautions

- Same A.3.16.3;
- The maximum change in output voltage may be less than 1%, in which case the recovery time is 0.

A.3.18. Start-up overshoot (V_{TO})

A.3.18.1. Test Conditions

Same as A.3.1.1.

A.3.18.2. Test Procedure

- Connect the device under test to the test system;
- Adjust the X and Y knobs of the oscilloscope channel to the appropriate positions, select DC coupling mode and trigger mode as single or normal, and select an appropriate trigger level;
- Set switch S1 as shown in Figure A.1 to the ON position to apply the specified DC input voltage to the input terminal of the device under test;
- The startup overshoot voltage V_{TO} from the waveform on the oscilloscope, as shown in Figure A.9.

A.3.18.3. Precautions

- The instantaneous output voltage value during startup may not exceed the stable output value, i.e., startup overshoot is zero;
- The rise time of the power supply voltage should be controlled within the range of 10μs to 500μs;
- Load I_O can be any value from no load to full load, but full load is generally used; when using an electronic load, the initial load level is 10% of the rated output value.
- To reduce the influence of other factors on the test results, it is best to remove the output voltmeter and ammeter;
- In case of dispute, the test results when the load is a purely resistive load shall prevail.

A.3.19. Startup Delay (t_{TR})

A.3.19.1. Test conditions

Same as A.3.1.1.

A.3.19.2. Test Procedure

- Connect the DUT to the test system under the specified temperature conditions;
- Adjust the X and Y knobs of the oscilloscope channel to the appropriate positions, select single or normal DC coupling mode and trigger mode, and select an appropriate trigger level; turn switch S1 shown in Figure A.1 to the ON position, so that the specified DC input voltage is applied to the DUT input terminal;
- The time from when the input voltage begins to step up from the oscilloscope waveform to when the output voltage reaches 90% of its stable value is the start-up delay time t_{TR}, as shown in Figure A.7.

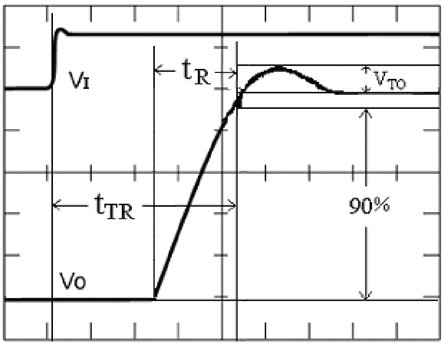

Figure A.7. Schematic diagram of start-up overshoot and start-up delay

A.4. Precautions

1. Do not reverse the positive input terminal and the input ground terminal.

2. During measurement, the voltmeter should be placed as close as possible to the product leads.

3. When measuring output ripple, the oscilloscope probe should be used in a "close-in" measurement manner.

Appendix B.

(Normative Appendix)

Surge resistance test

B.1. Surge Resistance Test

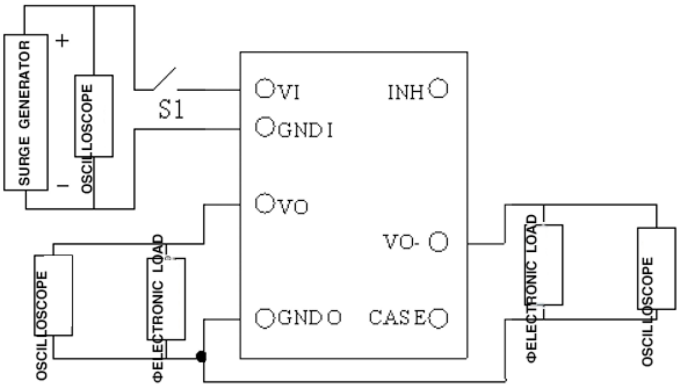

Figure B.1. Surge voltage test fixture connection diagram

B.1.1. Test Conditions:

- V_I = 28V, V_{IM} = 80V, output by the surge generator, with a single surge lasting 1s (T = 1s);
- The electronic load is adjusted to a constant current value according to the specified current.
- Switch S1 is in the OFF position.

B.1.2. Test Procedure

- Connect the device under test to the test system;
- Set the switch S1 shown in Figure B.1 to the ON position;
- The product did not experience any malfunctions after the surge.

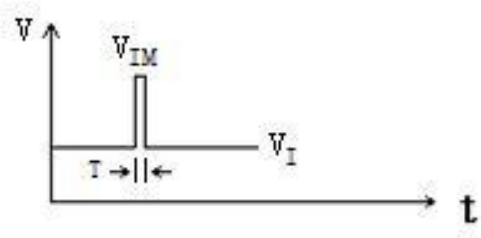

Figure B.2. Surge voltage diagram