BSTCC59-3238

Ka-band four-channel multi-function chip

data sheet

I. Product Introduction

BSTCC59-3238 is a Ka-band four-channel multi-function chip.

3.3V power supply, the operating frequency range is 32GHz ~ 38GHz. The chip integrates low noise amplifier, power amplifier, RF front-end switch, 6 -digital controlled attenuator, 6 -digital controlled phase shifter, power divider, beam control and other modules, which can provide a maximum attenuation range of 31.5dB, step 0.5dB, and a phase shift range of 360°, step 5.6°. BSTCC59-3238 also integrates an 8 -bit ADC circuit, which is suitable for applications such as temperature detection and power detection. BSTCC59-3238 adopts wafer-level WLCSP packaging with a package size of 5.555mm×5.855mm.

II. Application Areas

- Radar
- Communication

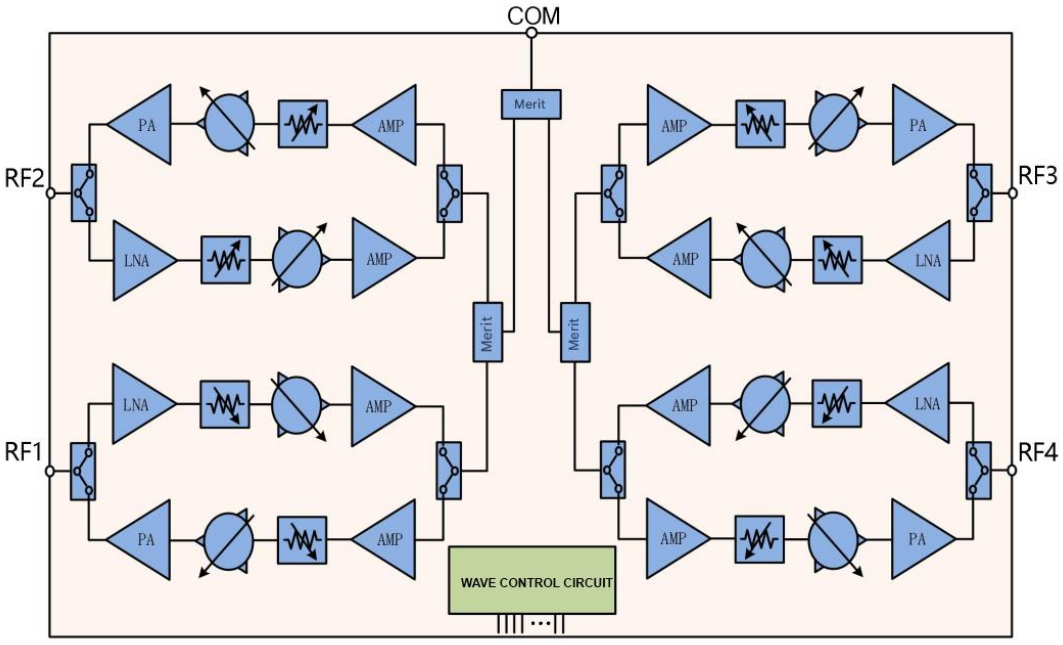


Figure 1. BSTCC59-3238 chip module schematic

III. Key technical indicators

- Working power supply voltage: 3.3V
- Operating frequency range: 32GHz ~ 38GHz
- 6 -bit attenuation control, step 0.5dB
- 6 phase shift control bits, 5.6° step
- Receive gain: 23dB@35GHz

(RFn port to COM port)

- Transmitter linear gain: 26dB@35GHz

(COM port to RFn port)

- Gain flatness in transmit and receive band: 2dB
- Receive noise factor NF: 5.5dB
- Receive input P-1dB: -30dBm
- Transmit output Psat: 21dBm
- RMS phase shift error: < 4°
- Amplitude consistency during phase shift: < ±1dB
- RMS attenuation error: < 2dB
- Attenuation additional phase shift: < ±15°
- Transmit and receive switching time: < 150ns
- Single channel operating current: 65mA/150(360)mA/25mA

@ Receive / Static (21dBm saturation) Transmit / Load

- Chip package and size: WLCSP 5.555mm×5.855mm
- Process: SiGe BiCMOS

IV. Electrical Characteristics

4.1. Basic electrical properties

Table 1.

PARAMETER	CONDITION	MINIMUM	TYPICAL VALUE	MAXIMUM	UNIT
Frequency range		32		38	GHz
Receive linear gain	RFn port to COM port		23		dB
Transmit linear gain	COM port to RFn port		25		dB
In-band gain flatness				3	dB

PARAMETER	CONDITION	MINIMUM	TYPICAL VALUE	MAXIMUM	UNIT
Port VSWR				2	—
Receive noise figure			5.5		dB
Receive input P-1dB			-30		dBm
Transmit output P-1dB			20		dBm
Transmit output Psat	1us pulse width, 10% transmit duty cycle		21		dBm
RMS Phase Shift Error				4	Deg
Phase shift amplitude consistency		-1		1	dB
RMS attenuation error (receive)				1.4	dB
Attenuation of additional phase shift		-15		15	Deg
Transmit/receive switching time				150	ns
Single channel receiving current			65		mA
Single channel static emission current	COM port not activated		150		mA
Single channel saturation emission current	COM port input -1dBm		360		mA
Single channel load current			25		mA

4.2. Digital port electrical parameters

Table 2.

PARAMETER	SYMBOL	CONDITION	MINIMUM	MAXIMUM	UNIT
Input high level voltage	VIH	VCC = 2.7 V to 3.6 V	1.7		V
Input low level voltage	VIL	VCC = 2.7 V to 3.6 V		0.8	V
Input high level current	IIH	VCC = 2.7 V to 3.6 V	-500	500	uA
Input low level current	IIL	VCC = 2.7 V to 3.6 V	-500	500	uA
Output high level voltage	VOH	VCC = 2.7 V to 3.6 V IOH = –100 uA	VCC-0.2	VCC	V
Output high level voltage	VOH	VCC = 2.7 V IOH = –4mA	2.4	VCC	V
Output low level voltage	VOL	VCC = 2.7 V to 3.6 V IOL= 100uA	0	0.2	V
Output low level voltage	VOL	VCC = 2.7 V, IOL = 4 mA	0	0.4	V

4.3. Limit parameters

Table 3.

PARAMETER	VALUE
Maximum supply voltage	3.6V
Maximum RF input power	15dBm
Storage temperature	-65 ～ 150 ℃
Operating temperature	-55 ～ 125 ℃

Note: For the above listed maximum limits, if the device is operated in an environment exceeding these limits, it is likely to cause permanent damage to the device.

In actual application, it is best not to operate the device in an environment where the limit value or the value exceeds this limit value.

4.4. ESD Protection

The anti-static level (HBM) of BSTCC59-3238 is at least Class 2: ≥2000V. When handling, take appropriate ESD protection measures to avoid performance degradation or functional failure.

V. Pin Configuration

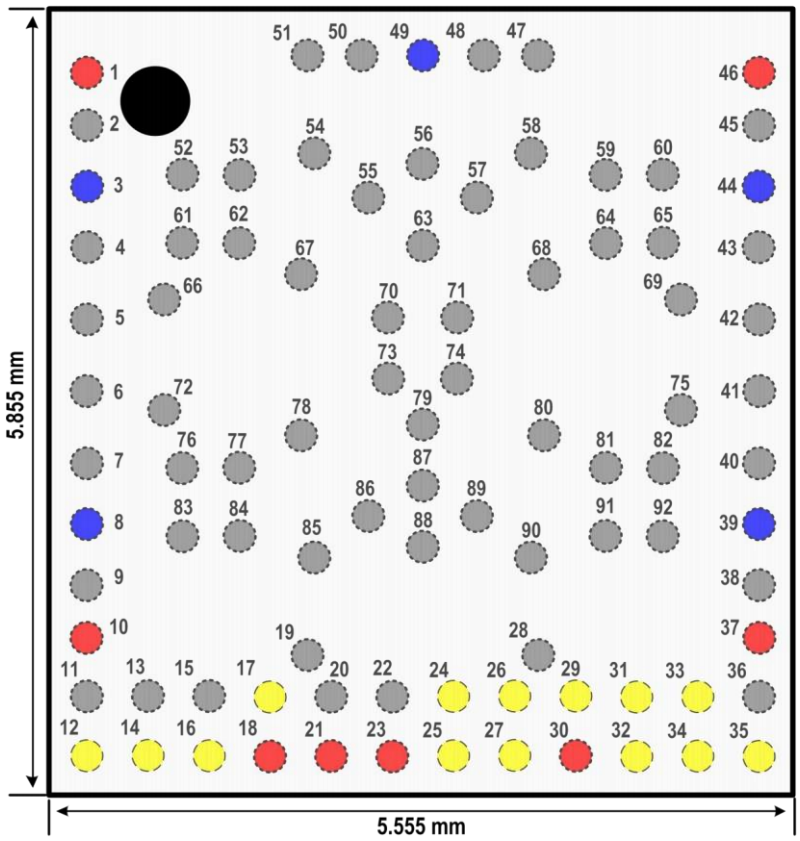


Figure 2. Chip pin layout (top view, pins at the bottom)

Chip pad function information table (the lower left corner of the back view is the coordinate origin)

Table 4.

PAD NUMBER	PAD NAME	X -AXIS COORDINATE (UM)	Y- AXIS COORDINATE (UM)	REMARK
1	VDD33_L2	330	5380.87	Channel three 3.3V power supply
2	GND	330	4993.37	Ground pad next to the RF port of channel 2
3	RF3	330	4543.37	Channel three RF port
4	GND	330	4093.37	Ground pad next to the RF port of channel three
5	GND	330	3563.37	Ground
6	GND	330	3033.37	Ground
7	GND	330	2503.37	Ground
8	RF4	330	2053.37	Channel four RF port
9	GND	330	1603.37	Ground pad next to channel 4 RF port
10	VDD33_L4	330	1215.87	Channel 4 3.3V power supply
11	GND	330	780.87	Ground
12	ADC_IN<1>	330	345.87	Input, internal ADC analog input signal 2 ports, connected to 3.3V power supply when not in use
13	GND	780	780.87	Ground
14	ADC_IN<0>	780	345.87	Input, analog input signal 1 port of internal ADC, connected to 3.3V power supply when not in use
15	GND	1230	780.87	Ground
16	NC	1230	345.87	
17	VDD12	1680	780.87	The wave control circuit has an internal 1.2V power supply. It is recommended to connect an external 0.1uF voltage stabilizing capacitor to prevent electromagnetic interference.
18	VDD33_DIG	1680	345.87	Wave control circuit 3.3V power supply
19	GND	1955	1088.09	Ground
20	GND	2130	780.87	Ground
21	VDD33_DIG	2130	345.87	Wave control circuit 3.3V power supply
22	GND	2580	780.87	Ground
23	VDD33_DIG	2580	345.87	Wave control circuit 3.3V power supply
24	FIN	3030	780.87	Function register serial input, weak pull-up
25	FEN	3030	345.87	Wave control circuit 3.3V power supply
26	OE	3480	780.87	Input, wave control output enable, weak pull-down, output valid when low
27	DOUT	3480	345.87	Serial data output, weak pull-up
28	GND	3655	1088.09	Ground
29	CLK	3930	780.87	Clock input, weak pull-down, recommended 1~20MHz
30	VDD33_DIG	3930	345.87	Wave control circuit 3.3V power supply

PAD NUMBER	PAD NAME	X -AXIS COORDINATE (UM)	Y- AXIS COORDINATE (UM)	REMARK
31	DIN	4380	780.87	Serial signal input, weak pull-up
32	DEN	4380	345.87	Input, serial data enable, weak pull-up, input valid when low
33	TR1	4830	780.87	Input, wave control input control signal, weak pull-down, generate receiving control signal
34	TR2	4830	345.87	Input, wave control input control signal, weak pull-down, generate pulse emission control signal
35	EN	5280	345.87	Input, wave control enable, weak pull-down, wave control is effective when it is low
36	GND	5280	780.87	Ground
37	VDD33_L1	5280	1215.87	Channel 1 3.3V power supply
38	GND	5280	1603.37	Ground pad next to the RF port of channel 1
39	RF1	5280	2053.37	Channel 1 RF Port
40	GND	5280	2503.37	Ground pad next to the RF port of channel 1
41	GND	5280	3033.37	Ground
42	GND	5280	3563.37	Ground
43	GND	5280	4093.37	Ground pad next to the RF port of channel 2
44	RF2	5280	4543.37	Channel 2 RF port
45	GND	5280	4993.37	Ground pad next to the RF port of channel 2
46	VDD33_L2	5280	5380.87	Channel 2 3.3V power supply
47	GND	3655	5508.65	Ground
48	GND	3255	5508.65	Ground
49	COM	2805	5508.65	Public Port
50	GND	2355	5508.65	Ground
51	GND	1955	5508.65	Ground
52	GND	1035	4628.37	Ground
53	GND	1455	4628.37	Ground
54	GND	2005	4788.37	Ground
55	GND	2405	4463.37	Ground
56	GND	2805	4708.37	Ground
57	GND	3205	4463.37	Ground
58	GND	3605	4788.37	Ground
59	GND	4155	4628.37	Ground
60	GND	4575	4628.37	Ground
61	GND	1035	4128.37	Ground
62	GND	1455	4128.37	Ground
63	GND	2805	4108.37	Ground
64	GND	4155	4128.37	Ground
65	GND	4575	4128.37	Ground
66	GND	900	3708.37	Ground

PAD NUMBER	PAD NAME	X -AXIS COORDINATE (UM)	Y- AXIS COORDINATE (UM)	REMARK
67	GND	1910	3895.87	Ground
68	GND	3700	3895.87	Ground
69	GND	4710	3708.37	Ground
70	GND	2550	3575.87	Ground
71	GND	3060	3575.87	Ground
72	GND	900	2898.37	Ground
73	GND	2550	3125.87	Ground
74	GND	3060	3125.87	Ground
75	GND	4710	2898.37	Ground
76	GND	1035	2468.37	Ground
77	GND	1455	2468.37	Ground
78	GND	1910	2710.87	Ground
79	GND	2805	2788.37	Ground
80	GND	3700	2710.87	Ground
81	GND	4155	2468.37	Ground
82	GND	4575	2468.37	Ground
83	GND	1035	1968.37	Ground
84	GND	1455	1968.37	Ground
85	GND	2005	1808.37	Ground
86	GND	2405	2113.37	Ground
87	GND	2805	2338.37	Ground
88	GND	2805	1888.37	Ground
89	GND	3205	2113.37	Ground
90	GND	3605	1808.37	Ground
91	GND	4155	1968.37	Ground
92	GND	4575	1968.37	Ground

VI. Typical test curve

(unless otherwise specified, the test conditions are 3.3V power supply voltage and room temperature)

Small signal S parameters Receive gain (RFn to COM, other channels loaded) Transmit gain (COM to RFn, other channels loaded)

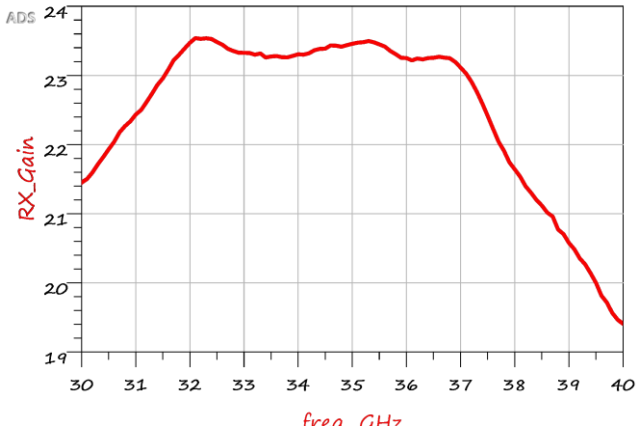


Figure 3. Receive gain (RFn to COM, other channels loaded)

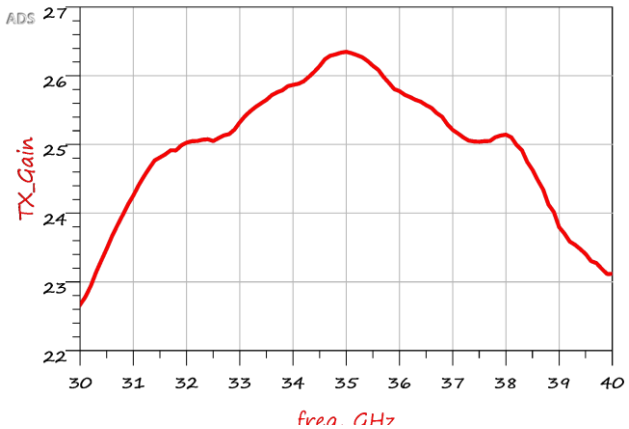


Figure 4. Transmit gain (COM to RFn, other channels loaded)

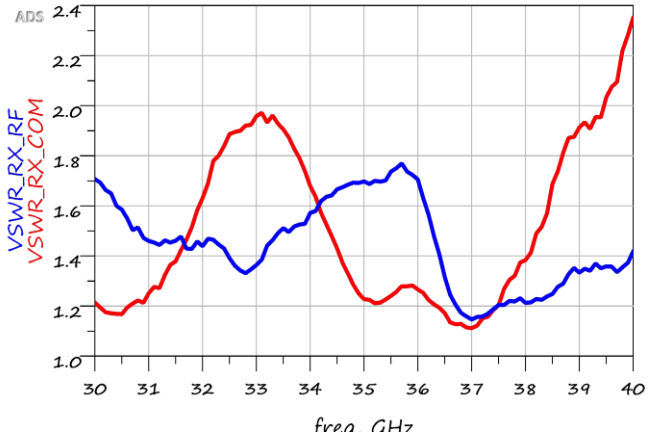


Figure 5. VSWR of receiving port

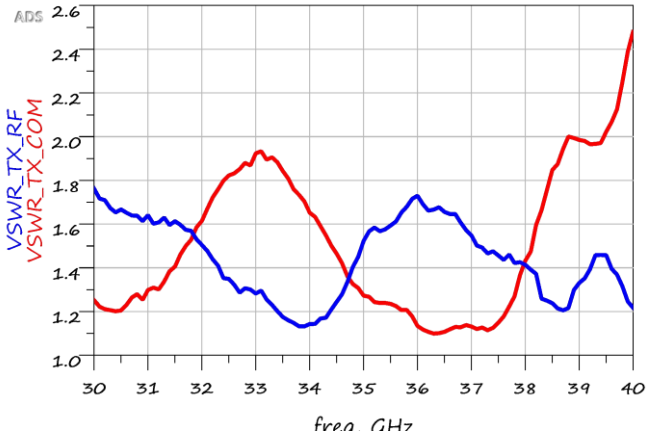


Figure 6. VSWR of transmitting port

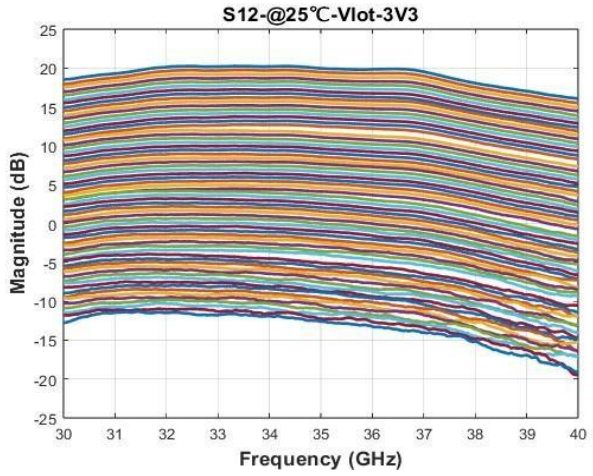


Figure 7. Receive gain 64-state attenuation curve vs frequency

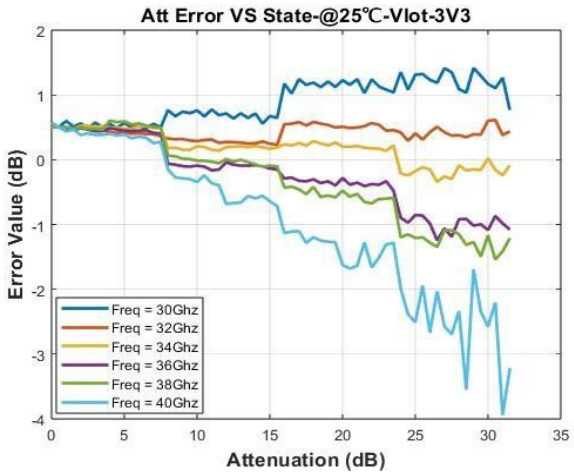


Figure 8. Receive mode attenuation error vs attenuation value

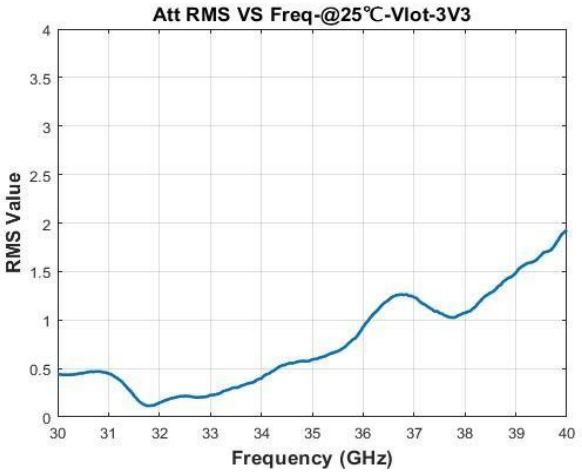


Figure 9. Receive mode RMS attenuation error vs. frequency

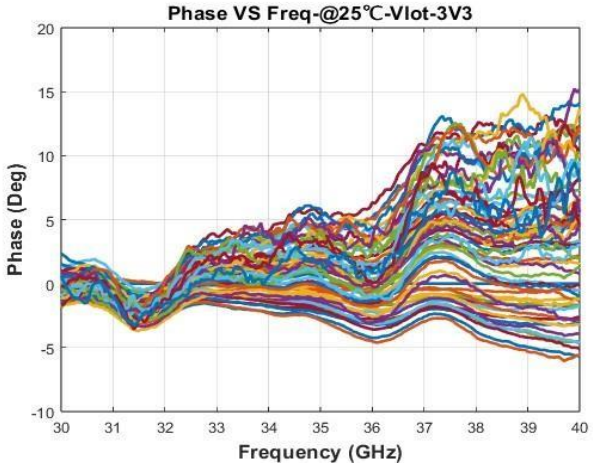


Figure 10. Receive mode Additional phase shift at 64- state attenuation vs. frequency

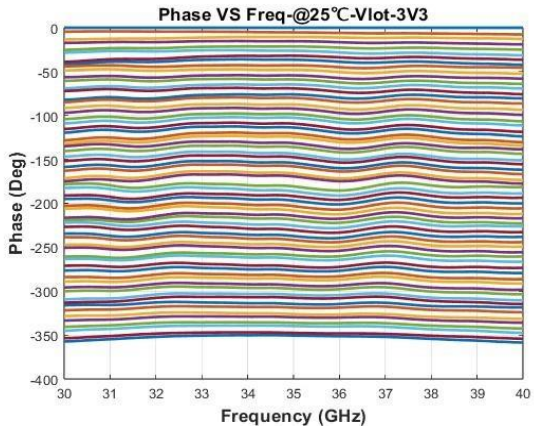


Figure 11. Receive mode 64-state relative phase shift curve vs frequency

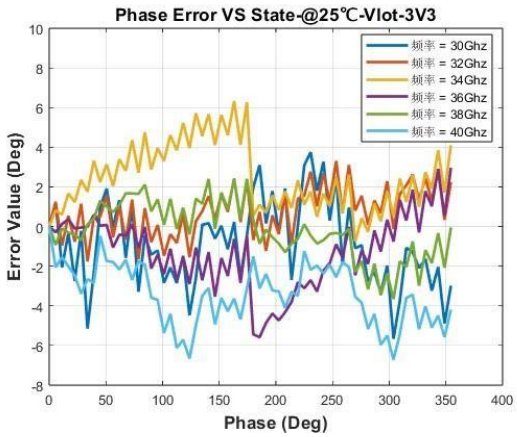


Figure 12. Receiving mode phase shift error vs phase shift value

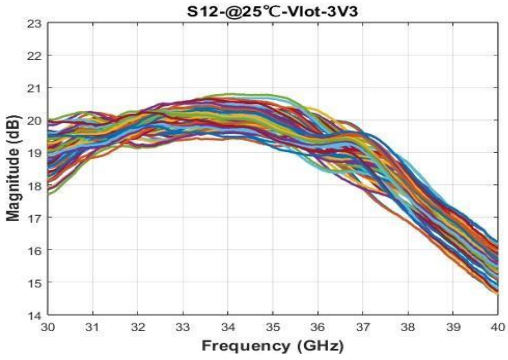


Figure 13. Gain curve vs frequency in receive mode 64-state phase shift

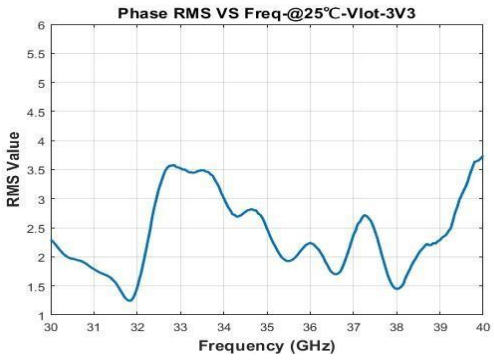


Figure 14. Receive Mode RMS Phase Error vs Frequency

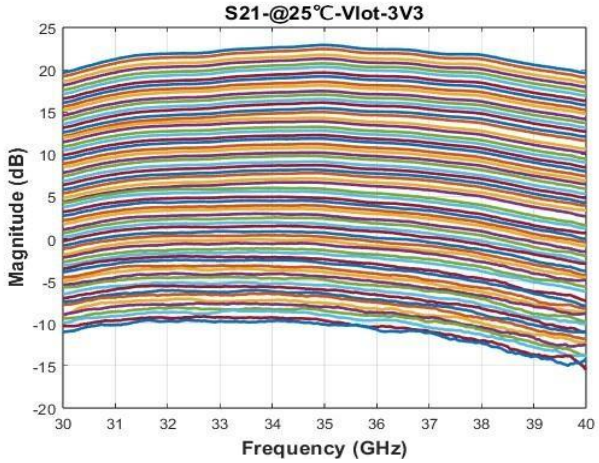


Figure 15. Transmit gain 64-state attenuation curve vs frequency

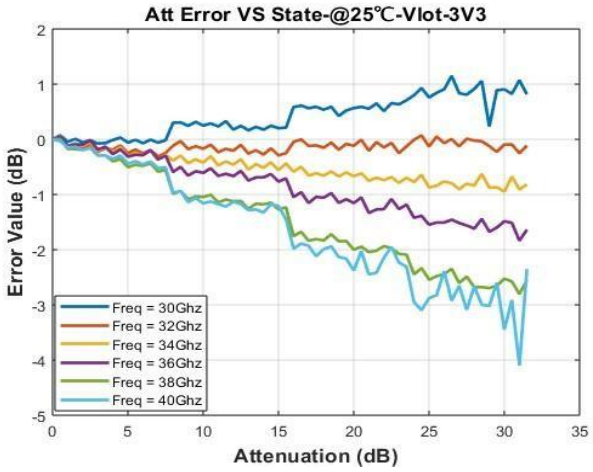


Figure 16. Transmit mode attenuation error vs attenuation value

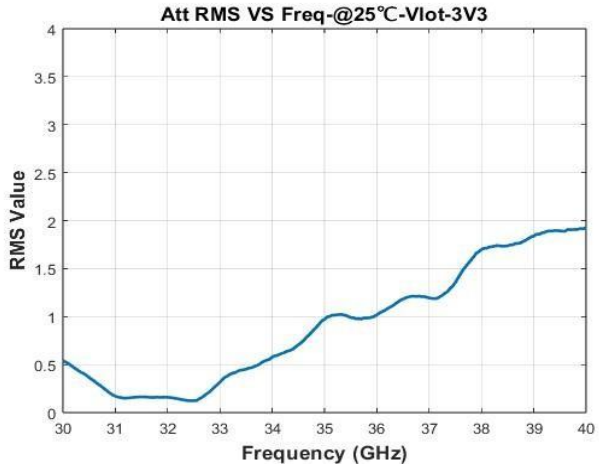


Figure 17. Transmit mode RMS attenuation error vs. frequency

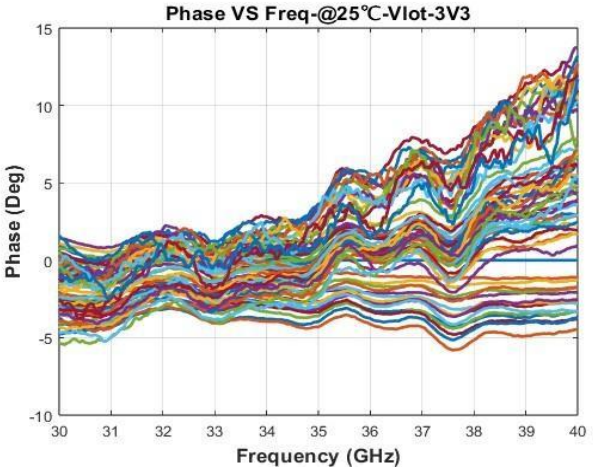


Figure 18. Transmit mode Additional phase shift vs. frequency for 64-state attenuation

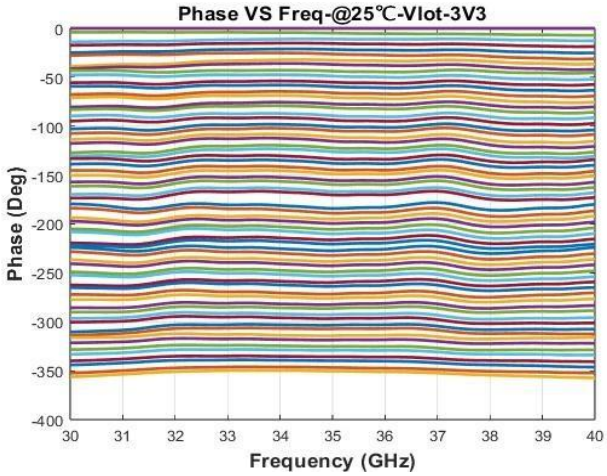


Figure 19. Transmit mode 64-state relative phase shift curve vs frequency

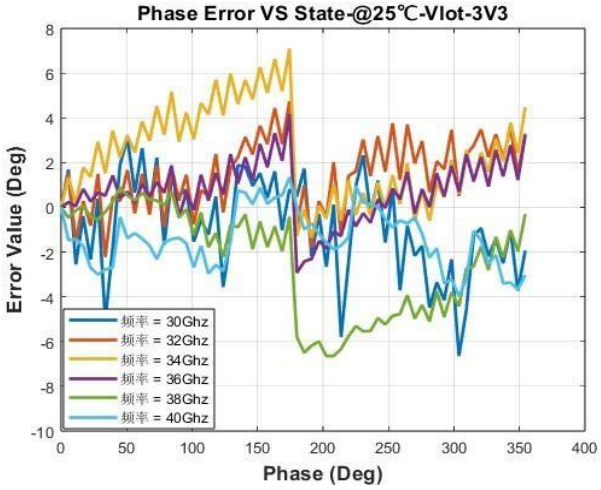


Figure 20. Transmit mode phase shift error vs phase shift value

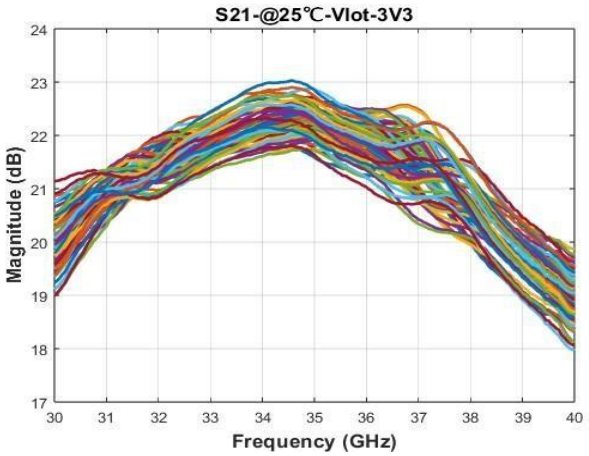


Figure 21. Transmit mode 64-state phase shift gain curve vs frequency

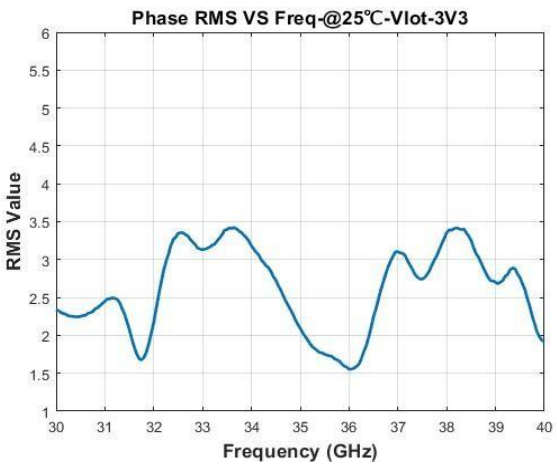


Figure 22. Transmit mode RMS phase shift error vs frequency

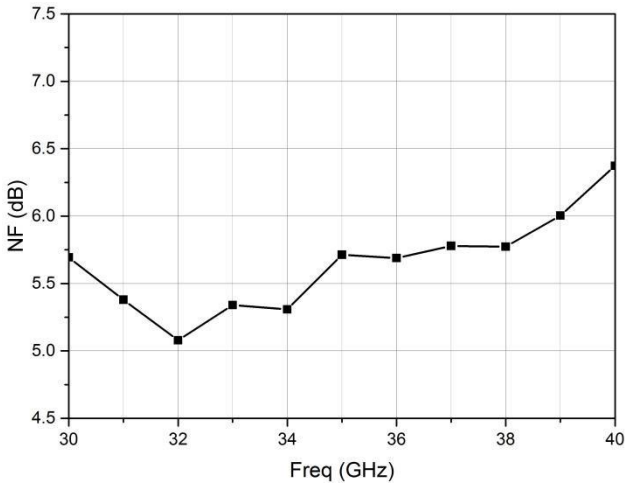


Figure 23. Receive noise coefficient

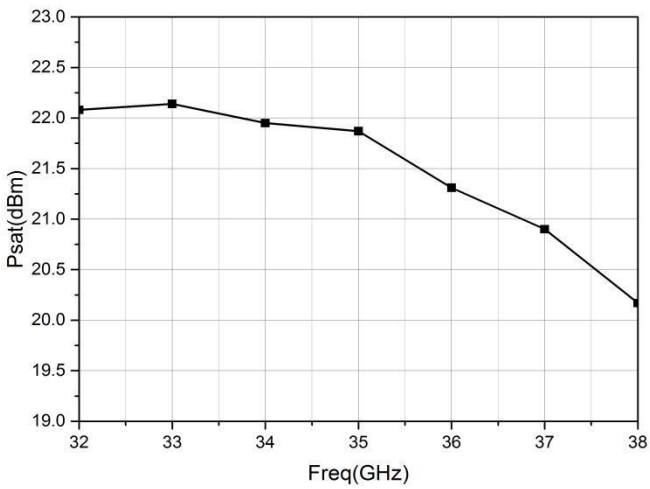


Figure 24. Transmit saturated output power (four-channel full-open pulse state)

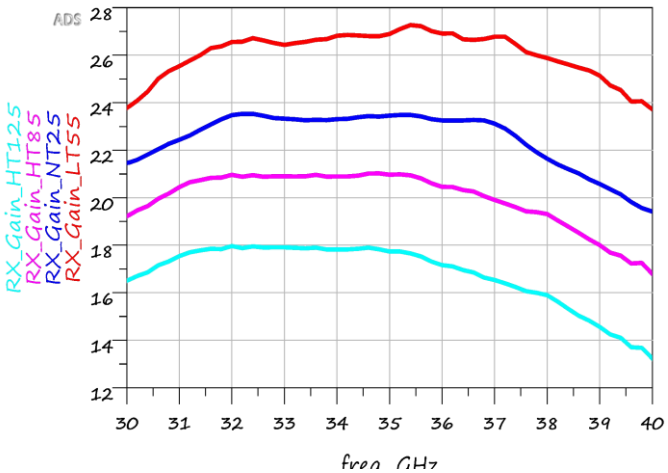


Figure 25. Receiving gain high and low temperature (-55 ℃ ~125 ℃)

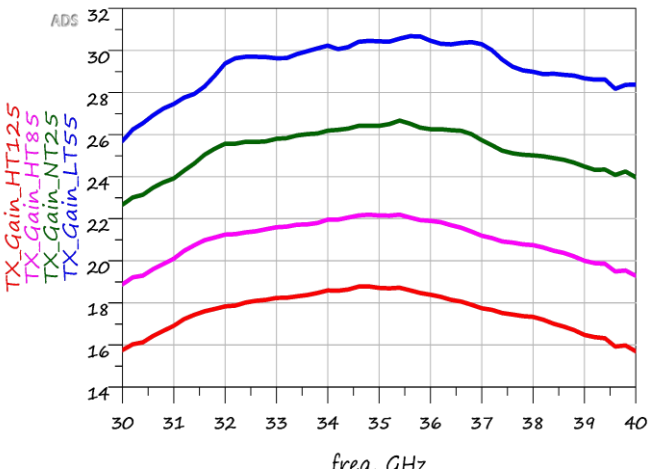


Figure 26. Transmitting gain high and low temperature (-55 ℃ ~ 125 ℃)

VII. Digital wave control function

7.1. Switch control output

The five channels use the same logic control input (the fifth channel is a spare channel), and the transmit and receive status control bits of each channel output the status of the corresponding channel respectively.

The switch control logic is listed in Table 4, where the input signals EN, TR1, and TR2 come from the wave control input port, and MCT and MCR come from the serial data input. After power-on, the default value of MCT=MCR is 1, and the chip is in the load state by default. When switching the transmit and receive states, MCT and MCR need to be configured accordingly. In addition, after power-on, the function register needs to be configured through FIN input 12'h380 to ensure the normal switching of the transmit and receive states.

7.2. Channel 1~5 switch control output logic

Table 5.

ENTER					CORRESPONDING CHANNEL STATUS
EN	TR1	TR2	MCT	MCR	
0	0	0	x	0	Receiving state
0	1	0	x	0	Emission state
0	1	x	0	x	Emission state
		Other combinations			Load state

7.3. Serial Data Register Input Timing

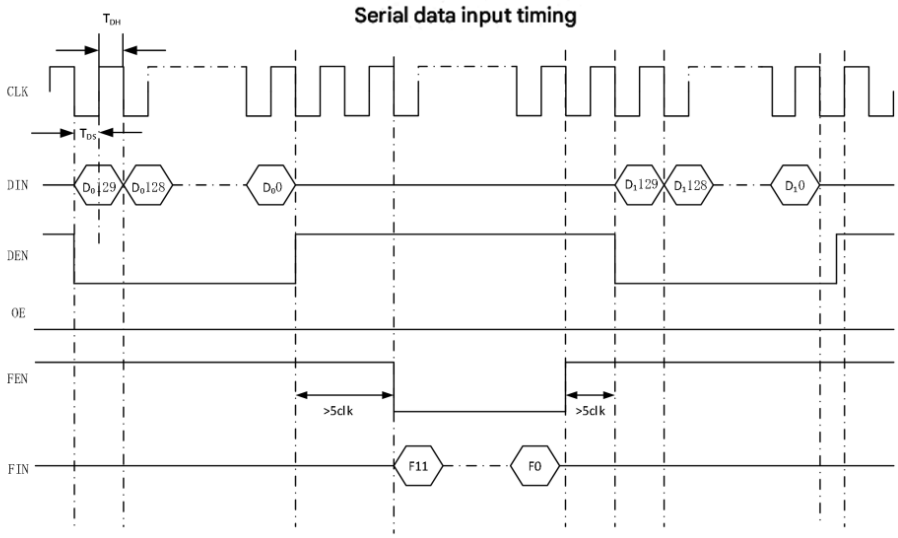


Figure 27.

DEN is low, the rising edge of the clock samples DIN and data is written from the DIN port. After each 130 -bit data is written, FIN needs to be serially input 12'h11f. It should be noted that after the chip is powered on and reset, DIN first serially inputs 130 bits, and the {5{26'h15D5A5A}} instruction code is used to unlock the internal device before 130 bits of user data can be written normally.

130-bit data is shown in Table 5, where AT and AR are the transmit and receive attenuation values, and PT and PR are the transmit and receive phase shift values.

7.4. Input 130-bit data definition

Table 6.

INPUT 130-BIT DATA DEFINITION					
First Channel					
D[25:20]	D19	D18	D[17:12]	D[11:6]	D[5:0]
AT1[5:0]	MCT1	MCR1	AR1[5:0]	PT1[5:0]	PR1[5:0]
Second channel					
D[51:46]	D45	D44	D[43:38]	D[37:32]	D[31:26]
AT2[5:0]	MCT2	MCR2	AR2[5:0]	PT2[5:0]	PR2[5:0]
Third Channel					
D[77:72]	D71	D70	D[69:64]	D[63:58]	D[57:52]
AT3[5:0]	MCT3	MCR3	AR3[5:0]	PT3[5:0]	PR3[5:0]
Fourth channel					
D[103:98]	D97	D96	D[95:90]	D[89:84]	D[83:78]
AT4[5:0]	MCT4	MCR4	AR4[5:0]	PT4[5:0]	PR4[5:0]

Fifth Channel					
D[129:124]	D123	D122	D[121:116]	D[115:110]	D[109:104]
AT5[5:0]	MCT5	MCR5	AR5[5:0]	PT5[5:0]	PR5[5:0]

7.5. Serial Data Register Output Timing

7.5.1. Serial Data Output Timing

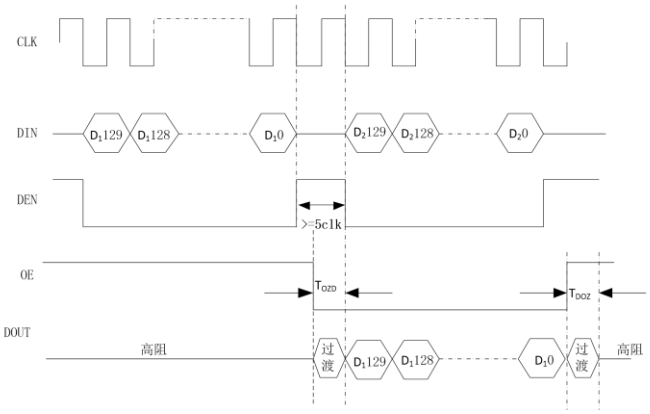


Figure 28.

7.5.2. Function Register Input Timing

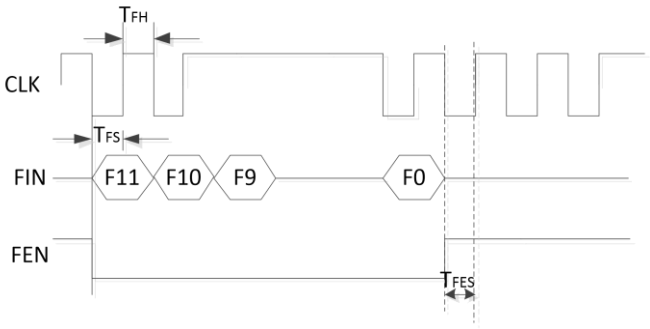


Figure 29.

FEN is low, the rising edge of the clock samples FIN and data is input from the FIN port.

7.6. ADC Function Description and Timing

7.6.1. ADC data reading timing

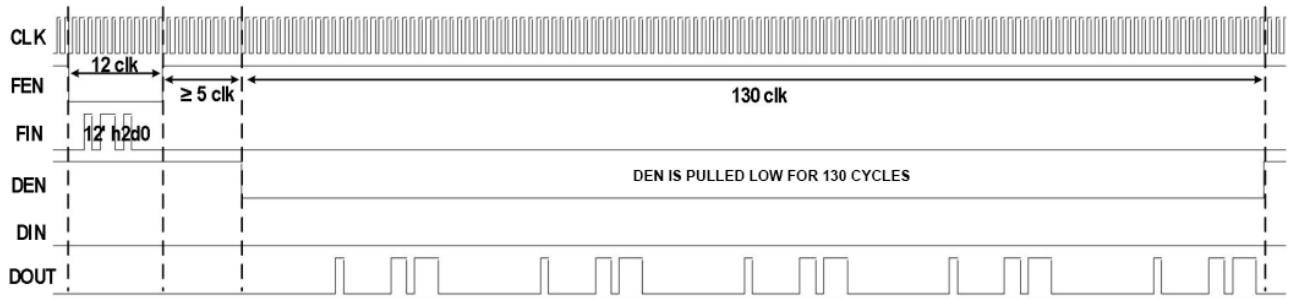


Figure 30.

The chip integrates ADC function. ADC_IN<0> and ADC_IN<1> are two pins that input analog signals. By reading DOUT data, the ADC_IN<0>, ADC_IN<1> inputs correspond to two 8- bit digital signals.

First, FEN is pulled low for 12 CLK cycles, during which FIN serially inputs the 12'h2d0 signal. After at least 5 CLK cycles, DEN is pulled low for 130 CLK cycles. At this time, DOUT serially outputs 130 bits of data in the format of {5{5'd0,ad_data1, 5'd0,ad_data0}}, where the lower 8 bits are D7: D0 is the ADC value corresponding to ADC_IN<0>, while D20: D13 is the ADC value corresponding to ADC_IN<1>.

The input-output correspondence of the actual test of the ADC circuit is listed in the following table.

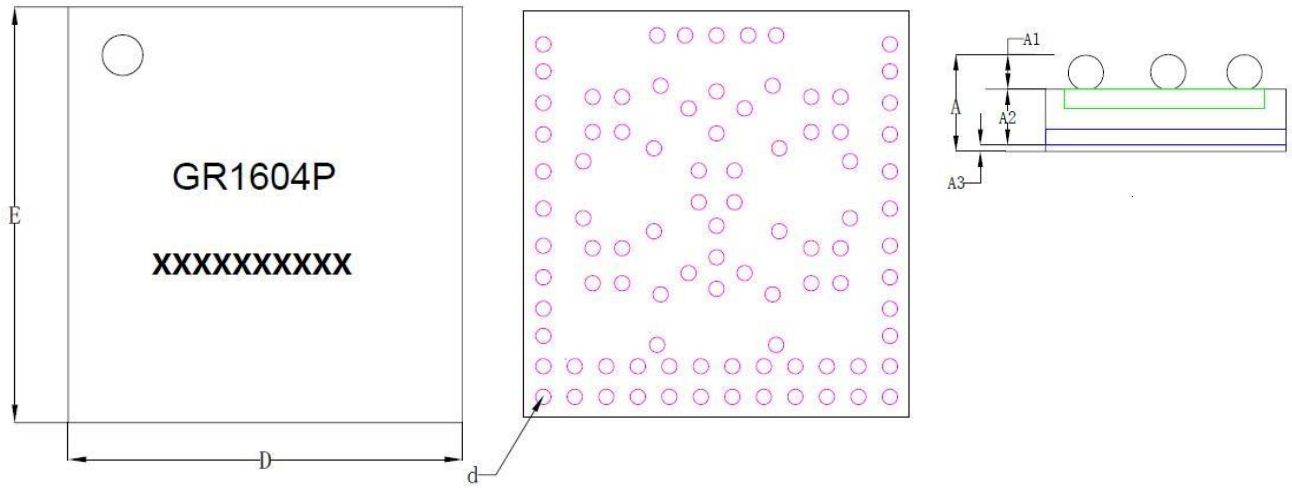
7.6.2. Input analog voltage value and ADC output

Table 7.

ADC ANALOG INPUT VOLTAGE (V)	8 -BIT DIGITAL OUTPUT (HEXADECIMAL)	THEORETICAL ANALOG VALUE CORRESPONDING TO DIGITAL OUTPUT
0.01	2	0.03
0.1	7	0.09
0.2	0f	0.19
0.3	16	0.28
0.4	1e	0.39
0.5	29	0.53
0.6	2e	0.59
0.7	36	0.70
0.8	3e	0.80
0.9	44	0.88
1	4b	0.97
1.1	52	1.06
1.2	58	1.13
1.3	62	1.26
1.4	6b	1.38
1.5	71	1.46
1.6	7b	1.59
1.7	82	1.68
1.8	88	1.75
1.9	8f	1.84
2	99	1.97
2.1	a1	2.08
2.2	a7	2.15
2.3	ae	2.24
2.4	b6	2.35
2.5	be	2.45
2.6	c5	2.54
2.7	cd	2.64
2.8	d4	2.73
2.9	db	2.82
3	e4	2.94
3.1	eb	3.03
3.2	f3	3.13
3.3	fa	3.22

VIII. Packaging Solutions

The chip adopts WLCSP wafer-level packaging with a size of 5.555mm×5.855mm. The detailed size information of the packaging is shown in the figure and table below.



Top view Bottom view Side view

Figure 31. BSTCC59-3238 package diagram

8.1. Package Dimensions

Table 8.

SIZE DESIGNATION	NOMINAL VALUE	TOLERANCE
A	0.800	±0.038
A1	0.166	±0.020
A2	0.594	±0.013
A3	0.040	±0.005
D	5.555	±0.025
E	5.855	±0.025
d	0.239	±0.020

IX. Typical Application and Assembly Schematics

The RF port and common port of each channel need to be led out by a 50- ohm transmission line, and no external DC isolation is required. Pay attention to the connection between different channels on the application board and between RF and

COMs requires good on-board isolation.

All GND pins need to have good contact with the ground plane underneath.

The power supply voltage of this chip is 3.3V. When used, place a 0.1uF chip capacitor to ground near the power pad of the chip. In addition, this four-channel chip needs

At least 100uF tantalum capacitor filtering is required to reduce the fluctuation of chip power supply voltage during pulse switching. When the chip is working, it is necessary to power on the power port VDD33 first, and then give the control signal to the wave control I/O port.

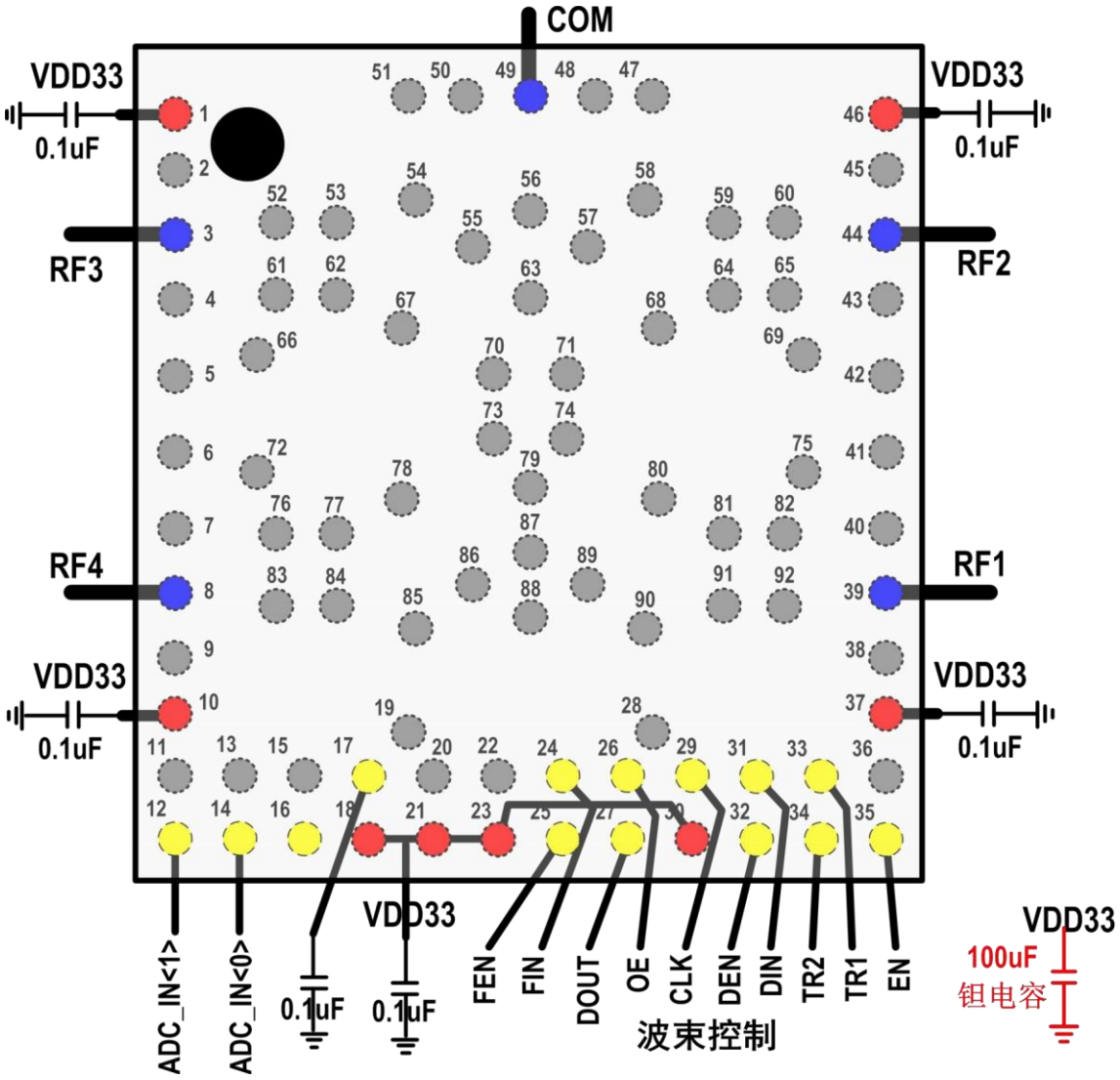


Figure 32. Typical Application and Assembly Schematics