BSTCC58-1418

Ku-band four-channel multi-function chip

Data Sheet

I. Product Introduction

BSTCC58-1418 is a Ku-band four-channel multi-function chip.

3.3V power supply, the operating frequency range is 14GHz ~ 18GHz. The chip integrates low noise amplifier, driver amplifier, switch, 6 -digital controlled attenuator, 6 -digital controlled phase shifter, power divider, beam control and other modules. The transceiver link of each channel can provide a maximum attenuation range of 31.5dB, stepping 0.5dB, and a 360° phase shift range, stepping 5.625°. The chip adopts plastic QFN package, with a total of 68 pins and a chip size of 8mm×8mm.

II. Application Areas

- Radar
- Communication
- Instrumentation

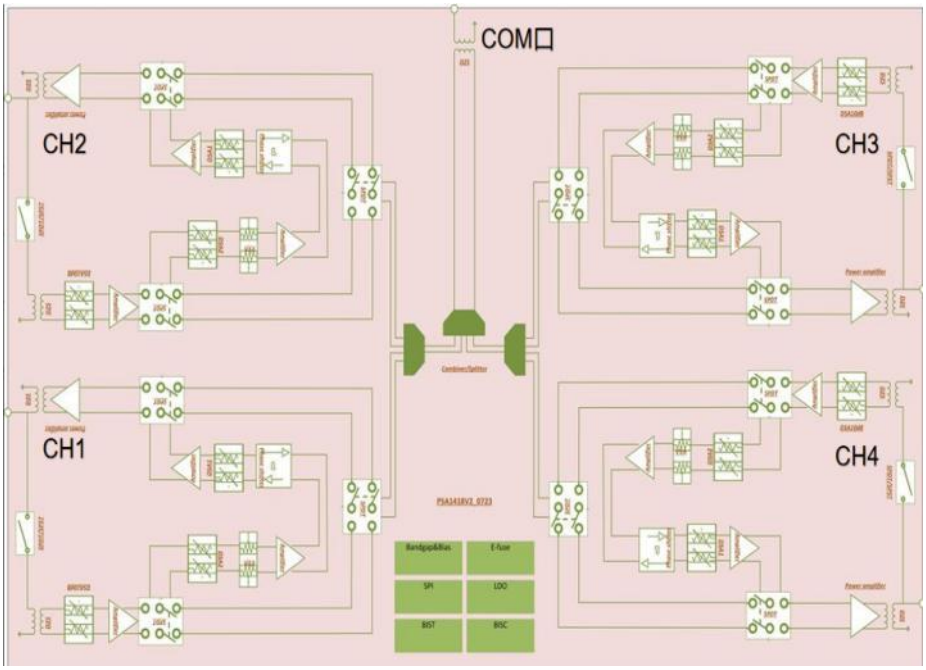

Figure 1. BSTCC58-1418 chip module schematic

III. Key technical indicators

- Working power supply voltage: 3.3V
- Operating frequency range: 14GHz ~ 18GHz
- 6 -bit attenuation control, step 0.5dB
- 6 phase shift control bits, stepping 5.625°
- Receive gain: 4dB@16GHz
- (RF port to COM port)
- Transmitter linear gain: 14dB@16GHz
- (COM port to RF port)
- Gain flatness in receiving band: 1dB
- Gain flatness in the emission band: 3dB
- Port standing wave ratio VSWR: 2
- Receive noise factor NF: 13dB (no attenuation)
- Receive input P-1dB: 1dBm
- Transmitter output P-1dB: 14dBm
- RMS phase shift error: < 3°
- Amplitude consistency during phase shift: < ±1dB
- Attenuation accuracy: < 0.3dB+4%Ai
- RMS attenuation error: < 0.5dB
- Attenuation additional phase shift: < ±8°
- Transmit and receive switching time: < 100ns
- Single channel operating current: 65mA/85mA/135mA/1mA
  @ Receive / Static Transmit /1dB Transmit / Load
- Package and size: QFN 8mm×8mm
- Process: SiGe BiCMOS

IV. Electrical Characteristics

4.1. Basic electrical properties

Table 1.

PARAMETER	CONDITION	MINIMUM	TYPICAL VALUE	MAXIMUM	UNIT
Frequency range		14	—	18	GHz
Receive linear gain	RF port to COM port		4		dB
Transmit linear gain	COM port to RF port		14		dB
In-band gain flatness				3	dB
Receive noise figure	No attenuation			13	dB
Receive input P-1dB			1		dBm
Transmit output P-1dB			14		dBm
RMS Phase Shift Error				3	Deg
Phase shift amplitude consistency		-1		1	dB
RMS attenuation error				0.5	dB
Attenuation of additional phase shift		-8		8	Deg
Transmit/receive switching time				100	ns
Single channel receiving current			65		mA
Single channel static emission current			85		mA
Single channel 1dB transmission current			135		mA
Single channel load current			1		mA

4.2. Digital port electrical parameters

Table 2.

PARAMETER	SYMBOL	CONDITION	MINIMUM	MAXIMUM	UNIT
Input high level voltage	VIH	VCC = 2.7 V to 3.6 V	1.7	—	V
Input low level voltage	VIL	VCC = 2.7 V to 3.6 V	—	0.8	V
Input high level current	IIH	VCC = 2.7 V to 3.6 V	-500	500	uA
Input low level current	IIL	VCC = 2.7 V to 3.6 V	-500	500	uA
Output high level voltage	VOH	VCC = 2.7 V to 3.6 V IOH = –100 uA	VCC-0.2	VCC	V
Output high level voltage	VOH	VCC = 2.7 V IOH = –8mA	2.4	VCC	V
Output low level voltage	VOL	VCC = 2.7 V to 3.6 V IOL= 100uA	0	0.2	V
Output low level voltage	VOL	VCC = 2.7 V, IOL = 8mA	0	0.4	V

4.3. Limit parameters

Table 3.

PARAMETER	VALUE
Maximum supply voltage	3.6V
Maximum RF input power	15dBm
Storage temperature	-65 ～ 150 ℃
Operating temperature	-55 ～ 125 ℃

Note: For the above listed maximum limits, if the device is operated in an environment exceeding these limits, it is likely to cause permanent damage to the device.

In actual application, it is best not to operate the device in an environment where the limit value or the value exceeds this limit value.

4.4. ESD Protection

The anti-static level (HBM) of BSTCC58-1418 is at least Class 2: ≥2000V. When handling, take appropriate ESD protection measures to avoid performance degradation or functional failure.

V. Pin Configuration

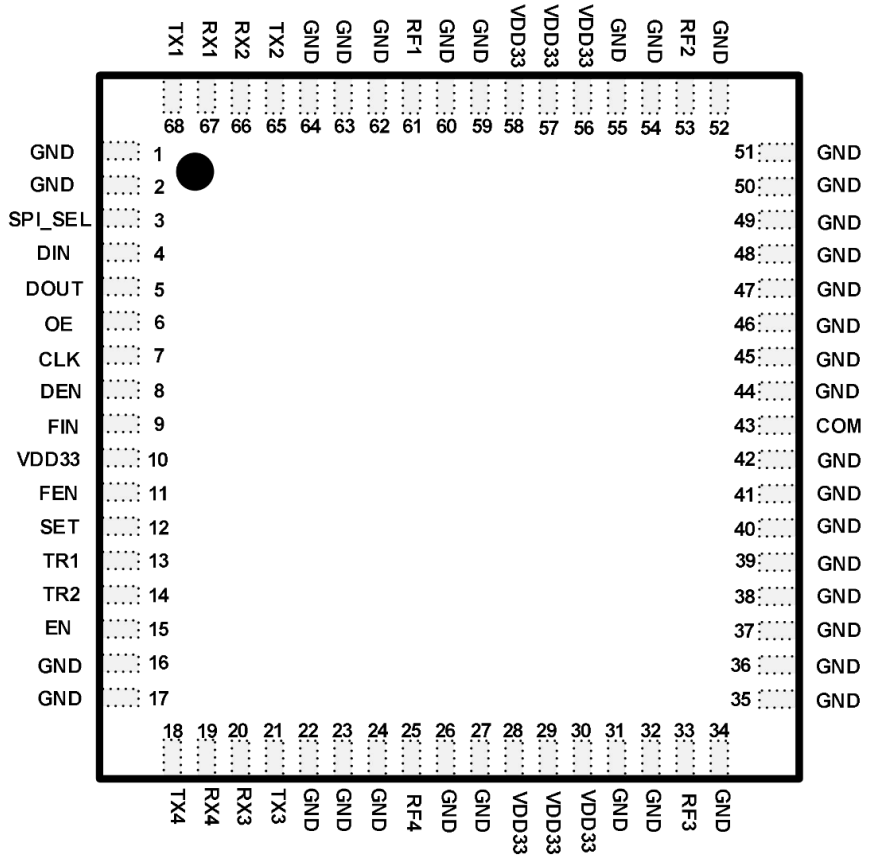

Figure 2. Chip pin layout

5.1. Chip pad function information table

Table 4.

PIN NUMBER	PIN NAME	PORT ATTRIBUTES	PIN FUNCTION	PIN NUMBER	PIN NAME	PORT ATTRIBUTES	PIN FUNCTION
1	GND	Ground	Ground	35	GND	Ground	Ground
2	GND	Ground	Ground	36	GND	Ground	Ground
3	SPI_SEL	Digital Input	Debug mode selection signal, weak pull-down, floating by default	37	GND	Ground	Ground
4	DIN	Digital Input	Serial data input, weak pull-down	38	GND	Ground	Ground
5	DOUT	Digital Output	Serial data output, weak pull-up	39	GND	Ground	Ground
6	OE	Digital Input	Output enable, weak pull-down	40	GND	Ground	Ground
7	CLK	Clock Input	Digital clock signal, weak pull-down	41	GND	Ground	Ground
8	DEN	Digital Input	Secondary latch signal, weak pull-up	42	GND	Ground	Ground
9	FIN	Digital Input	Function register input, weak pull-down	43	COM	Radio Frequency	Public Port
10	VDD33	power supply	Digital circuit 3.3V power supply	44	GND	Ground	Ground
11	FEN	Digital Input	Function register enable, weak pull-up	45	GND	Ground	Ground
12	SET	Digital Input	Digital reset signal, weak pull-down	46	GND	Ground	Ground
13	TR1	Digital Input	Receive switch control, weak pull-down	47	GND	Ground	Ground
14	TR2	Digital Input	Transmit switch control, weak pull-down	48	GND	Ground	Ground
15	EN	Digital Input	Wave control enable control, weak pull-down	49	GND	Ground	Ground
16	GND	Ground	Ground	50	GND	Ground	Ground
17	GND	Ground	Ground	51	GND	Ground	Ground
18	TX4	Output	0V after power on	52	GND	Ground	Ground
19	RX4	Output	3.3V after power on	53	RF2	Radio Frequency	Channel 2 RF port
20	RX3	Output	3.3V after power on	54	GND	Ground	Ground
21	TX3	Output	0V after power on	55	GND	Ground	Ground
22	GND	Ground	Ground	56	VDD33	power supply	3.3V power supply for channel 1 and channel 2
23	GND	Ground	Ground	57	VDD33	power supply	3.3V power supply for channel 1 and channel 2

PIN NUMBER	PIN NAME	PORT ATTRIBUTES	PIN FUNCTION	PIN NUMBER	PIN NAME	PORT ATTRIBUTES	PIN FUNCTION
24	GND	Ground	Ground	58	VDD33	power supply	3.3V power supply for channel 1 and channel 2
25	RF4	Radio Frequency	Channel four RF port	59	GND	Ground	Ground
26	GND	Ground	Ground	60	GND	Ground	Ground
27	GND	Ground	Ground	61	RF1	Radio Frequency	Channel 1 RF Port
28	VDD33	power supply	Channel 3 and Channel 4 3.3V power supply	62	GND	Ground	Ground
29	VDD33	power supply	Channel 3 and Channel 4 3.3V power supply	63	GND	Ground	Ground
30	VDD33	power supply	Channel 3 and Channel 4 3.3V power supply	64	GND	Ground	Ground
31	GND	Ground	Ground	65	TX2	Output	0V after power on
32	GND	Ground	Ground	66	RX2	Output	3.3V after power on
33	RF3	Radio Frequency	Channel three RF port	67	RX1	Output	3.3V after power on
34	GND	Ground	Ground	68	TX1	Output	0V after power on

VI. Typical test curve

(unless otherwise specified, the test conditions are 3.3V power supply voltage, normal temperature environment) Transceiver gain and port standing wave

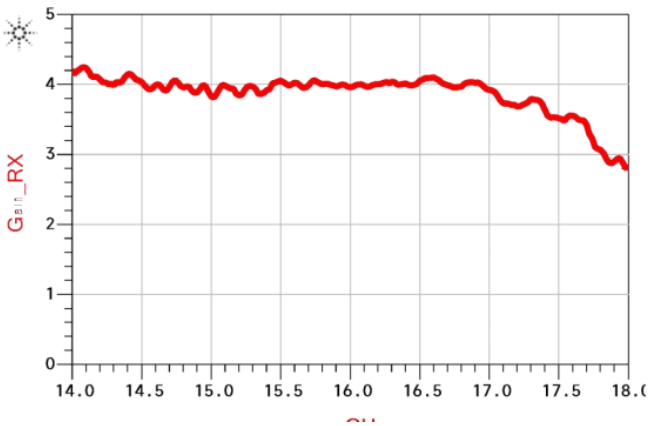

Figure 3. Receive Gain (RF_CHn to RF_COM)

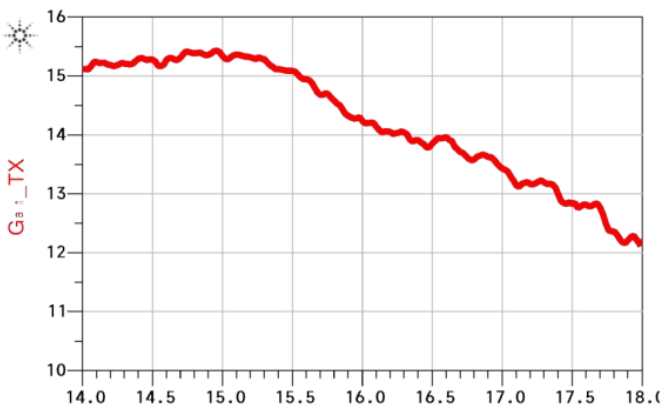

Figure 4. Transmit Gain (RF_COM to RF_CHn)

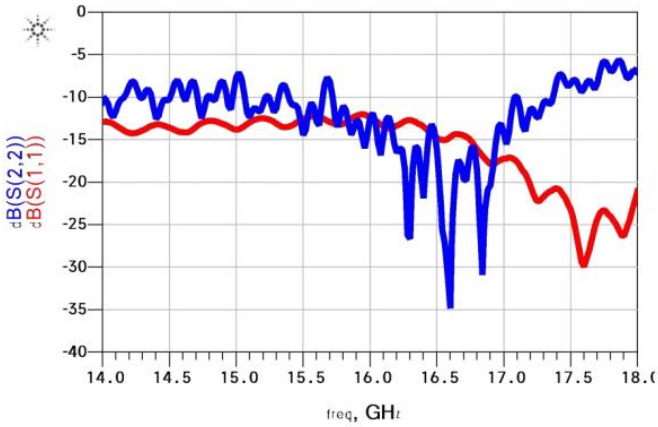

Figure 5. Receive port return loss

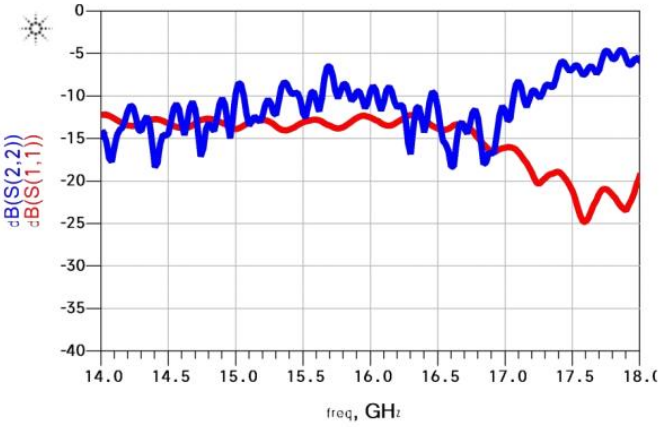

Figure 6. Transmit port return loss

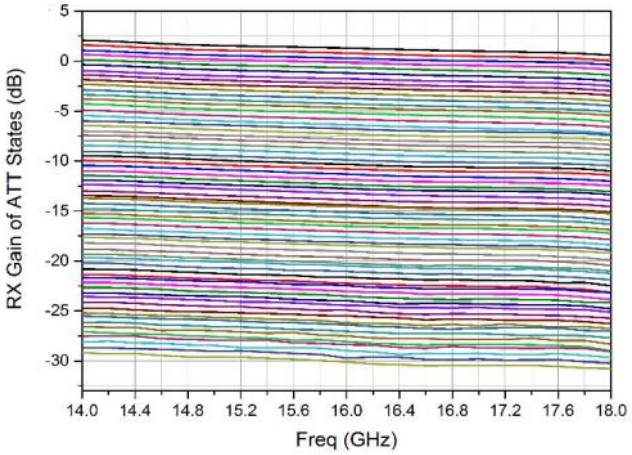

Figure 7. Receive Gain 64-State Attenuation Curve vs Frequency

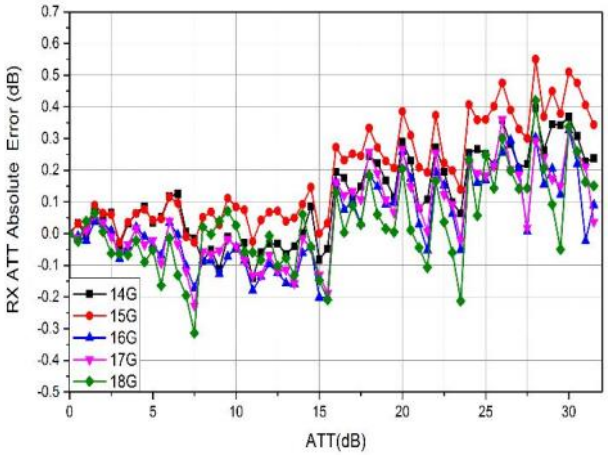

Figure 8. Receive mode attenuation error vs attenuation value

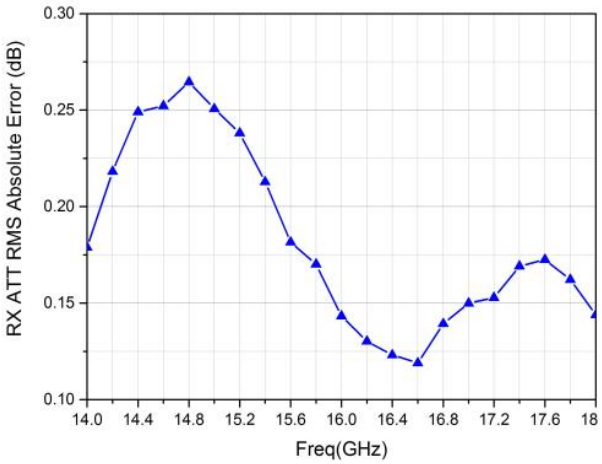

Figure 9. Receive Mode RMS Attenuation Error vs Frequency

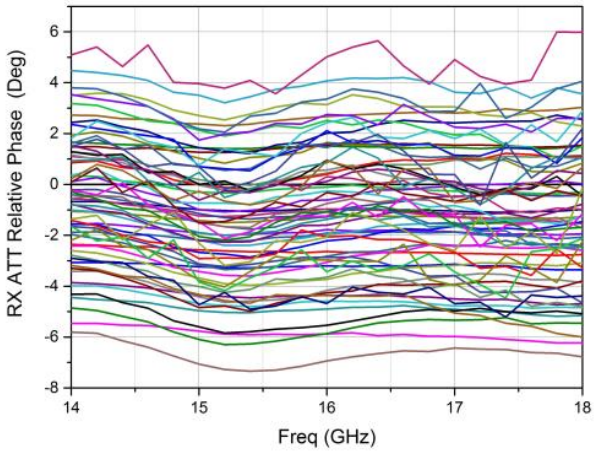

Figure 10. Receive Mode 64 Additional Phase Shift vs Frequency During State Attenuation

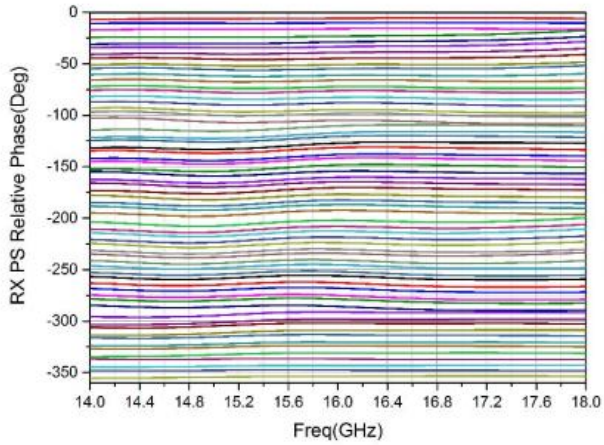

Figure 11. Relative phase shift curve of receiving mode 64 vs frequency

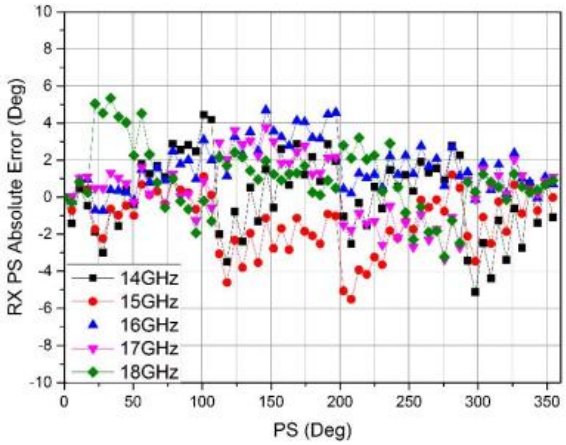

Figure 12. Receive mode phase shift error vs phase shift value

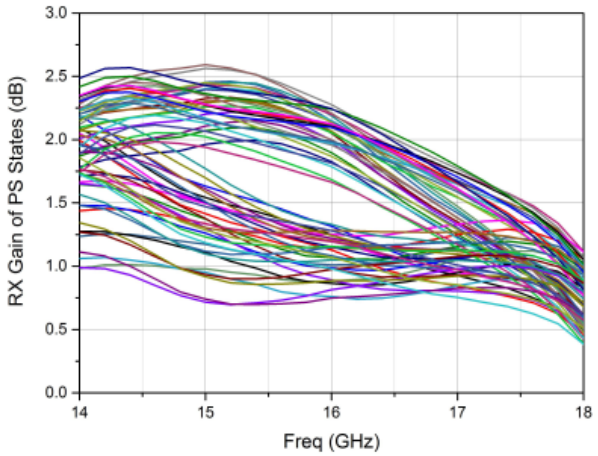

Figure 13. Transmitter Gain 64-State Attenuation Curve vs Frequency

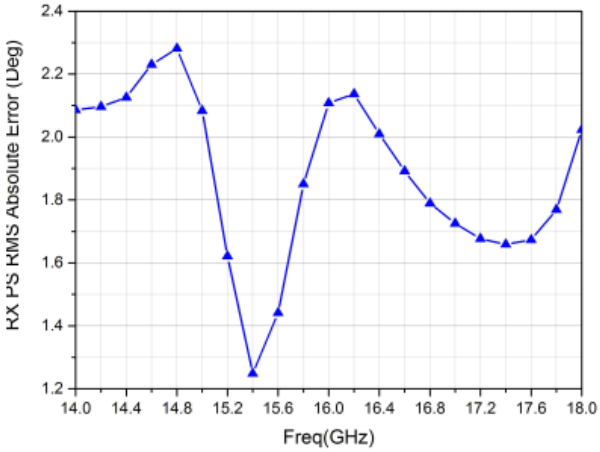

Figure 14. Receive Mode RMS Phase Error vs Frequency

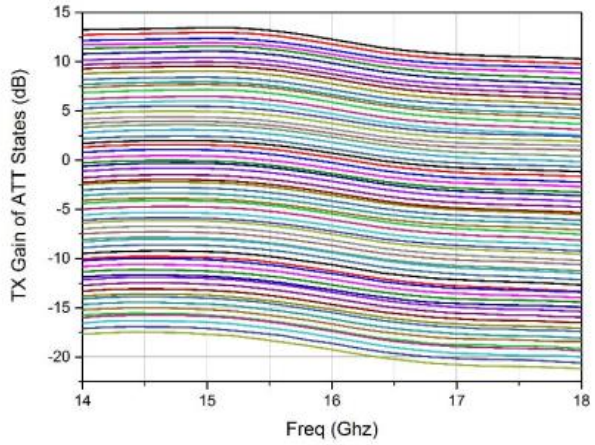

Figure 15. Transmitter Gain 64-State Attenuation Curve vs Frequency

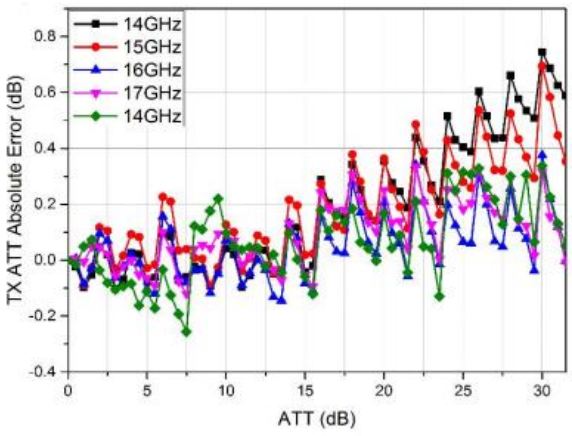

Figure 16. Transmit mode attenuation error vs attenuation value

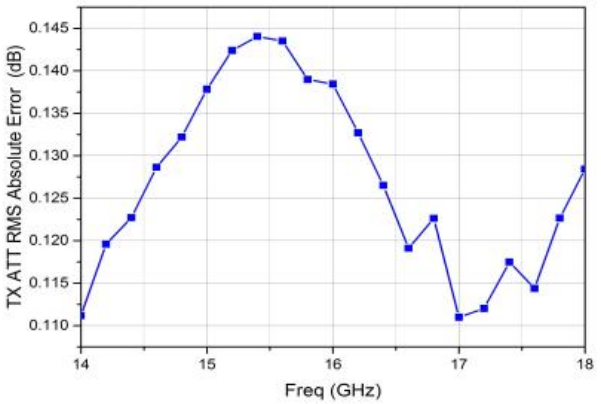

Figure 17. Transmit Mode RMS Attenuation Error vs Frequency

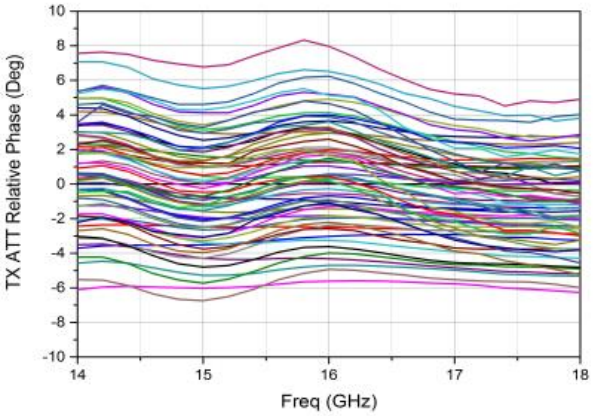

Figure 18. Additional phase shift vs frequency when transmitting mode 64 decays

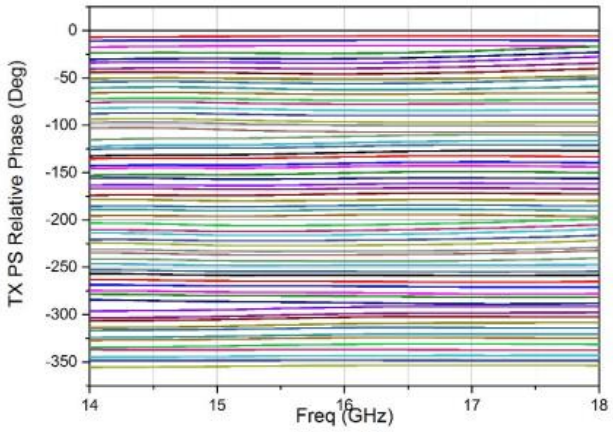

Figure 19. Transmit mode 64 state relative phase shift curve vs frequency

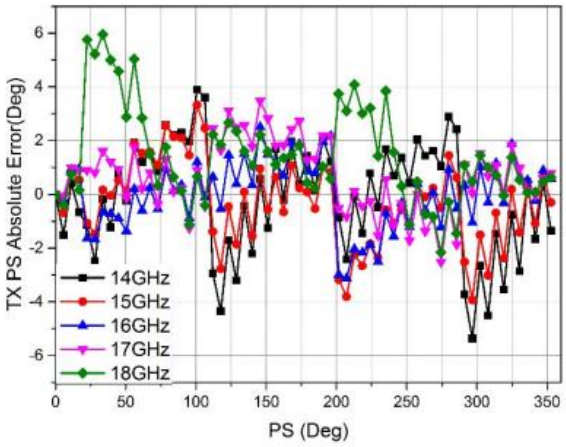

Figure 20. Transmit mode phase shift error vs phase shift value

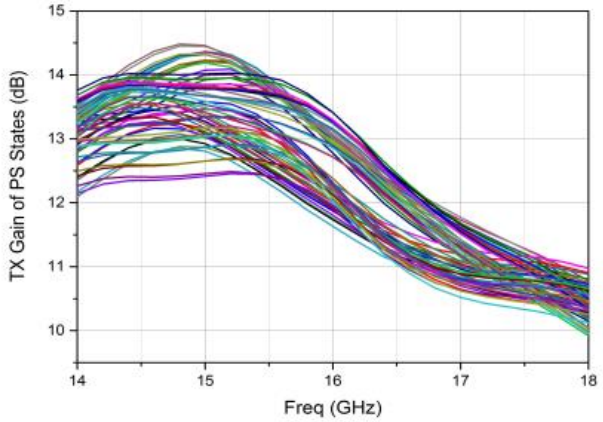

Figure 21. Transmit Mode 64 Phase Shift Gain Curve vs Frequency

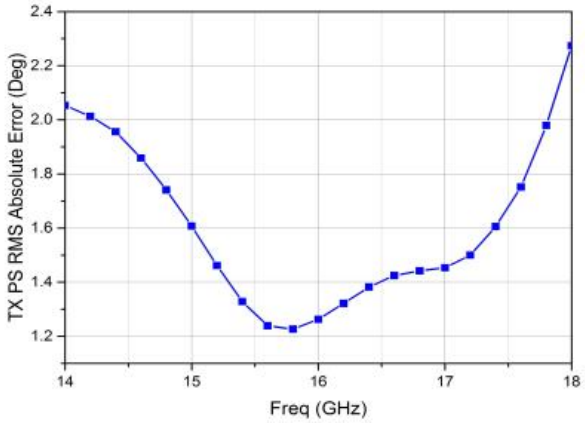

Figure 22. Transmit Mode RMS Phase Error vs Frequency

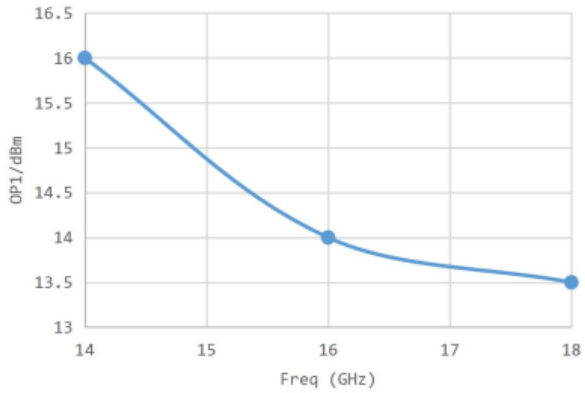

Figure 23 Transmit output 1dB power vs frequency

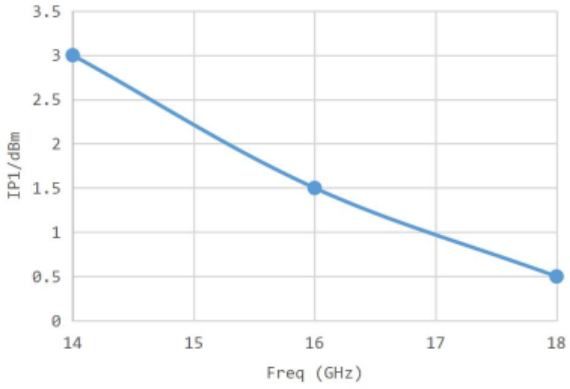

Figure 24. Receive input 1dB power vs frequency

VII. Digital wave control function

The overall block diagram of the multifunctional chip digital wave control circuit

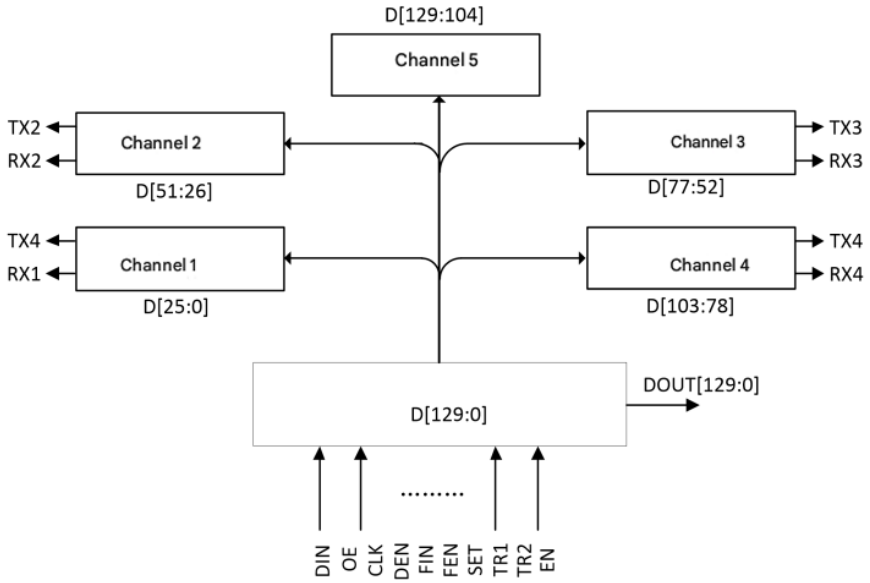

Figure 25. Digital control system block diagram

Channels 1 to 4 control four RF channel links, and the fifth channel data D[129:D104] is a spare digital code.

7.1. Status control output description

The transmit and receive state control is listed in Table 4. The five channels use the same logic control. The control input of each channel is composed of the TR1 and TR2 wave control signals of the chip as a whole and the MCT and MCR data input of each channel. The positions of MCT and MCR are listed in Table 5. RX and TX are the wave control signals of each channel. Control output, which can be used to control the status of external LNA and PA of each channel.

7.2. Description of each channel's receiving and sending status control

Table 5.

ENTER					CHANNEL STATUS AND OUTPUT					
EN	TR1	TR2	MCT	MCR	COM-RX	COM-TX	COM-Load	state	RX	TX
0	0	0	0	0	Conductivity	Shutdown	Shutdown	Receiving state	0	0
0/1	0	0	0	1	Shutdown	Shutdown	Conductivity	Load state	3.3V	0
0	0	0	1	0	Conductivity	Shutdown	Shutdown	Receiving state	0	0
0/1	0	0	1	1	Shutdown	Shutdown	Conductivity	Load state	3.3V	0
0/1	0	1	0	0	Shutdown	Shutdown	Conductivity	Load state	3.3V	0
0/1	0	1	0	1	Shutdown	Shutdown	Conductivity	Load state	3.3V	0
0/1	0	1	1	0	Shutdown	Shutdown	Conductivity	Load state	3.3V	0
0/1	0	1	1	1	Shutdown	Shutdown	Conductivity	Load state	3.3V	0
0	1	0	0	0	—	—	—	Transition state	3.3V	0
0/1	1	0	0	1	Shutdown	Shutdown	Conductivity	Load state	3.3V	0
0	1	0	1	0	—	—	—	Transition state	3.3V	0
0/1	1	0	1	1	Shutdown	Shutdown	Conductivity	Load state	3.3V	0
0	1	1	0	0	Shutdown	Conductivity	Shutdown	Emission state	3.3V	3.3V
0	1	1	0	1	Shutdown	Conductivity	Shutdown	Emission state	3.3V	3.3V
0/1	1	1	1	0	Shutdown	Shutdown	Conductivity	Load state	3.3V	0
0/1	1	1	1	1	Shutdown	Shutdown	Conductivity	Load state	3.3V	0

Table 6.

WAVE CONTROL 130-BIT DATA DEFINITION					
First Channel					
D[25:20]	D19	D18	D[17:12]	D[11:6]	D[5:0]
AT1[5:0]	MCR1	MCT1	AR1[5:0]	PT1[5:0]	PR1[5:0]
Second channel					
D[51:46]	D45	D44	D[43:38]	D[37:32]	D[31:26]
AT2[5:0]	MCR2	MCT2	AR2[5:0]	PT2[5:0]	PR2[5:0]
Third Channel					
D[77:72]	D71	D70	D[69:64]	D[63:58]	D[57:52]
AT3[5:0]	MCR3	MCT3	AR3[5:0]	PT3[5:0]	PR3[5:0]
Fourth channel					
D[103:98]	D97	D96	D[95:90]	D[89:84]	D[83:78]
AT4[5:0]	MCR4	MCT4	AR4[5:0]	PT4[5:0]	PR4[5:0]

WAVE CONTROL 130-BIT DATA DEFINITION					
Channel 5 (spare)					
D[129:124]	D123	D122	D[121:116]	D[115:110]	D[109:104]
AT5[5:0]	MCT5	MCR5	AR5[5:0]	PT5[5:0]	PR5[5:0]

Note: The chip automatically resets when powered on

After power-on, the default value of MCT=MCR is 1, and the chip is in load state by default; in load state, the chip is not powered off; when each channel switches state, the MCR and MCT inputs of the channel need to be configured accordingly;

TX wave control output is used, in order to ensure the normal operation of the entire transmission link, first input 12'h3e0 through FIN to configure the function register.

27 for the sequence.

7.3. Wave control timing diagram

Data input timing, the clock cycle can be 1~40MHz.

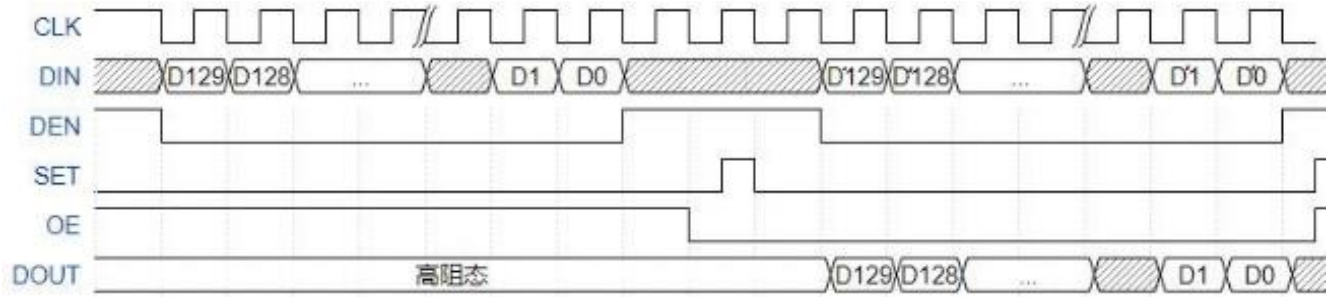

Figure 26. Data input timing

DIN has a total of 130 digits;

SET is the trigger signal

When DEN is low, the digital sample is valid;

DOUT is the data serial output and is in high impedance state when OE is high.

Parallel port output timing (TR switching)

7.4. Parallel port output timing

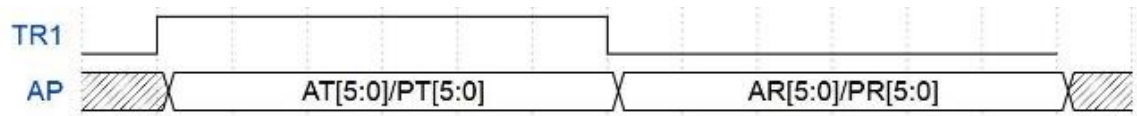

Figure 27.

7.5. FIN data input timing

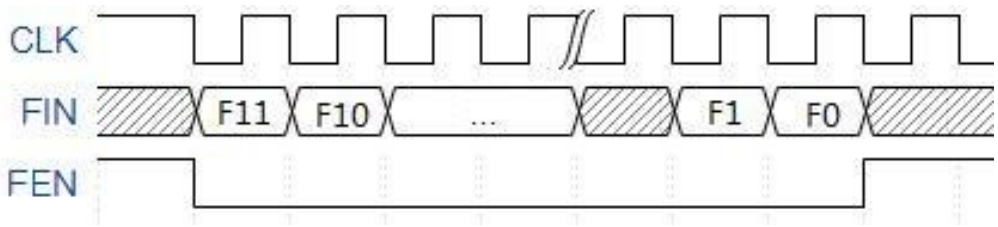

Figure 28.

VIII. Packaging Solutions

The chip adopts QFN68 pin package with a size of 8mm×8mm. The detailed size information is shown in the figure below.

The metal on the back of the chip after packaging is the ground terminal of the DC and AC signals of the entire chip and the main heat dissipation output terminal of the chip. When used, it needs to have a fully ideal connection with the ground plane on the board and fully good heat dissipation.

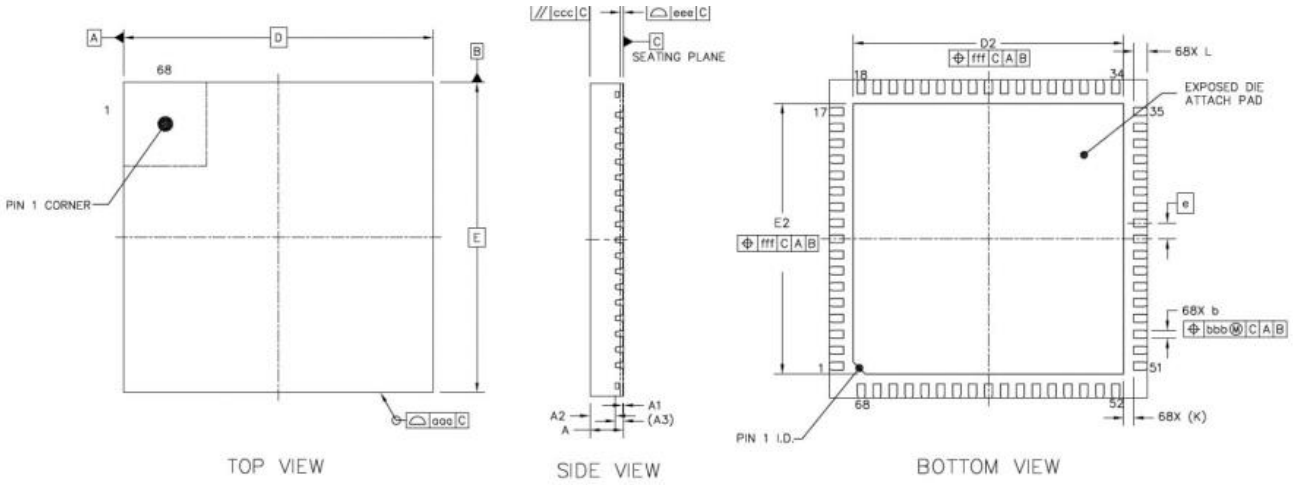

Figure 29. Package front view, side view, bottom view

8.1. Package size

Table 7.

DIMENSION SYMBOLS	VALUE (MM)		
	MINIMUM	NOMINAL	MAXIMUM
A	0.8	0.85	0.9
A1	0	0.02	0.05
A2	—	0.65	—
A3		0.203 REF	
b	0.15	0.20	0.25

DIMENSION SYMBOLS	VALUE (MM)		
	MINIMUM	NOMINAL	MAXIMUM
D		8 BSC	
E		8 BSC	
e		0.4 BSC	
D2	6.7	6.8	6.9
E2	6.7	6.8	6.9
L	0.25	0.35	0.45
K		0.25 REF	
aaa		0.1	
ccc		0.1	
eee		0.08	
bbb		0.07	
fff		0.1	

IX. Application Circuit

BSTCC58-1418 chip adopts plastic QFN package, with 68 pins in total. The recommended application circuit diagram is shown in the figure below.

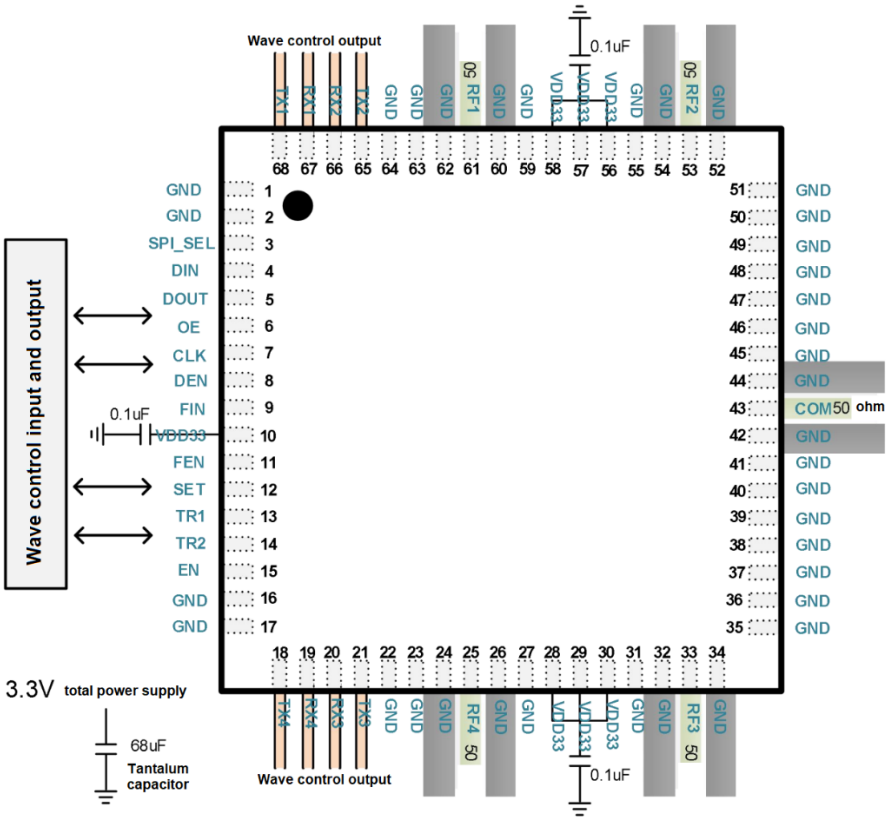

Figure 30

COM, RF1, RF2, RF3 and RF4 are both RF signal ports, which require 50 ohm transmission lines to connect. RF signal ports do not require external DC blocking capacitors. The power supply voltage of this chip is 3.3V. When used, a 0.1uF chip capacitor is placed close to the chip VDD33 pin to the ground. In addition, this four-channel chip requires at least 68uF tantalum capacitor filtering to reduce the fluctuation of the chip power supply voltage during pulse switching.

The back of the chip is the ground terminal for DC and AC. It needs to be fully grounded when used and provide a good heat dissipation path.