BSTCC36-0812

X-Band Four-Channel Multi-Function Chip

Data Sheet

I. Product Introduction

BSTCC36-0812 is a highly integrated four-channel multi-function chip in X-band, powered by 3.3V power supply, with an operating frequency range of 8GHz to 12GHz.

The chip integrates low noise amplifier, power amplifier, switch, 6 -digital control attenuator, 6 -digital control phase shifter, power divider, beam control and other modules, which can provide a maximum attenuation range of 31.5dB, step 0.5dB, and a 360° phase shift range, step 5.625°. The chip adopts plastic QFN package, with a total of 76 pins and a chip size of 9×9mm.

II. Application Areas

- radar
- Communication System

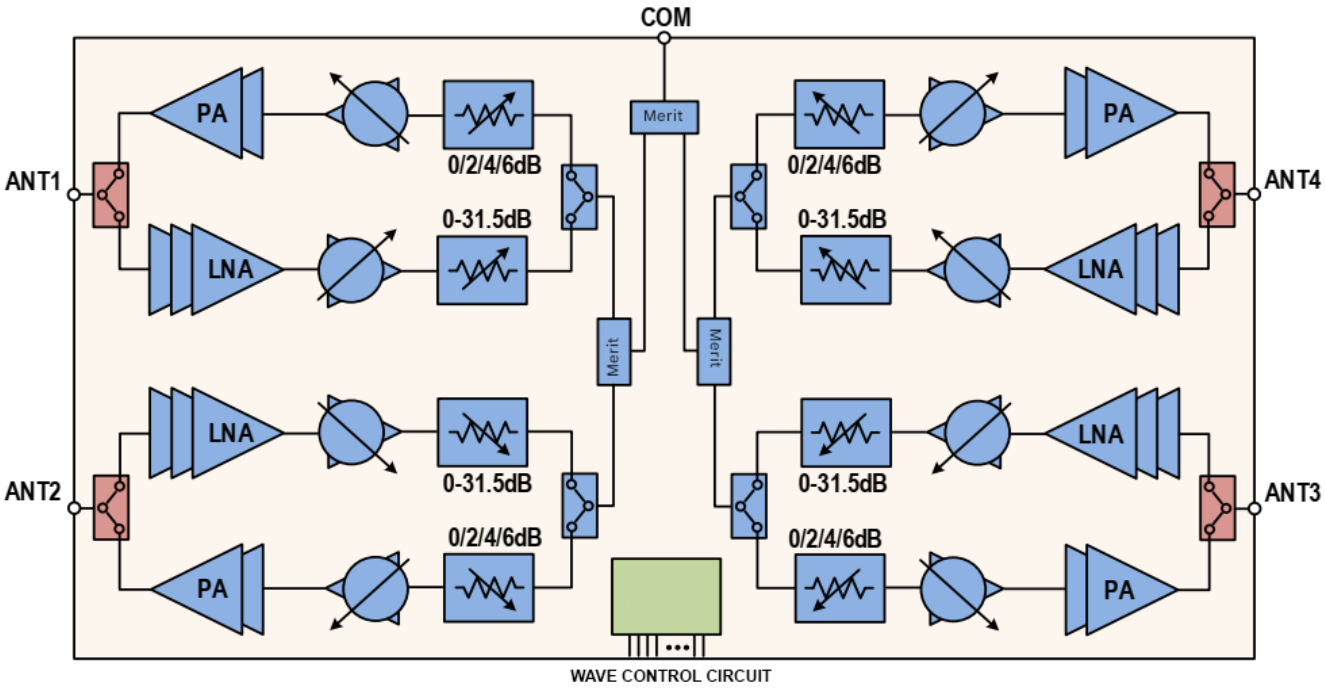

Figure 1. BSTCC36-0812 structure diagram

III. Key technical indicators

- Working power supply voltage: 3.3V
- Operating frequency range: 8GHz ~ 12GHz
- 6 -bit attenuation control, step 0.5dB
- 6 phase shift control bits, stepping 5.625°
- Receive gain: 12dB@10GHz (ANT port to COM port)
- Transmitter gain: 18dB@10GHz (COM port to ANT port) (2dB/4dB/6dB attenuation adjustable, minimum adjustable to 12dB)
- Port VSWR: < 2@8 ~ 10.5GHz
- Receive noise factor NF: 3dB (no attenuation)
- Receive input P-1dB: -38dBm
- Transmit output Psat: 28dBm@8～10.5GHz
- RMS phase shift error: < 4°
- Amplitude consistency during phase shift: < ±1dB
- Attenuation accuracy: < 0.2+2%Ai
- Attenuation additional phase shift: < ±8°
- Transmit and receive switching time: < 150ns
- Four-channel operating current: 160mA/3600mA
  @10GHz receiving / continuous wave saturation transmitting
- Package and size: QFN 9×9mm

IV. Basic electrical properties

Table 1.

PARAMETER	CONDITION	MINIMUM	TYPICAL VALUE	MAXIMUM	UNIT
Frequency range		8	—	12	GHz
Receive linear gain	ANTn port to COM port	—	12	—	dB
Transmit linear gain	COM port to ANTn port	—	18	—	dB
Port VSWR	8 to 10.5 GHz	—	—	2	—
Receive noise figure	No attenuation	—	-3	—	dB
Receive input P-1dB		—	-38	—	dBm
Transmit output Psat	8 ~ 10.5GHz, COM port input 14dBm, 1us pulse width, 10% transmit duty cycle	27.5	28	—	dBm

PARAMETER	CONDITION	MINIMUM	TYPICAL VALUE	MAXIMUM	UNIT
RMS Phase Shift Error		—	—	4	Deg
Phase shift amplitude consistency		-1	—	1	dB
RMS attenuation error		—	—	0.5	dB
Attenuation of additional phase shift		-8	—	8	Deg
Transmit/receive switching time		—	—	150	ns
Four-channel receiving current		—	160	—	mA
Four-channel transmitter quiescent current	COM port not activated	—	1200	—	mA
Four-channel emission current	CW saturation emission 10GHz	—	3600	—	mA
Four-channel emission current	CW saturation emission 8GHz	—	4400	—	mA

4.1. Digital port electrical parameters

Table 2.

PARAMETER	SYMBOL	CONDITION	MINIMUM	MAXIMUM	UNIT
Input high level voltage	VIH	VCC = 2.7 V to 3.6 V	1.7	—	V
Input low level voltage	VIL	VCC = 2.7 V to 3.6 V	—	0.8	V
Input high level current	IIH	VCC = 2.7 V to 3.6 V	-500	500	uA
Input low level current	IIL	VCC = 2.7 V to 3.6 V	-500	500	uA
Output high level voltage	VOH	VCC = 2.7 V to 3.6 V IOH = –100 uA	VCC-0.2	VCC	V
Output high level voltage	VOH	VCC = 2.7 V IOH = –8 mA	2.4	VCC	V
Output low level voltage	VOL	VCC = 2.7 V to 3.6 V IOL= 100uA	0	0.2	V
Output low level voltage	VOL	VCC = 2.7 V, IOL = 8 mA	0	0.4	V

4.2. Use limit parameters

Table 3.

PARAMETER	VALUE
Maximum supply voltage	+3.6V
Maximum RF input power	+20dBm
Storage temperature	-65 ℃ ~+150 ℃
Operating temperature	-55 ℃ ~+125 ℃

Note: For the above listed maximum limits, if the device is operated in an environment exceeding these limits, it is likely to cause permanent damage to the device.

In actual application, it is best not to operate the device in an environment where the limit value or the value exceeds this limit value.

4.3. ESD Protection

BSTCC36-0812 anti-static level (HBM) is at least Class 1A: ≥250V, <500V. When handling, take appropriate ESD protection measures to avoid performance degradation or functional failure.

V. Pin Configuration

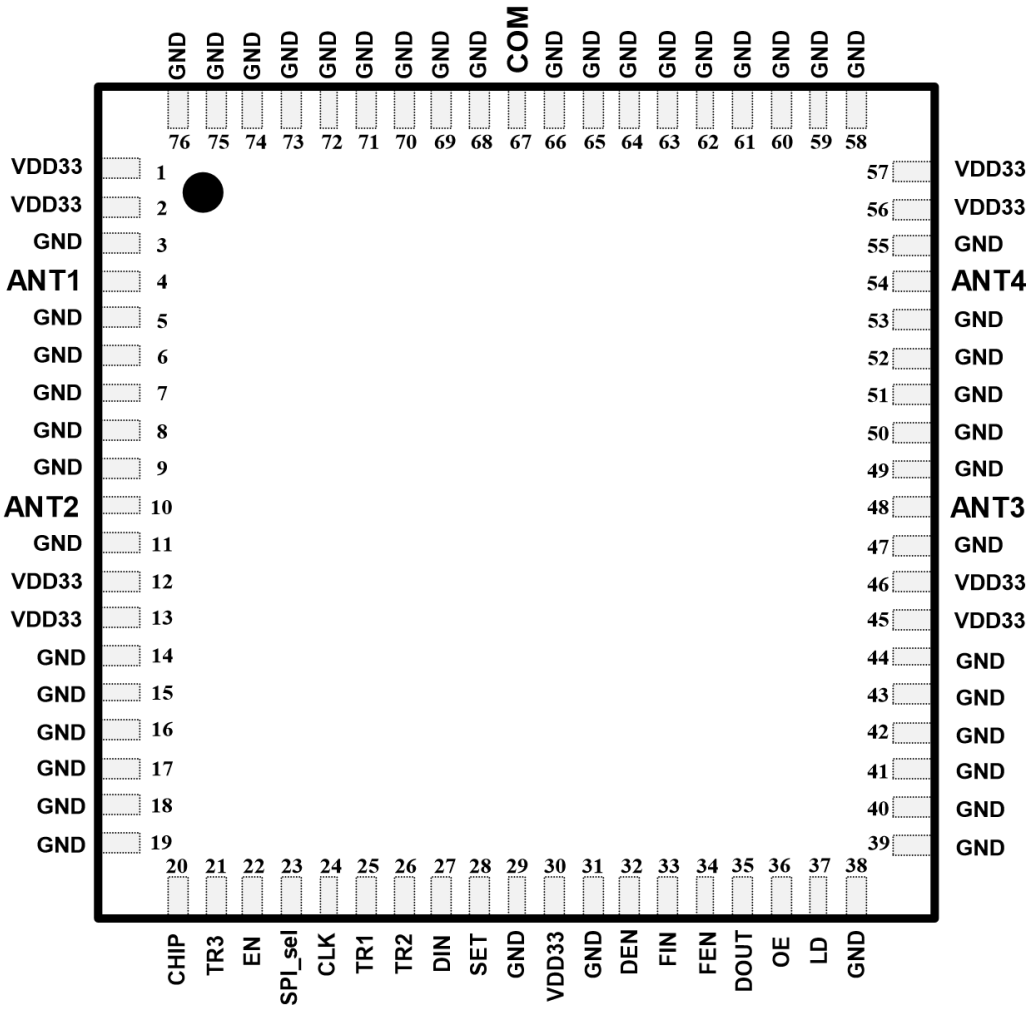

Figure 2. Chip pin layout

5.1. Chip function information table

Table 4.

PIN NUMBER	PIN NAME	PORT ATTRIBUTES	REMARK	PIN NUMBER	PIN NAME	PORT ATTRIBUTES	REMARK
1	VDD33	power supply	Channel 1 3.3V power supply terminal	39	GND	Ground	
2	VDD33	power supply	Channel 1 3.3V power supply terminal	40	GND	Ground	
3	GND	Ground		41	GND	Ground	
4	ANT1	Radio Frequency	Channel 1 RF Port	42	GND	Ground	
5	GND	Ground		43	GND	Ground	
6	GND	Ground		44	GND	Ground	
7	GND	Ground		45	VDD33	power supply	Channel 3 3.3V power supply terminal
8	GND	Ground		46	VDD33	power supply	Channel 3 3.3V power supply terminal
9	GND	Ground		47	GND	Ground	
10	ANT2	Radio Frequency	Channel 2 RF port	48	ANT3	Radio Frequency	Channel three RF port
11	GND	Ground		49	GND	Ground	
12	VDD33	power supply	Channel 2 3.3V power supply terminal	50	GND	Ground	
13	VDD33	power supply	Channel 2 3.3V power supply terminal	51	GND	Ground	
14	GND	Ground		52	GND	Ground	
15	GND	Ground		53	GND	Ground	
16	GND	Ground		54	ANT4	Radio Frequency	Channel four RF port
17	GND	Ground		55	GND	Ground	
18	GND	Ground		56	VDD33	power supply	Channel 4 3.3V power supply terminal
19	GND	Ground		57	VDD33	power supply	Channel 4 3.3V power supply terminal
20	CHIP	Input	Channel control, weak pull-down, default ground	58	GND	Ground	
21	TR3	Input	Channel control, weak pull-down, default ground	59	GND	Ground	
22	EN	Input	Enable control, weak pull-down, default grounding	60	GND	Ground	
23	SPI_sel	Input	Wave control mode connects to 3.3V voltage or floats, weak pull-up, default connection is high	61	GND	Ground	

PIN NUMBER	PIN NAME	PORT ATTRIBUTES	REMARK	PIN NUMBER	PIN NAME	PORT ATTRIBUTES	REMARK
24	CLK	Input	Clock, weak pull-down	62	GND	Ground	
25	TR1	Input	Receive switch control, weak pull-down	63	GND	Ground	
26	TR2	Input	Pulse emission switch control, weak pull-down	64	GND	Ground	
27	DIN	Input	Serial data input, weak pull-down	65	GND	Ground	
28	SET	Input	Three-level register latch, weak pull-down	66	GND	Ground	
29	GND	Ground		67	COM	Radio Frequency	RF common port
30	VDD	power supply	Wave control 3.3V power supply terminal	68	GND	Ground	
31	GND	Ground		69	GND	Ground	
32	DEN	Input	Secondary latch signal, weak pull-up	70	GND	Ground	
33	FIN	Input	Function register input, weak pull-down	70	GND	Ground	
34	FEN	Input	Function register enable, weak pull-up	72	GND	Ground	
35	DOUT	Output	Serial data output, weak pull-up	73	GND	Ground	
36	OE	Input	Output enable, weak pull-up	74	GND	Ground	
37	LD	Input	Self-test control, weak pull-down	75	GND	Ground	
38	GND	Ground		76	GND	Ground	

VI. Typical test curve

(unless otherwise specified, the test conditions are 3.3V power supply voltage and room temperature)

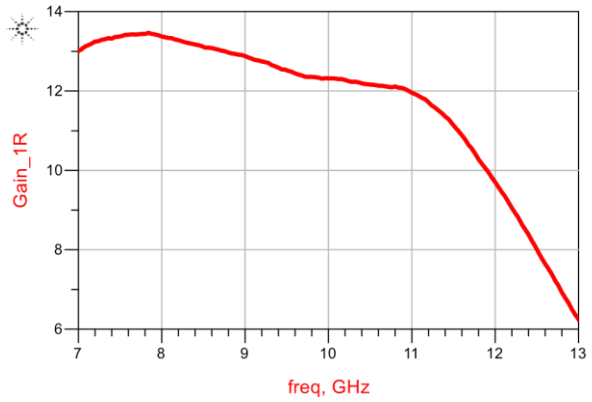

Figure 3. Receive Gain (ANTn to COM)

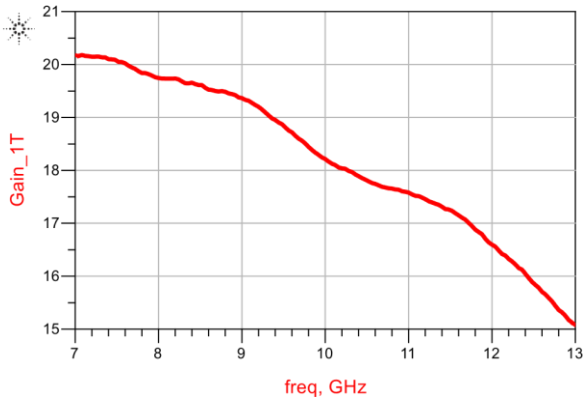

Figure 4. Transmitter Gain (COM to ANTn)

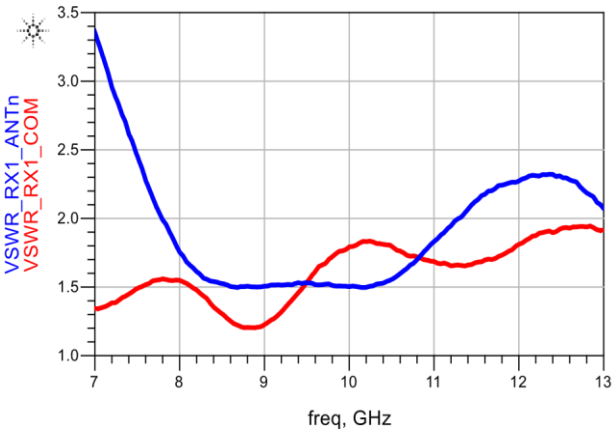

Figure 5. Receive mode port VSWR

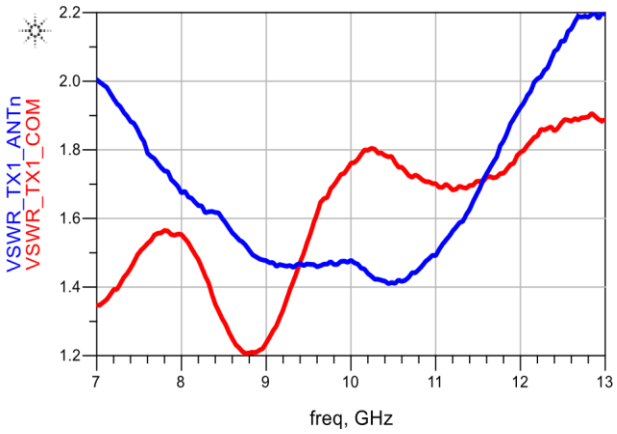

Figure 6. Transmit mode port standing wave ratio

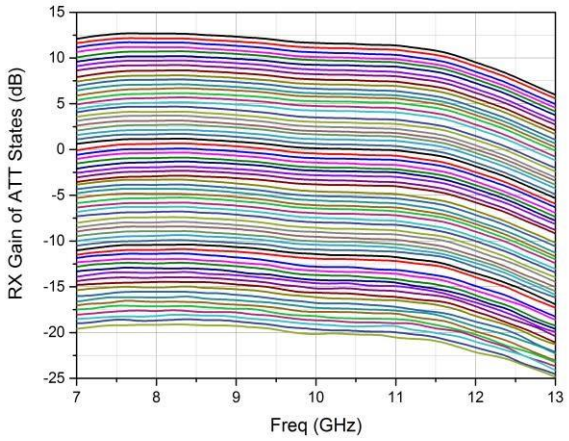

Figure 7. Receive gain 64 -state attenuation curve vs frequency

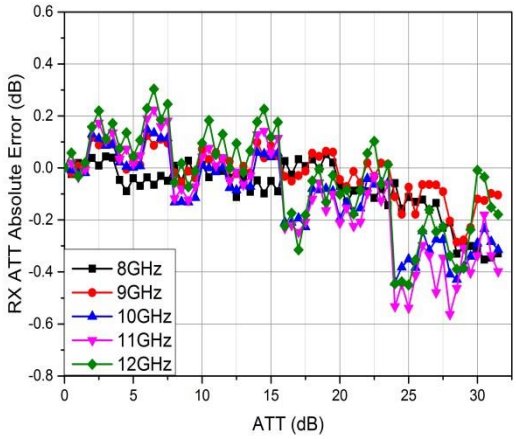

Figure 8. Receive mode attenuation error vs attenuation value

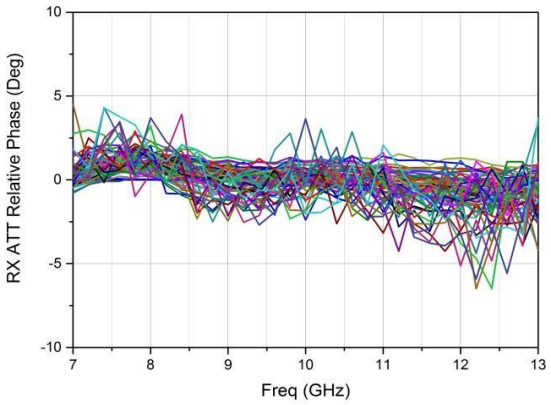

Figure 9. Additional phase shift vs frequency when receiving mode 64- state attenuation

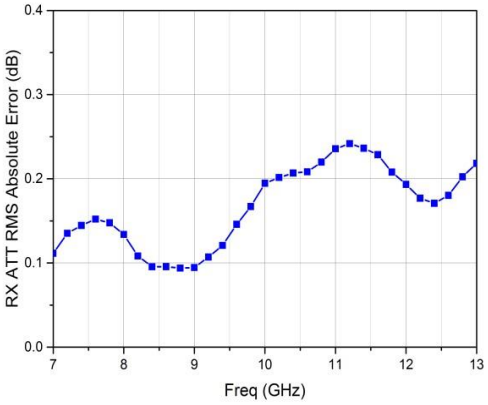

Figure 10. Receive Mode RMS Attenuation Error vs Frequency

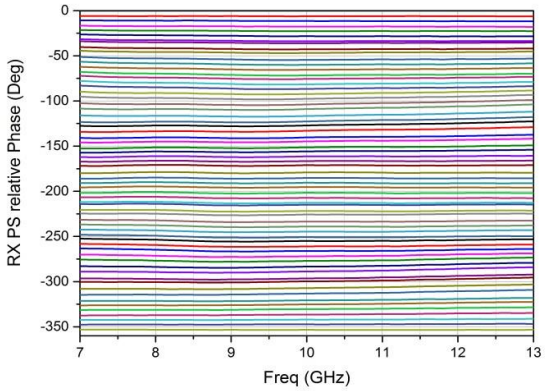

Figure 11. Receiving mode 64 -state relative phase shift curve vs frequency

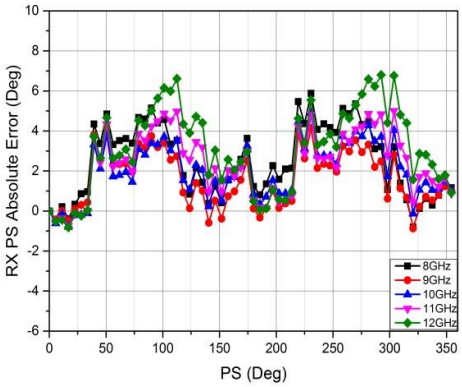

Figure 12. Receive mode phase shift error vs phase shift value

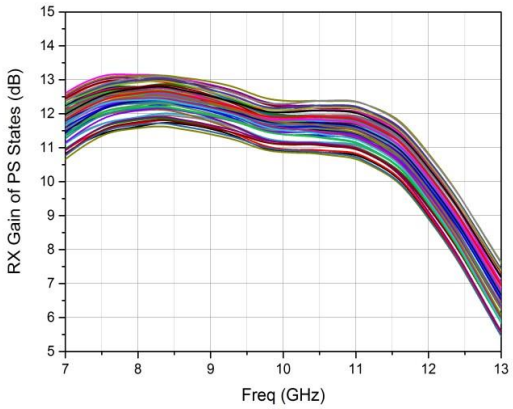

Figure 13. vs frequency in 64 -state phase shift in receiving mode

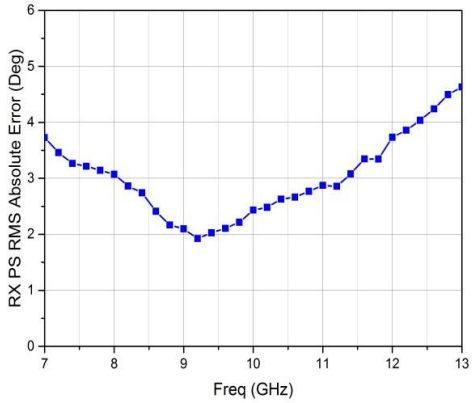

Figure 14. Receive Mode RMS Phase Error vs Frequency

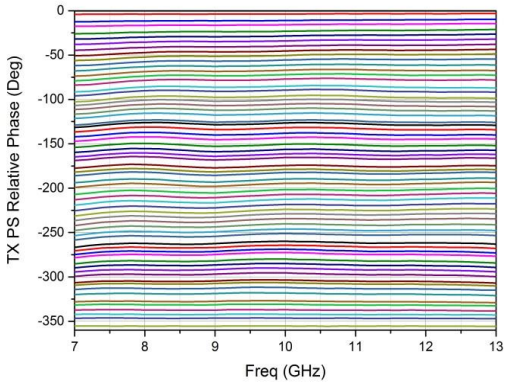

Figure 15. Transmit mode 64 -state relative phase shift curve vs frequency

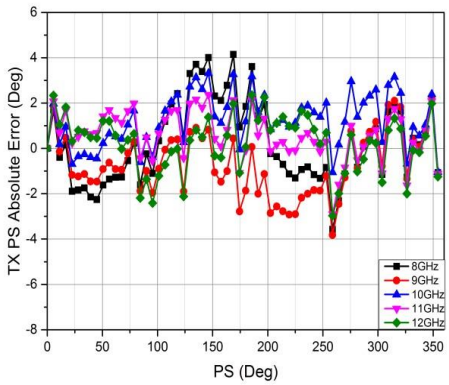

Figure 16. Transmit mode phase shift error vs phase shift value

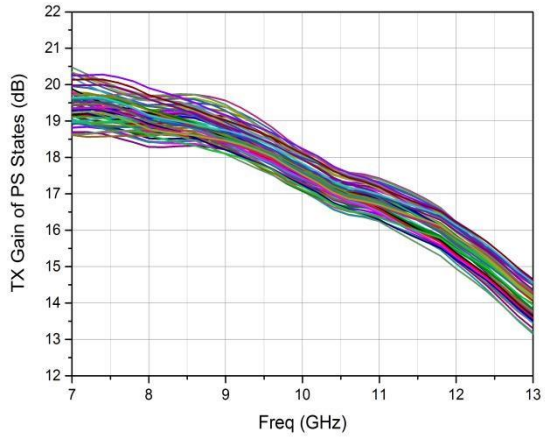

Figure 17. Gain curve vs frequency in 64 -state phase shift in transmit mode

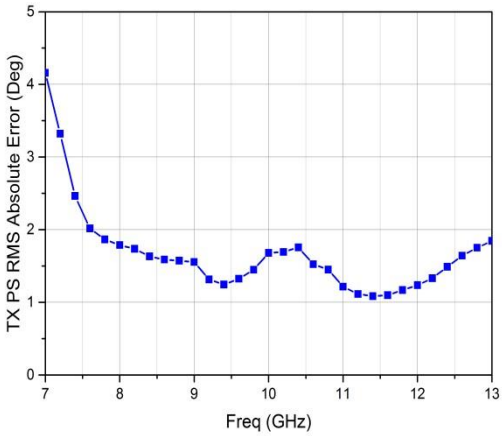

Figure 18. Transmit Mode RMS Phase Error vs Frequency

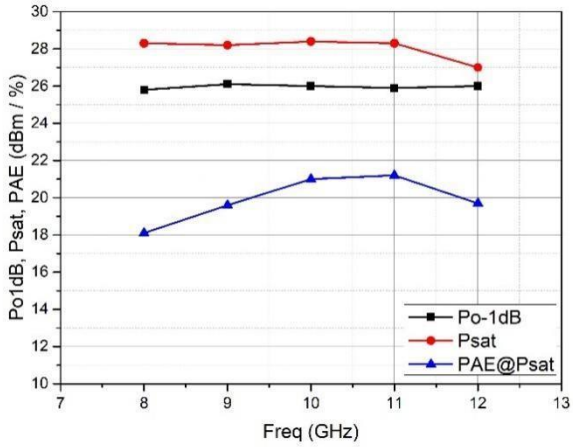

Figure 19. Transmit output 1dB power, saturation power, efficiency vs frequency 10GHz

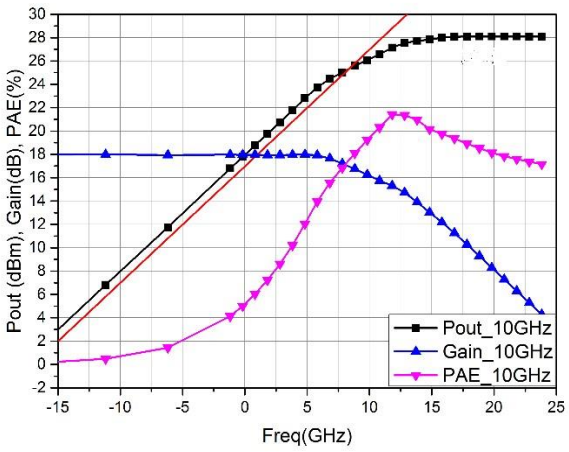

Figure 20. transmit output power, transmit efficiency, gain vs input power

VII. Digital control function

The SPI_sel signal is connected to a high level by default, which is the wave control mode.

7.1. Status control output description

For the transmit/receive status control, the four channels use the same logic control input, and the transmit/receive status control bits of each channel output the status of the corresponding channel respectively.

Table 5. Status Control Description

INPUT					CORRESPONDING CHANNEL STATUS
EN	TR1	TR2	MCT	MCR	
0	0	0	x	0	Receiving state
0	1	0	x	0	Transition state
0	1	1	0	x	Emission state
Other combinations					Load state

Note 1: When configuring the transmit state, first input 12'h3e0 through FIN to configure the function register.

Note 2: After power-on, the default value of MCT=MCR is 1, and the chip is in load state by default. When switching the transmit and receive states, MCT and MCR need to be configured accordingly.

VIII. Wave control timing diagram

1. Data input timing

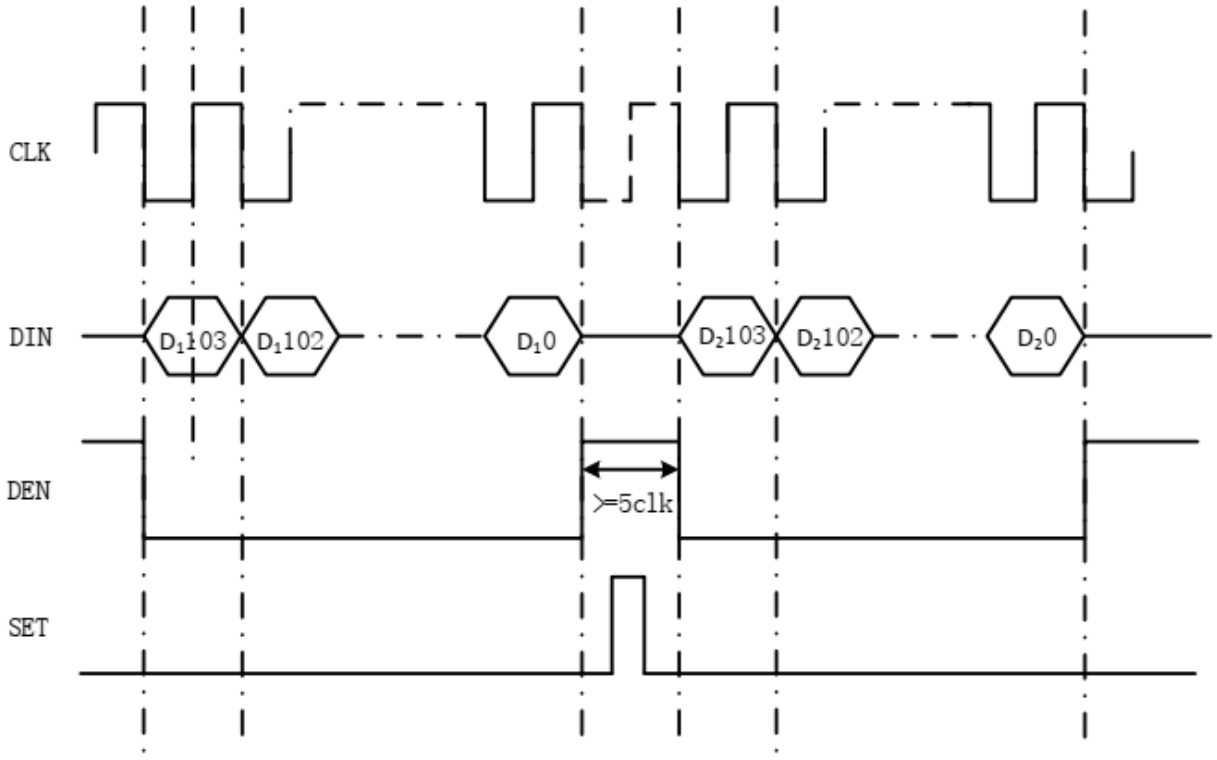

Figure 21. Wave control timing diagram

DEN is low, CLK rises and data is written from the DIN port. The 104 -bit data of the four channels is defined as follows: AT,

AR is the transmit and receive attenuation values, PT and PR are the transmit and receive phase shift values respectively; the rising edge of SET updates the data.

Table 6.

FIRST CHANNEL					
D[25:20]	D19	D18	D[17:12]	D[11:6]	D[5:0]
AT1[5:0]	MCT1	MCR1	AR1[5:0]	PT1[5:0]	PR1[5:0]
			Second channel		
D[51:46]	D45	D44	D[43:38]	D[37:32]	D[31:26]
AT2[5:0]	MCT2	MCR2	AR2[5:0]	PT2[5:0]	PR2[5:0]
			Third Channel		
D[77:72]	D71	D70	D[69:64]	D[63:58]	D[57:52]
AT3[5:0]	MCT3	MCR3	AR3[5:0]	PT3[5:0]	PR3[5:0]
			Fourth channel		
D[103:98]	D97	D96	D[95:90]	D[89:84]	D[83:78]
AT4[5:0]	MCT4	MCR4	AR4[5:0]	PT4[5:0]	PR4[5:0]

104 -bit data definition

2. Function Register Input Timing

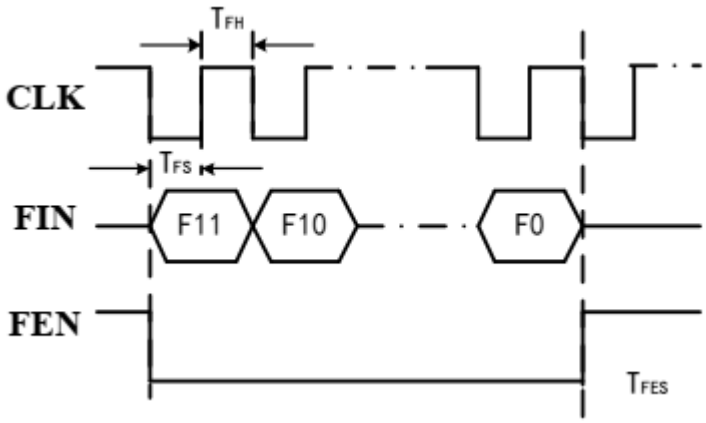

Figure 22. Function Register Input Timing

When FEN is low, data is input from the FIN port at the rising edge of CLK.

3. Serial Output Timing

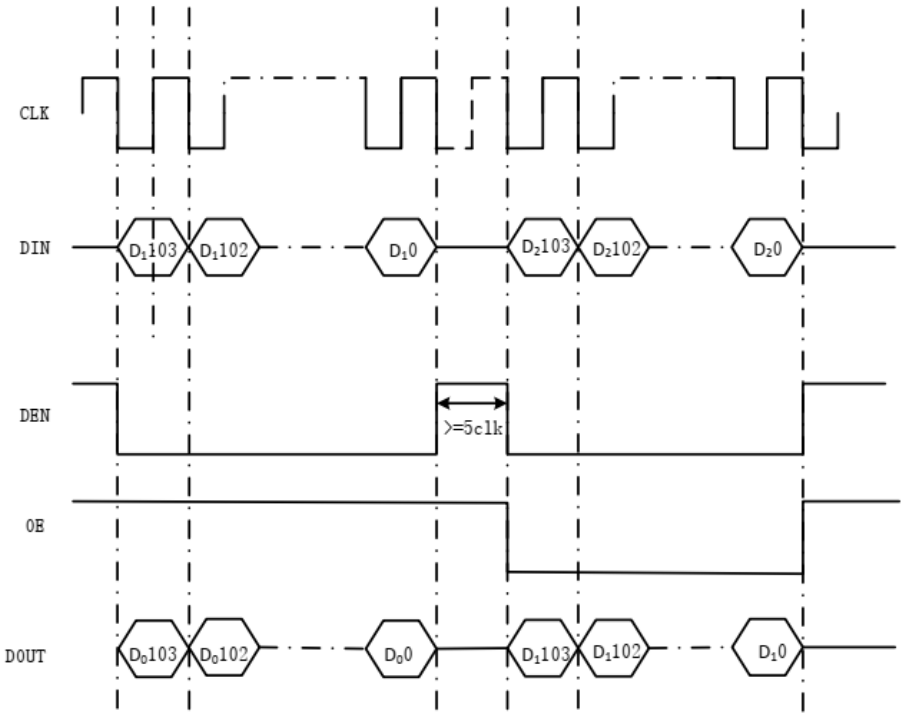

Figure 23. Serial Output Timing

When continuous input is performed, pull OE low, and DOUT will sequentially output the 104-bit data of the last input, which can be used in chip cascading scenarios.

IX. Application Information and Application Circuits

BSTCC36-0812 is a highly integrated four-channel multifunctional chip for X -band. The chip integrates low noise amplifier, power amplifier, switch, 6 -digital controlled attenuator, 6 -digital controlled phase shifter, power divider, beam control and other modules. The chip module is shown in Figure 1. The attenuation and phase shift of the received and transmitted signals are realized by encoding the attenuation and phase shift inside the chip. The chip has high sensitivity and high attenuation and phase shift accuracy, which can meet the application requirements of current military and civilian radar systems.

The chip is packaged in plastic QFN, with a total of 76 pins and a chip size of 9×9mm. COM, ANT1, ANT2, ANT3 and ANT4 are all RF signal ports, which require 50 ohm transmission lines to connect. The RF signal ports do not require external DC isolation capacitors. The power supply voltage of this chip is 3.3V. When used, a 0.1uF chip capacitor is placed close to the chip VDD33 pin to the ground. In addition, this four-channel chip requires at least 100uF

tantalum capacitor filtering to reduce the fluctuation of the chip power supply voltage during pulse switching. CHIP, TR3, EN, CLK, TR1, TR2, DIN, SET, DEN, FIN, FEN, DOUT, OE, LD are wave control input and output ports. When the chip is working, the power supply port VDD33 must be powered on first, and then the wave control I/O port control signal must be given.

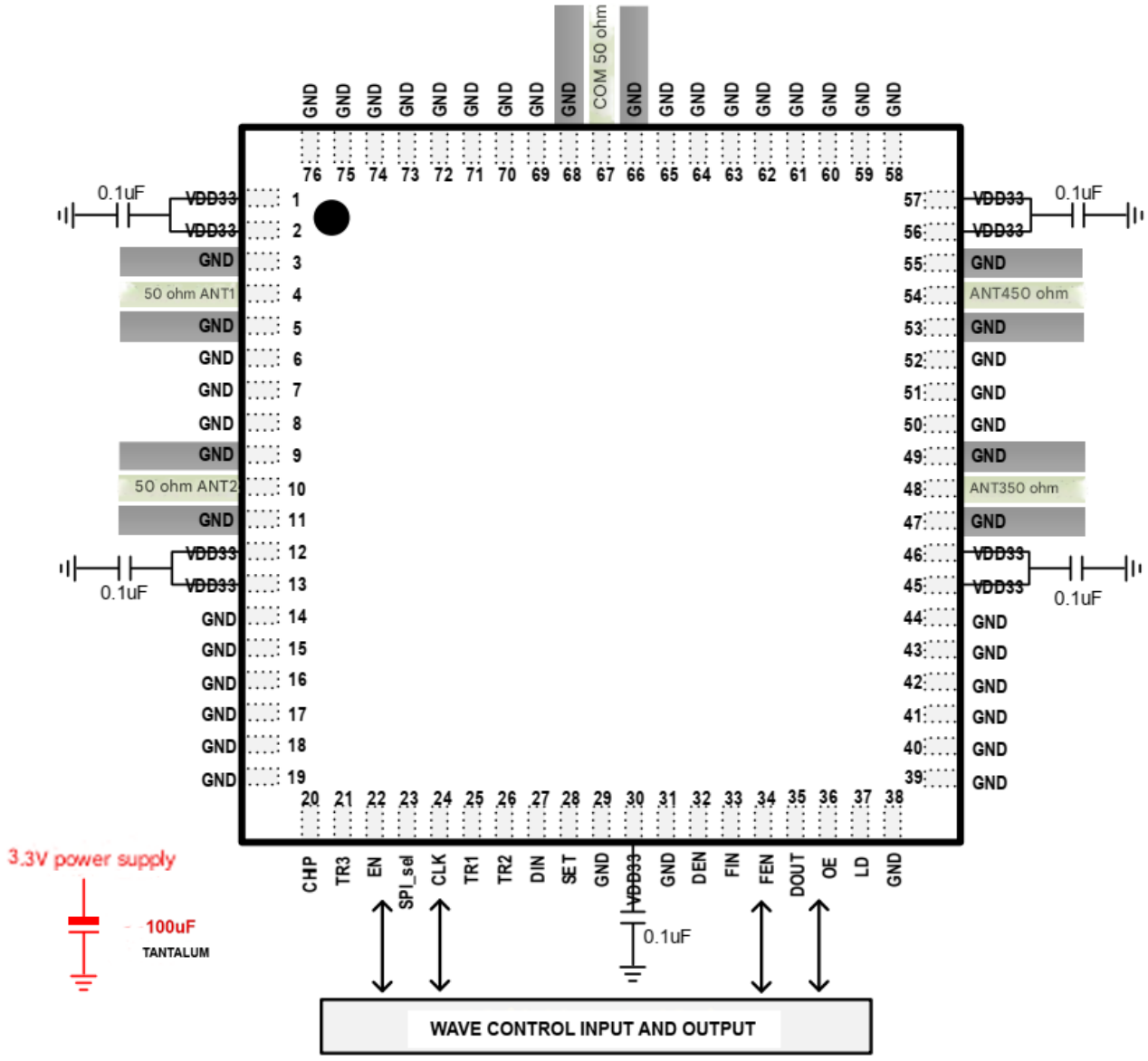

Figure 24. Wave control input and output

X. Application Circuit Packaging Solution

The chip is packaged in QFN76 pins with a size of 9mm×9mm. The detailed size information is shown in the figure below. The metal on the back of the chip after packaging is the ground

terminal of the DC and AC signals of the entire chip and the main heat dissipation output terminal of the chip. When used, it needs to have a sufficient and ideal connection with the ground plane on the board and sufficient and good heat dissipation.

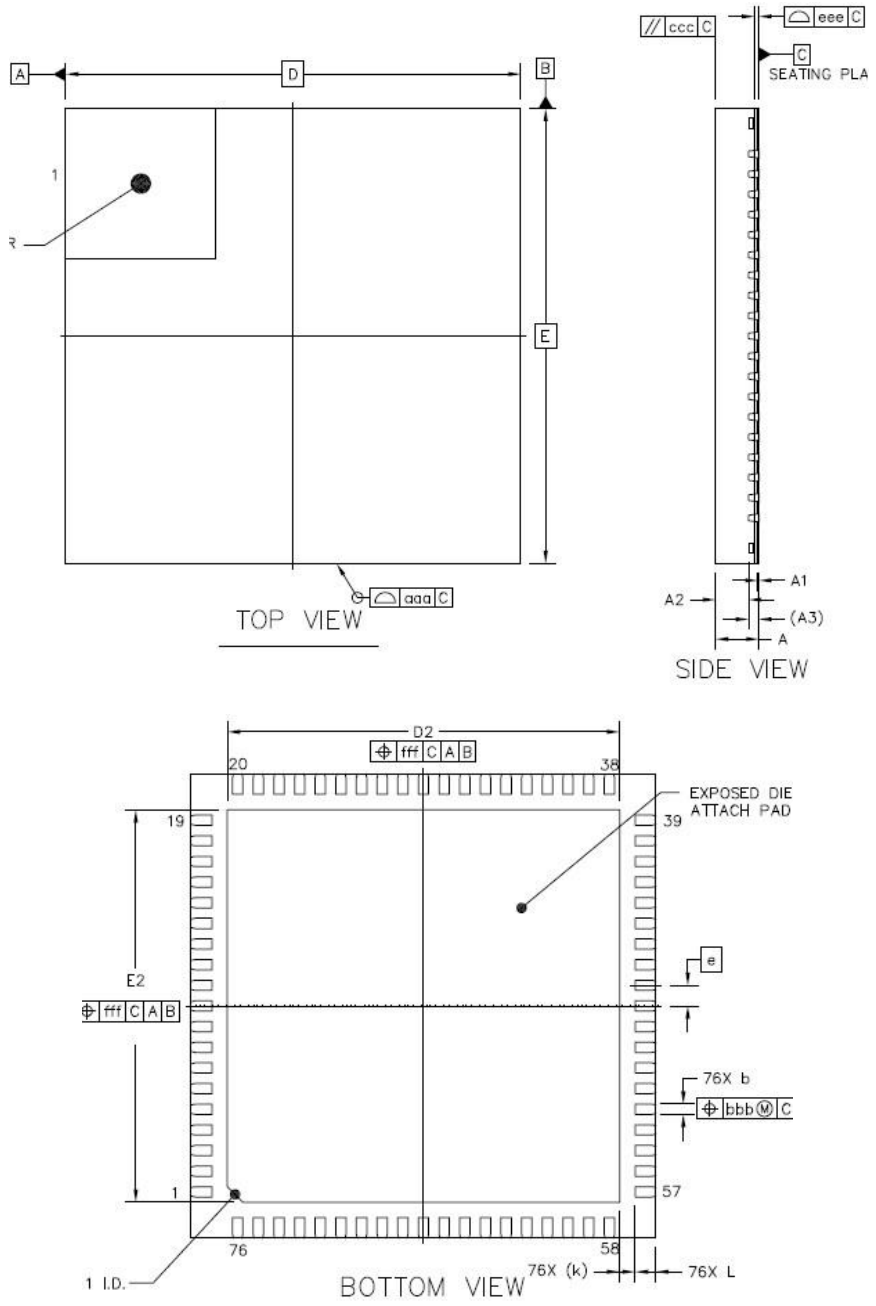

Figure 25. Package front view, side view, bottom view

10.1. Package size table

Table 7.

DIMENSION SYMBOLS	VALUE (MM)		
	MINIMUM	NOMINAL	MAXIMUM
A	0.8	0.85	0.9
A1	0	0.02	0.05
A2	—	0.65	—
A3		0.203 REF	
b	0.15	0.20	0.25
D		9 BSC	
E		9 BSC	
e		0.4 BSC	
D2	7.6	7.7	7.8
E2	7.6	7.7	7.8
L	0.2	0.3	0.4
K		0.35 REF	
aaa		0.1	
ccc		0.1	
eee		0.08	
bbb		0.07	
fff		0.1	