BSTCC35-1518

Ku-band four-channel multi-function chip

Data Sheet

I. Product Introduction

BSTCC35-1518 is a Ku-band highly integrated four-channel multi-function chip, 3.3V power supply, operating frequency range 15GHz ~ 18GHz, The chip integrates low noise amplifier, power amplifier, switch, 6 -digital controlled attenuator, 6 -digital controlled phase shifter, power divider, beam control and other modules, which can provide a maximum attenuation range of 31.5dB, with a step of 0.5dB, and a phase shift range of 360°, with a step of 5.625°. The chip adopts plastic QFN package, with a total of 76 pins and a chip size of 9×9mm.

II. Application Areas

- Radar
- Communication System

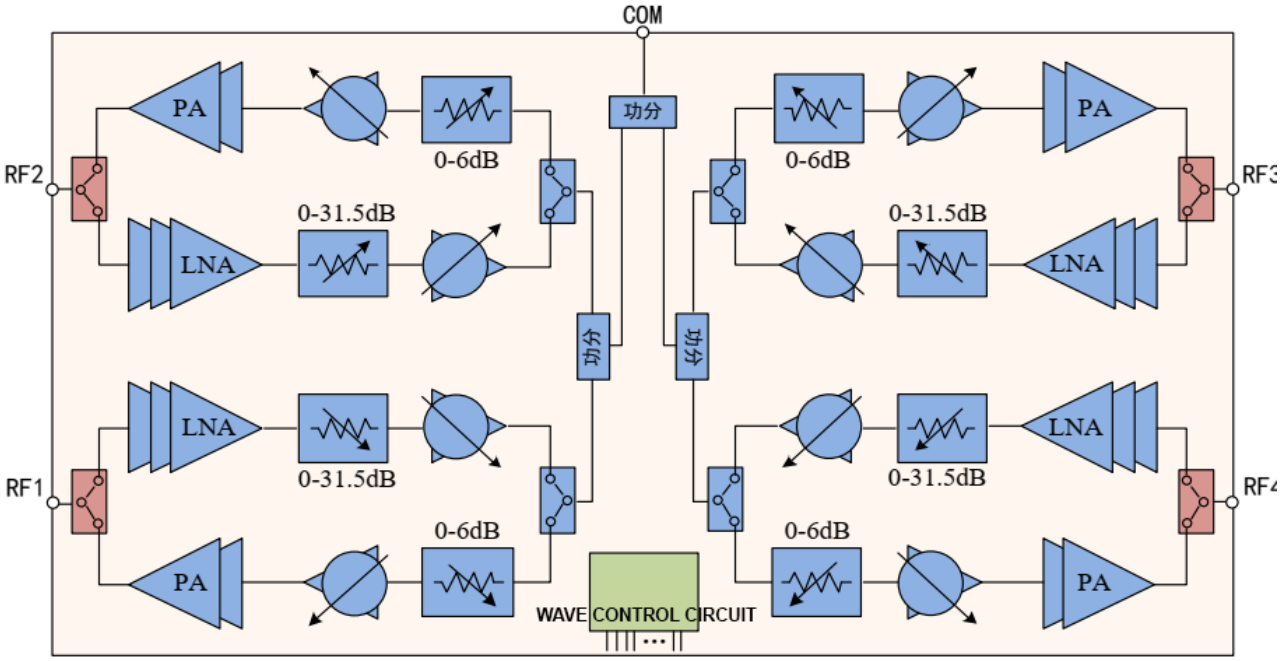

Figure 1. BSTCC35-1518 structure diagram

III. Key technical indicators

- Working power supply voltage: 3.3V
- Operating frequency range: 15GHz ~ 18GHz
- 6 -bit attenuation control, step 0.5dB
- 6 phase shift control bits, stepping 5.625°
- Receive gain: 15dB@17GHz (RF port to COM Port)
- Transmitter linear gain: 16dB@17GHz (COM terminal port to RF port)
- Port standing wave ratio VSWR: < 2
- Receive noise factor NF: 3.1dB
- Receive input P-1dB: -25dBm
- Transmitter output Psat: 24dBm (COM port input power
- Power >12dBm)
- Emission efficiency at saturation emission: 18%
- RMS phase shift error: < 3°
- Amplitude consistency during phase shift: < ±1dB
- Attenuation accuracy: < 0.2+3%Ai
- Attenuation additional phase shift: < ±8°
- Transmit and receive switching time: < 100ns
- Four-channel operating current: 400 mA /2000mA/135mA
  @17GHz receiving / continuous wave saturation transmitting / load state
- Package and size: QFN 9×9mm

IV. Basic electrical properties

Table 1.

PARAMETER	CONDITION	MINIMUM	TYPICAL VALUE	MAXIMUM	UNIT
Frequency range		15	—	18	GHz
Receive linear gain	RFn port to COM port	—	15	—	dB
Transmit linear gain	COM port to RFn port	—	16	—	dB
In-band gain flatness	15.7~17.7GHz	—	—	2	dB
Port VSWR		—	—	2	—
Receive noise figure	No attenuation	—	3.1	—	dB
Receive input P-1dB		—	-25	—	dBm

PARAMETER	CONDITION	MINIMUM	TYPICAL VALUE	MAXIMUM	UNIT
Transmit output P-1dB		—	22	—	dBm
Transmit output Psat		—	24	—	dBm
Transmission efficiency	CW saturation emission	—	18	—	%
RMS Phase Shift Error		—	—	3	Deg
Phase shift amplitude consistency		-1	—	1	dB
RMS attenuation error		—	—	0.5	dB
Attenuation of additional phase shift		-8	—	8	Deg
Transmit/receive switching time		—	—	100	ns
Four-channel receiving current		—	400	—	mA
Four-channel emission current	Static	—	760	—	mA
Four-channel emission current	CW saturation emission, 17GHz	—	2000	—	mA

V. Digital port electrical parameters

Table 2.

PARAMETER	SYMBOL	CONDITION	MINIMUM	MAXIMUM	UNIT
Input high level voltage	VIH	VCC = 2.7 V to 3.6 V	1.7	—	V
Input low level voltage	VIL	VCC = 2.7 V to 3.6 V	—	0.8	V
Input high level current	IIH	VCC = 2.7 V to 3.6 V	-500	500	uA
Input low level current	IIL	VCC = 2.7 V to 3.6 V	-500	500	uA
Output high level voltage	VOH	VCC = 2.7 V to 3.6 V IOH = –100 uA	VCC-0.2	VCC	V
Output high level voltage	VOH	VCC = 2.7 V IOH = –8mA	2.4	VCC	V
Output low level voltage	VOL	VCC = 2.7 V to 3.6 V IOL= 100uA	0	0.2	V
Output low level voltage	VOL	VCC = 2.7 V, IOL= 8mA	0	0.4	V

5.1. Use limit parameters

Table 3.

PARAMETER	VALUE
Maximum supply voltage	+3.6V
Maximum RF input power	+20dBm
Storage temperature	-65 ℃ ~+150 ℃
Operating temperature	-55 ℃ ~+125 ℃

Note: For the above listed maximum limits, if the device is operated in an environment exceeding these limits, it is likely to cause permanent damage to the device.

In actual application, it is best not to operate the device in an environment where the limit value or the value exceeds this limit value.

5.2. ESD Protection

BSTCC35-1518 anti-static level (HBM) is at least Class 1A: ≥250V, <500V. When handling, take appropriate ESD protection measures to avoid performance degradation or functional failure.

VI. Pin Configuration

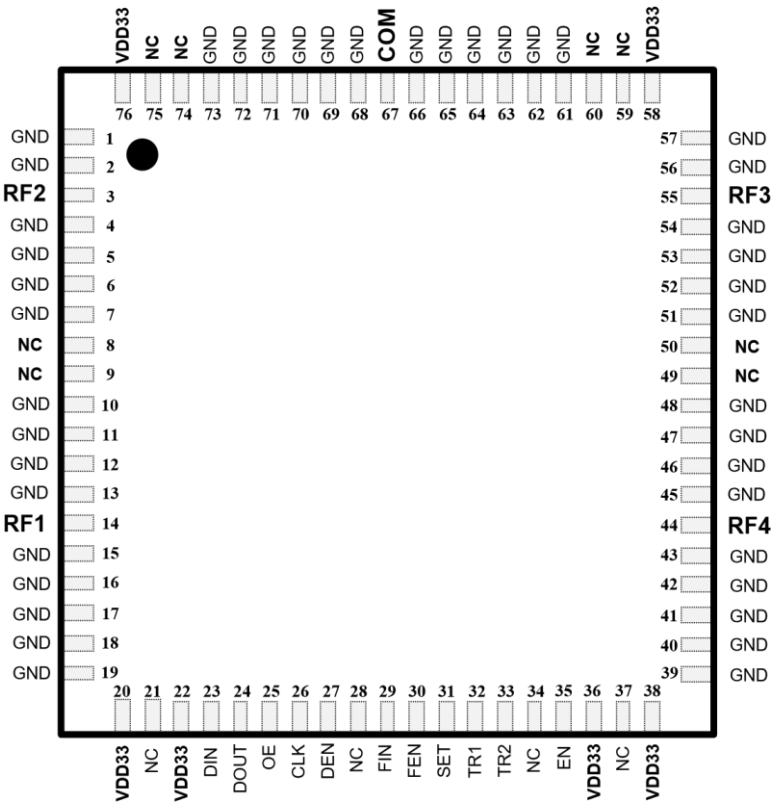

Figure 2. Chip pin layout

Table 4.

PIN NUMBER	PIN NAME	PORT ATTRIBUTES	REMARK	PIN NUMBER	PIN NAME	PORT ATTRIBUTES	REMARK
1	GND	Ground		39	GND	Ground	
2	GND	Ground		40	GND	Ground	
3	RF2	Radio Frequency	Channel 2 RF port	41	GND	Ground	
4	GND	Ground		42	GND	Ground	
5	GND	Ground		43	GND	Ground	
6	GND	Ground		44	RF4	Radio Frequency	Channel four RF port
7	GND	Ground		45	GND	Ground	
8	NC		Can be left floating or grounded	46	GND	Ground	
9	NC		Can be left floating or grounded	47	GND	Ground	
10	GND	Ground		48	GND	Ground	
11	GND	Ground		49	NC		Can be left floating or grounded
11	GND	Ground		50	NC		Can be left floating or grounded
13	GND	Ground		51	GND	Ground	
14	RF1	Radio Frequency	Channel 1 RF Port	52	GND	Ground	
15	GND	Ground		53	GND	Ground	
16	GND	Ground		54	GND	Ground	
17	GND	Ground		55	RF3	Radio Frequency	Channel three RF port
18	GND	Ground		56	GND	Ground	
19	GND	Ground		57	GND	Ground	
20	VDD33	power supply	Channel 1 3.3V power supply terminal	58	VDD33	power supply	Channel 3 3.3V power supply terminal
21	NC		Can be left floating or grounded	59	NC		Can be left floating or grounded
22	VDD33	power supply	Wave control 3.3V power supply terminal	60	NC		Can be left floating or grounded
23	DIN	Input	Serial data input, weak pull-down	61	GND	Ground	
24	DOUT	Output	Serial data output	62	GND	Ground	
25	OE	Input	Output enable, weak pull-up	63	GND	Ground	
26	CLK	Input	Clock, weak pull-down	64	GND	Ground	

PIN NUMBER	PIN NAME	PORT ATTRIBUTES	REMARK	PIN NUMBER	PIN NAME	PORT ATTRIBUTES	REMARK
27	DEN	Input	Secondary latch signal, weak pull-up	65	GND	Ground	
28	NC		Can be left floating or grounded	66	GND	Ground	
29	FIN	Input	Function register input, weak pull-down	67	COM	Radio Frequency	RF common port
30	FEN	Input	Function register enable, weak pull-up	68	GND	Ground	
31	SET	Input	Three-level register latch, weak pull-down	69	GND	Ground	
32	TR1	Input	Receive switch control, weak pull-down	70	GND	Ground	
33	TR2	Input	Pulse emission switch control, weak pull-down	70	GND	Ground	
34	NC		Can be left floating or grounded	72	GND	Ground	
35	EN	Input	Wave control enable control, weak pull-down	73	GND	Ground	
36	VDD33	power supply	Wave control 3.3V power supply terminal	74	NC		Can be left floating or grounded
37	NC		Can be left floating or grounded	75	NC		Can be left floating or grounded
38	VDD33	power supply	Channel 4 3.3V power supply terminal	76	VDD33	power supply	Channel 2 3.3V power supply terminal

VII. Chip function information table

Typical test curve (unless otherwise specified, the test conditions are 3.3V power supply voltage and room temperature)

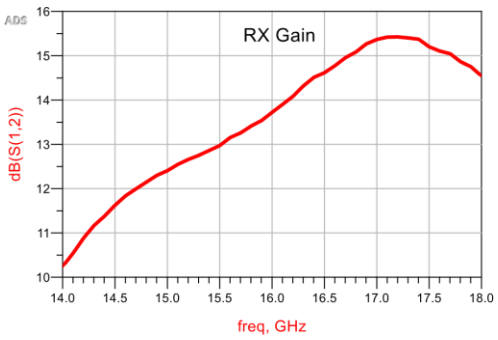

Figure 3. Receive gain (RFn to COM, other channels loaded)

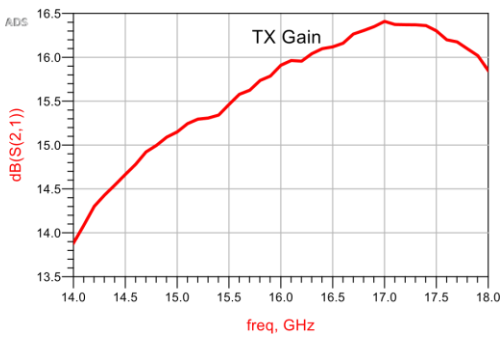

Figure 4. Transmitter gain (COM to RFn, other channels loaded)

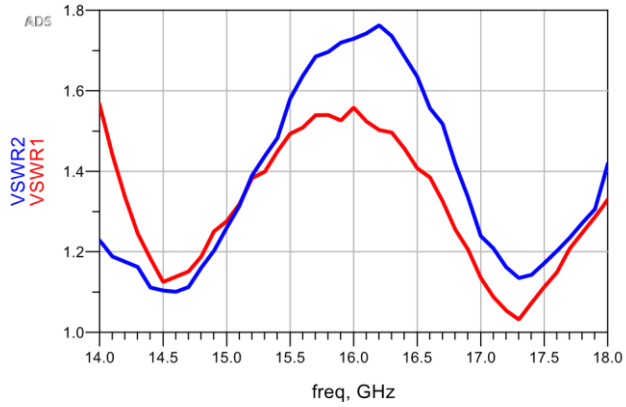

Figure 5. Receiving mode port standing wave ratio (COM is port 1)

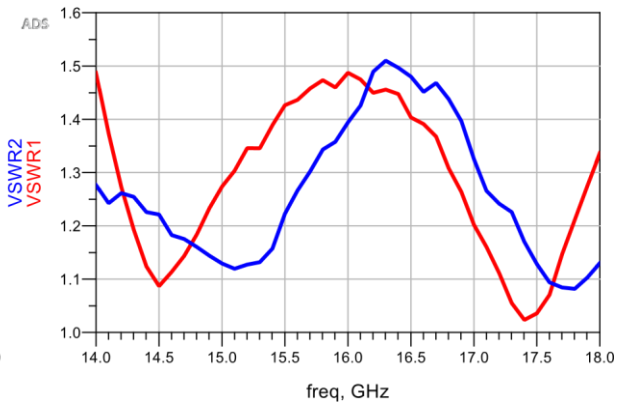

Figure 6. Transmit mode port standing wave ratio (COM is port 1)

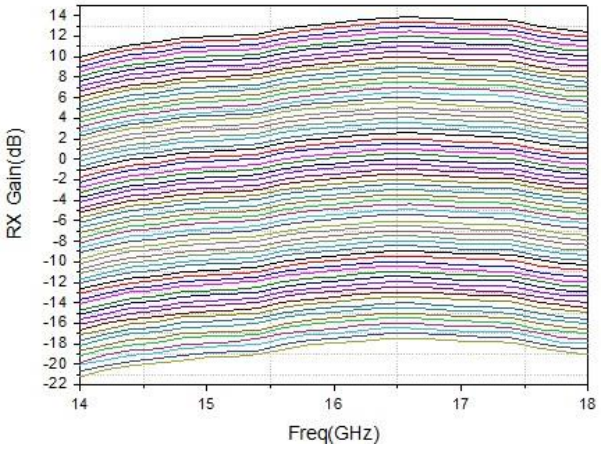

Figure 7. Receive gain 64 -state attenuation curve vs frequency

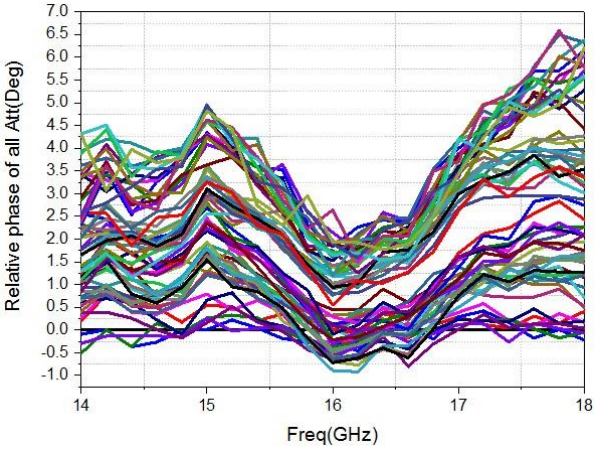

Figure 8. Additional phase shift vs frequency when receiving mode 64- state attenuation

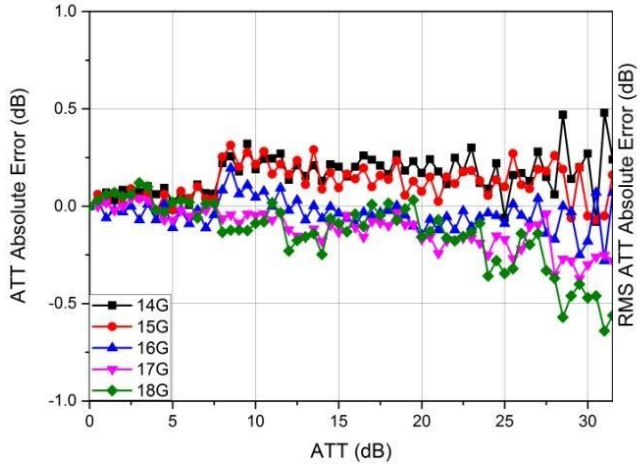

Figure 9. Receive mode attenuation error vs attenuation value graph

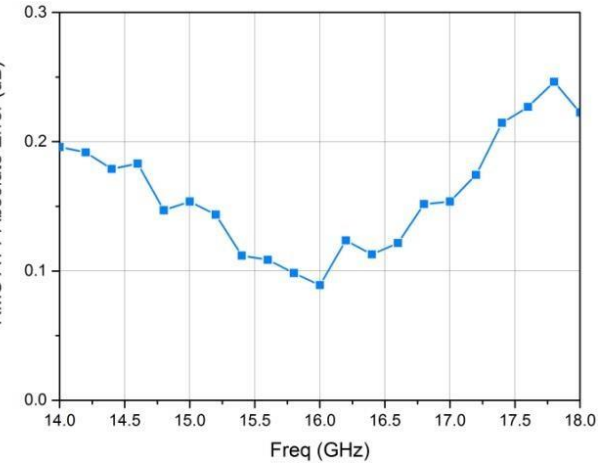

Figure 10. Receive Mode RMS Attenuation Error vs Frequency

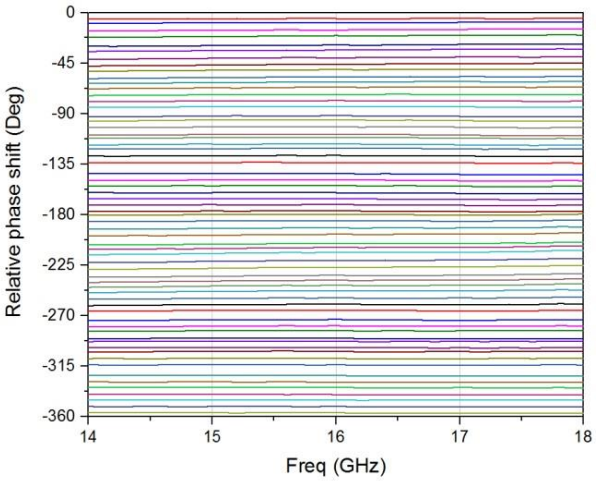

Figure 11. Receiving mode 64 -state relative phase shift curve vs frequency

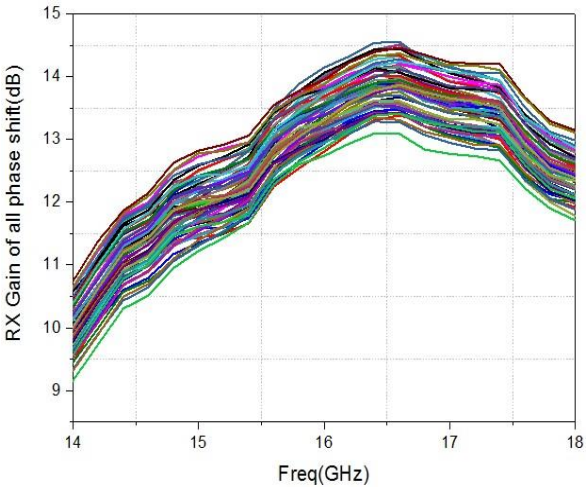

Figure 12. Gain curve vs frequency in 64 -state phase shift in receiving mode

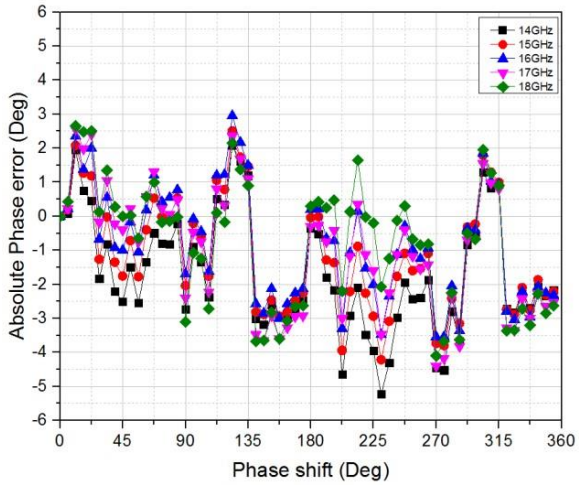

Figure 13. Receive mode phase shift error vs phase shift value

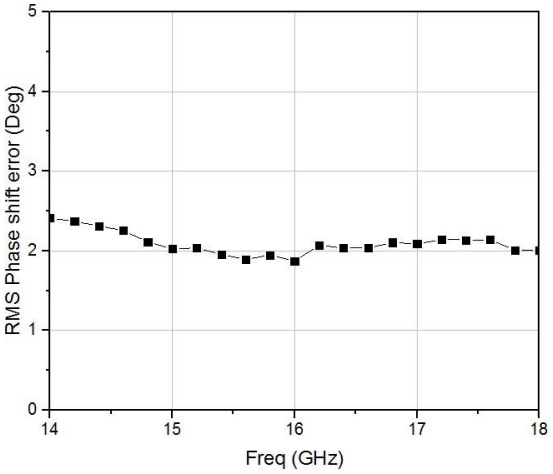

Figure 14. Receive Mode RMS Phase Error vs Frequency

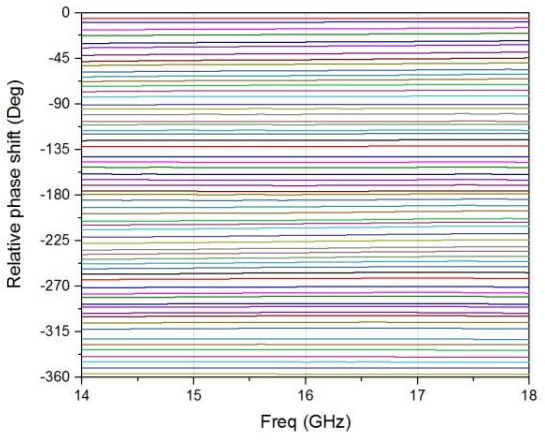

Figure 15. Transmit mode 64 -state relative phase shift curve vs frequency

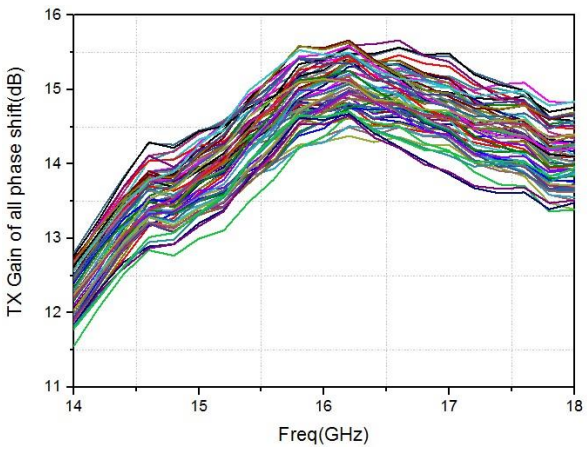

Figure 16. Gain curve vs frequency in 64 -state phase shift in transmit mode

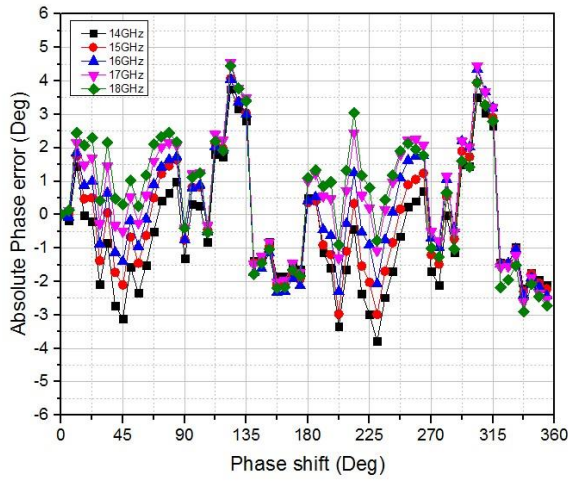

Figure 17. Transmit mode phase shift error vs Phase Shift Value

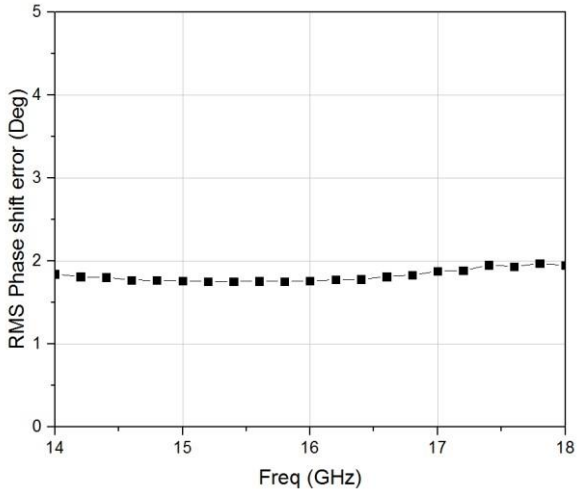

Figure 18. Transmit Mode RMS Phase Error vs Frequency

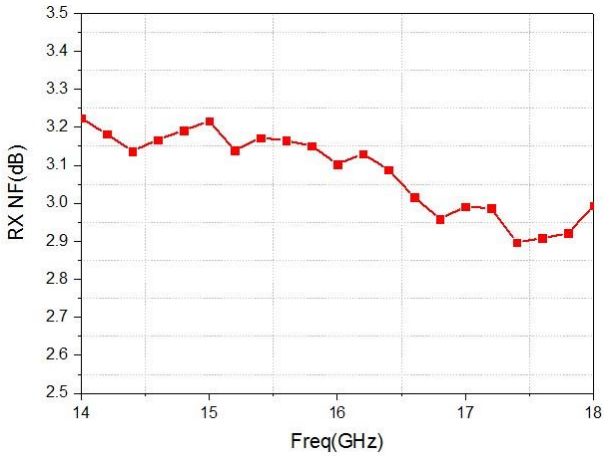

Figure 19. Receive Noise Figure vs Frequency

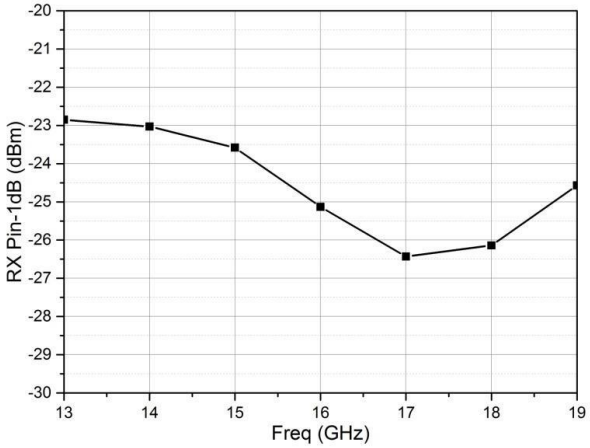

Figure 20. Receive input 1dB power vs frequency

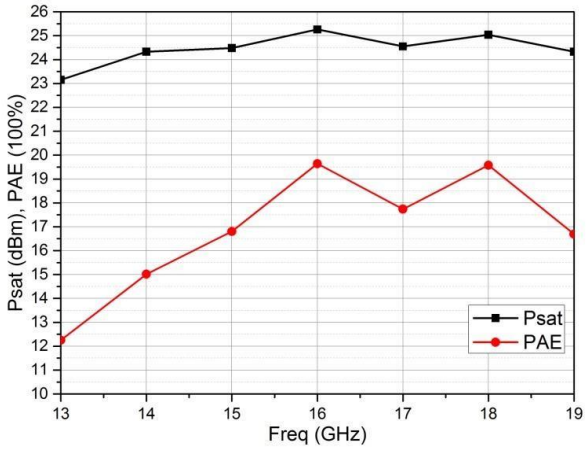

Figure 21. Transmitter saturation power, efficiency vs frequency digital control function

VIII. Status control output description

Transceiver status control, each channel uses the same logic control input, and the transmit and receive status control bits of each channel output the status of the corresponding channel respectively.

Table 5.

ENTER					CORRESPONDING CHANNEL STATUS
EN	TR1	TR2	MCT	MCR	
0	0	0	x	0	Receiving state
0	1	1	0	x	Emission state
Other combinations					Load state

8.1. Status Control Description

Note 1: When configuring the transmit state, first input 12'h3e0 through FIN to configure the function register.

Note 2: After power-on, the default value of MCT=MCR is 1, and the chip is in load state by default. When switching the transmit and receive states, MCT and MCR need to be configured accordingly.

IX. Wave control timing diagram (recommended chip working at 1MHz~20MHz)

1. Data input timing

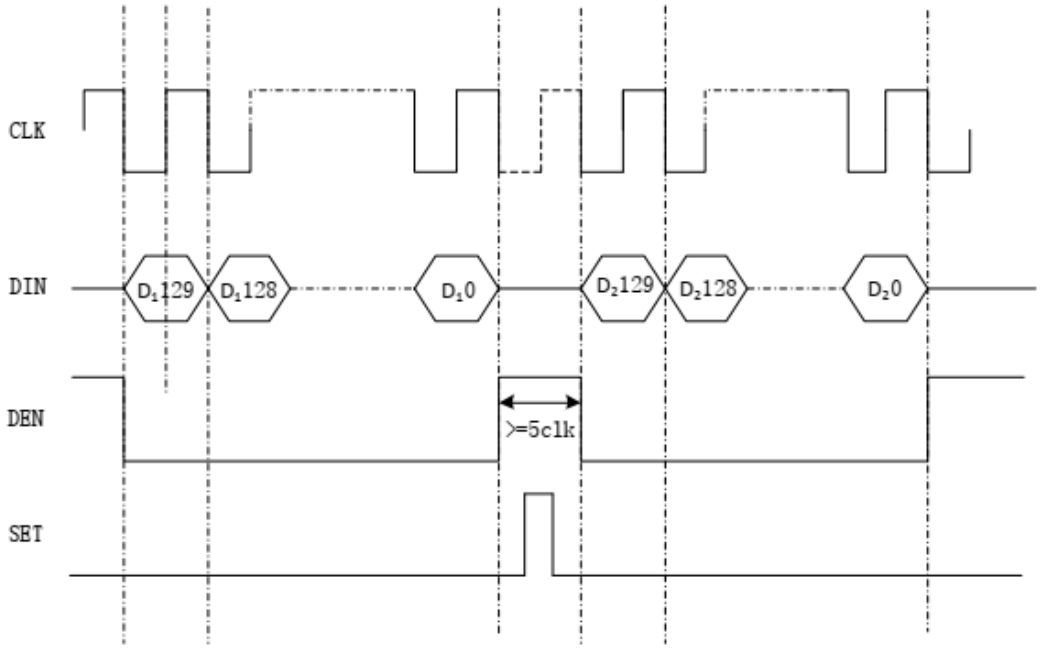

Figure 22. Data input timing

DEN is low, data is written from the DIN port on the rising edge of CLK. The 130 -bit data is defined as follows: AT and AR are the transmit and receive attenuation values, PT and PR are the transmit and receive phase shift values; SET is updated on the rising edge.

Table 6.

FIRST CHANNEL					
D[25:20]	D19	D18	D[17:12]	D[11:6]	D[5:0]
AT1[5:0]	MCT1	MCR1	AR1[5:0]	PT1[5:0]	PR1[5:0]
			Second channel		
D[51:46]	D45	D44	D[43:38]	D[37:32]	D[31:26]
AT2[5:0]	MCT2	MCR2	AR2[5:0]	PT2[5:0]	PR2[5:0]
			Third Channel		
D[77:72]	D71	D70	D[69:64]	D[63:58]	D[57:52]
AT3[5:0]	MCT3	MCR3	AR3[5:0]	PT3[5:0]	PR3[5:0]
			Fourth channel		
D[103:98]	D97	D96	D[95:90]	D[89:84]	D[83:78]
AT4[5:0]	MCT4	MCR4	AR4[5:0]	PT4[5:0]	PR4[5:0]
			Fifth Channel		
D[129:124]	D123	D122	D[121:116]	D[115:110]	D[109:104]
AT5[5:0]	MCT5	MCR5	AR5[5:0]	PT5[5:0]	PR5[5:0]

130-bit data definition

2. Function Register Input Timing

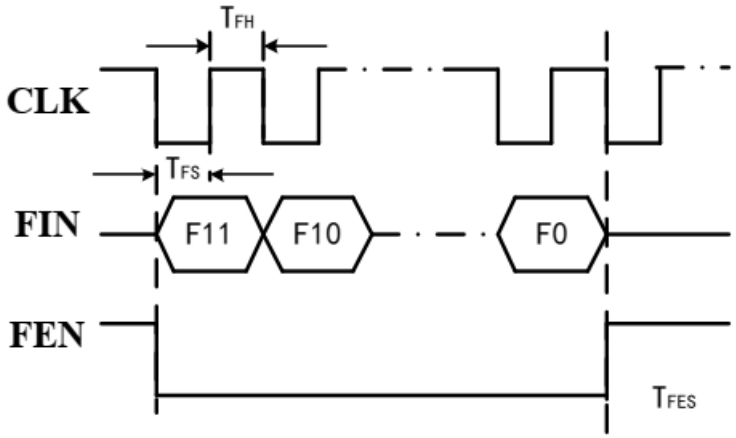

Figure 23. Function Register Input Timing

When FEN is low, data is input from the FIN port at the rising edge of CLK.

3. Serial Output Timing

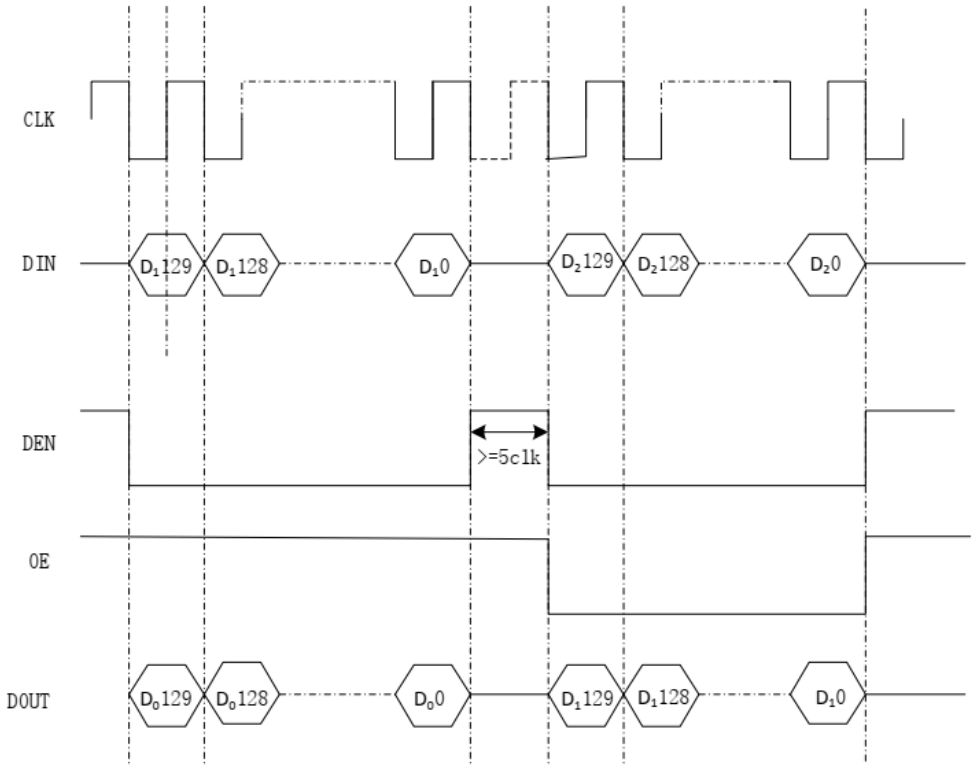

Figure 24. Serial Output Timing

When continuous input is performed, pull OE low, and DOUT will output the 130-bit data of the last input in sequence, which can be used in chip cascading scenarios.

X. Application Circuit

The chip is packaged in a plastic QFN package with 76 pins and a chip size of 9×9mm. COM is the common input terminal, RF1, RF2, RF3 and RF4 are four-channel input and output terminals, and the common port and the RF input and output ports need to be connected by a 50- ohm transmission line, and no off-chip DC blocking capacitor is required.

The power supply voltage of this chip is 3.3V. When used, place a 0.1uF chip capacitor to ground near the chip VDD33 pin. In addition, this four-channel chip requires at least 100uF tantalum capacitor filtering to reduce the fluctuation of the chip power supply voltage during pulse switching. DIN, DOUT, OE, CLK, DEN, FIN, FEN, SET, TR1, TR2, EN are wave control input and output ports. When the chip is working, the power supply port VDD33 must be powered on first, and then the wave control I/O port control signal must be given.

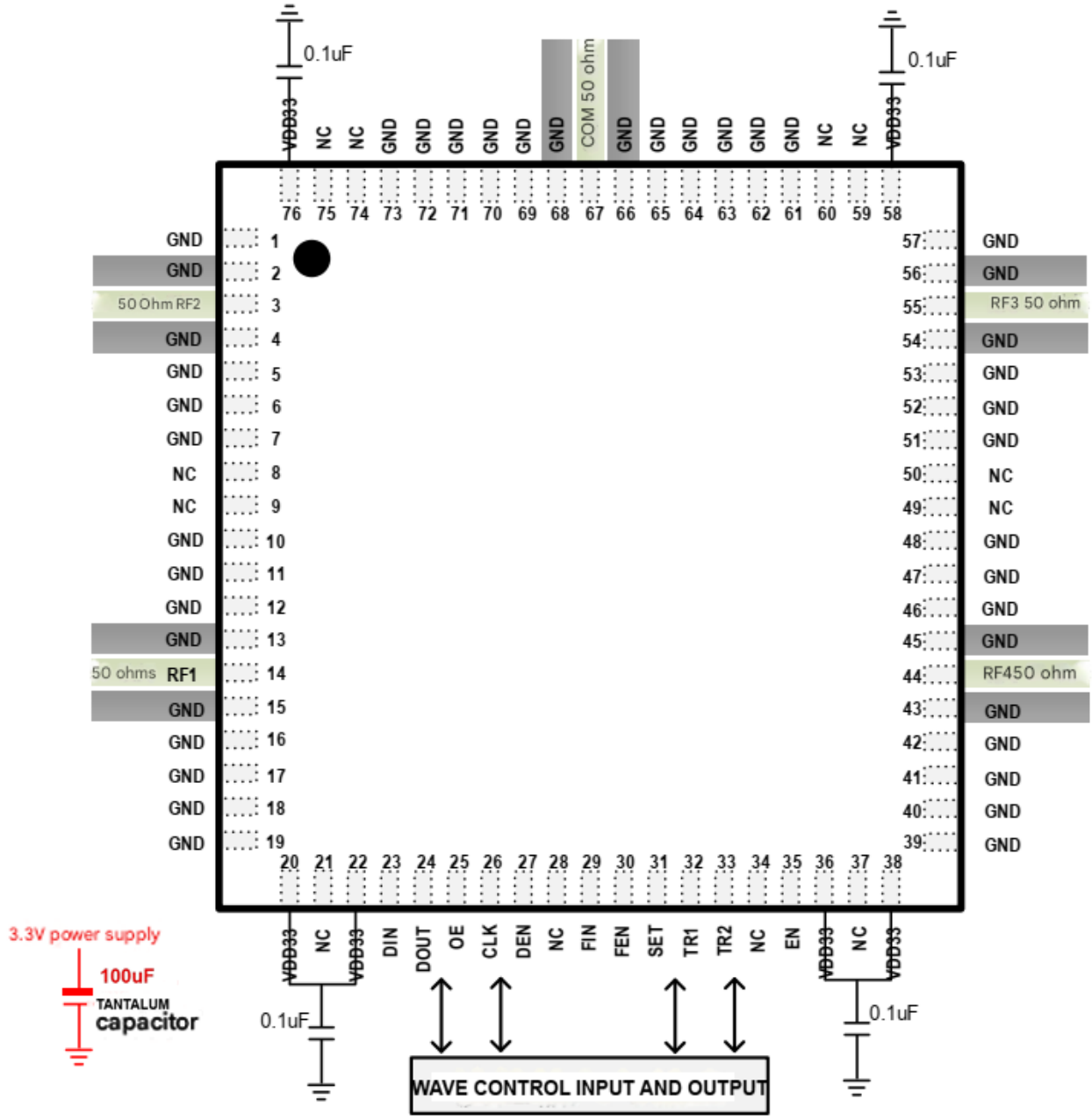

Figure 25

XI. Application Information

BSTCC35-1518 is a Ku-band highly integrated four-channel multifunctional chip. The chip integrates low noise amplifier, power amplifier, switch, 6 -digital controlled attenuator, 6 -digital controlled phase shifter, power divider, beam control and other modules. The attenuation and phase shift of the received and transmitted signals are realized by encoding the attenuation and phase shift inside the chip. The chip has high sensitivity and high attenuation and phase

shift accuracy, which can meet the application requirements of current military and civilian radar systems.

XII. Packaging Solutions

The chip is packaged in QFN76 pins with a size of 9mm×9mm. The detailed size information is shown in the figure below. The metal on the back of the chip after packaging is the ground terminal of the DC and AC signals of the entire chip and the main heat dissipation output terminal of the chip. When used, it needs to have a sufficient and ideal connection with the ground plane on the board and sufficient and good heat dissipation.

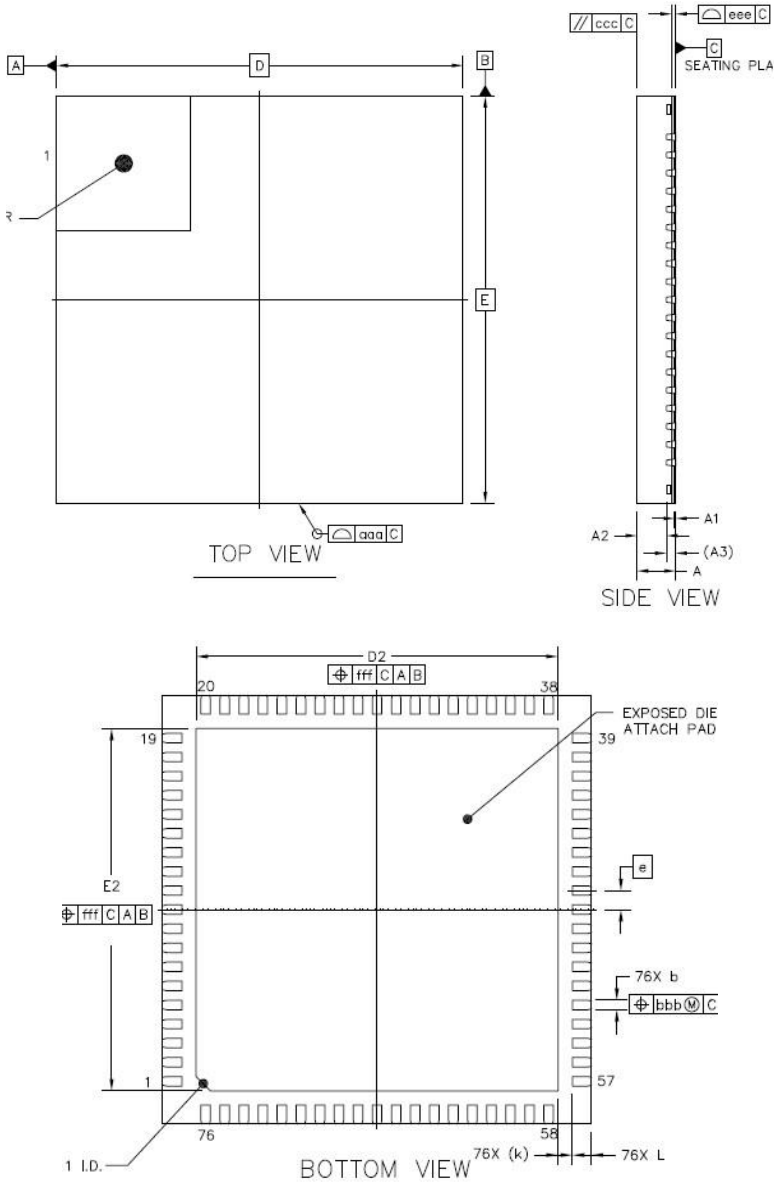

Figure 26. Package front view, side view, bottom view

12.1. Package size table

DIMENSION SYMBOLS	VALUE (MM)		
	Minimum	Nominal	maximum
A	0.8	0.85	0.9
A1	0	0.02	0.05
A2	—	0.65	—
A3		0.203 REF	
b	0.15	0.20	0.25
D		9 BSC	
E		9 BSC	
e		0.4 BSC	
D2	7.5	7.6	7.7
E2	7.5	7.6	7.7
L	0.3	0.4	0.5
K		0.3 REF	
aaa		0.1	
ccc		0.1	
eee		0.08	
bbb		0.07	
fff		0.1	