BSTCC33-0713S

7–13GHz Quad-Channel Multifunction Chip

Data Sheet

I. Product Introduction

BSTCC33-0713S is a broadband four-channel multi-function chip with an operating frequency range of 7GHz - 13GHz, low noise integrated into the chip amplifier, power amplifier, transmit and receive switch, 6-digital controlled attenuator, 6-digital controlled phase shifter, power splitter, beam steering, low Noise amplifier power supply modulation, on-chip ADC and other modules can provide maximum 31.5dB attenuation range, stepped 0.5dB, and 360° movement phase range, step 5.6°.

II. Application Areas

- Radar
- Communication System

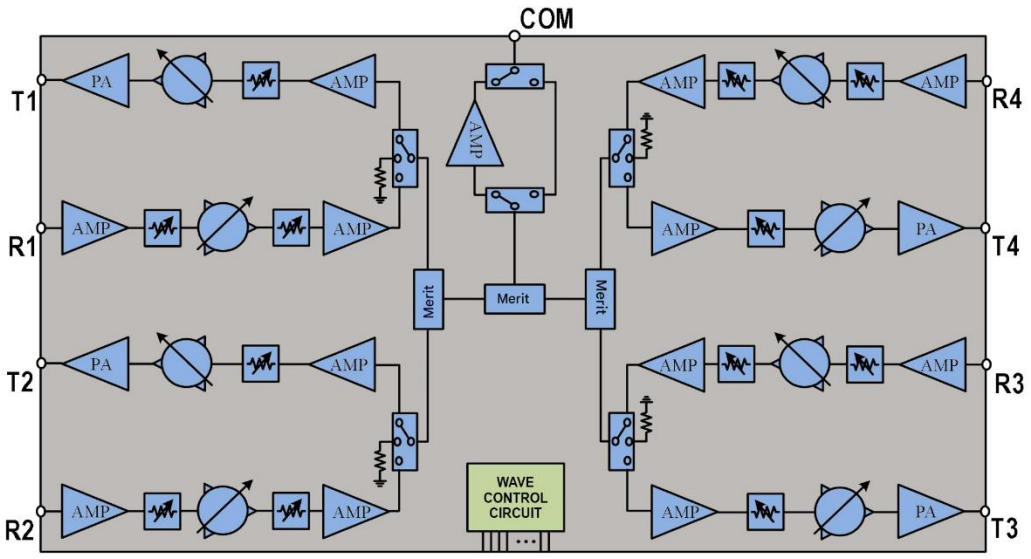

Figure 1. BSTCC33-0713S module schematic

III. Key technical indicators

- Operating power supply voltage: 3.3V

- Operating frequency: 7 GHz to 13 GHz
- 6-bit attenuation control bit, 0.5dB step ;
- 6 phase shifts, 5.6° steps
- Receive gain: 5dB (Rn port to COM port) n Transmit gain: 5dB (COM port to Tn port)
- Gain flatness in receiving band: 2dB
- Port standing wave ratio VSWR: 2
- Receive noise figure NF: 15dB
- Receive input Pin-1dB: -1dBm
- Transmitter output Po-1dB: 15dBm
- Transmitter Psat: 13.5dBm
- RMS phase shift error: < 3
- Amplitude consistency during phase shift: <±0.8dB
- Attenuation accuracy: < 0.2+5%Ai
- RMS attenuation error: < 1dB
- Attenuation additional phase shift: < ±8°
- Transmit and receive switching time: < 100ns
- Single channel operating current: 75mA/70mA @ receive / static transmit
- Bare core size: 5.06mm×6.36mm
- Process: SiGe BiCMOS

Table 1. Basic electrical properties

PARAMETER	CONDITION	MINIMUM	TYPICAL VALUES	MAXIMUM	UNIT
Frequency range		7		13	GHz
Receive linear gain	Rn port to COM port		5		dB
Transmit linear gain	COM port to TN port		5		dB
In-band gain flatness			2		dB
Port VSWR			2		-
Receive noise figure			15		dB
Receive input P-1dB			-1		dBm
Transmitter output P-1dB			15		dBm
Transmit output Psat			16		dBm
RMS phase error				3	Deg
Phase shift amplitude consistency		-0.8		0.8	dB
RMS attenuation error			-	1	dB

PARAMETER	CONDITION	MINIMUM	TYPICAL VALUES	MAXIMUM	UNIT
Attenuation of additional phase shift		-8		8	Deg
Transmitting and receiving switching time				100	ns
Single channel receiving current			75		mA
Single channel static emission current			70		mA
Single channel Po-1dB emission current			140		mA
Single channel load current			10		mA

Table 2. Digital port electrical parameters

PARAMETER	SYMBOL	CONDITION	MINIMUM	MAXIMUM	UNIT
Input high level voltage	V_{IH}	V_{CC} = 2.7 V to 3.6 V,	1.7		V
Input low level voltage	V_{IL}	V_{CC} = 2.7 V to 3.6 V,		0.8	V
Input high level current	I_{IH}	V_{CC} = 2.7 V to 3.6 V,	-500	500	uA
Input low level current	I_{IL}	V_{CC} = 2.7 V to 3.6 V,	-500	500	uA
Output high level voltage	V_{OH}	V_{CC} = 2.7 V to 3.6 V, I_{OH} = –100 uA	VCC - 0.2	VCC	V
Output high level voltage	V_{OH}	V_{CC} = 2.7 V I_{OH} = –4mA	2.4	VCC	V
Output low level voltage	V_{OL}	V_{CC} = 2.7 V to 3.6 V, I_{OL}= 100 uA	0	0.2	V
Output low level voltage	V_{OL}	V_{CC} = 2.7 V, I_{OL} = 4 mA	0	0.4	V

IV. Absolute Maximum Ratings

Table 3.

PARAMETER	VALUE
Maximum power supply voltage	3.6V
Maximum RF input power	TBD
Storage temperature	-65~150 ℃
Operating temperature	-55~125 ℃

*Note: For the maximum limit values listed above, if the device is operated in an environment exceeding these limits, it is likely to cause permanent damage to the device.

In actual application, it is best not to operate the device in an environment where the limit value or the value exceeds this limit value.

V. ESD protection

The BSTCC33-0713S has an ESD protection rating (Human Body Model) of at least Class 1B: ≥500V, <1000V. When handling the device, take appropriate ESD protection measures to avoid performance degradation or functional failure.

VI. Pin configuration

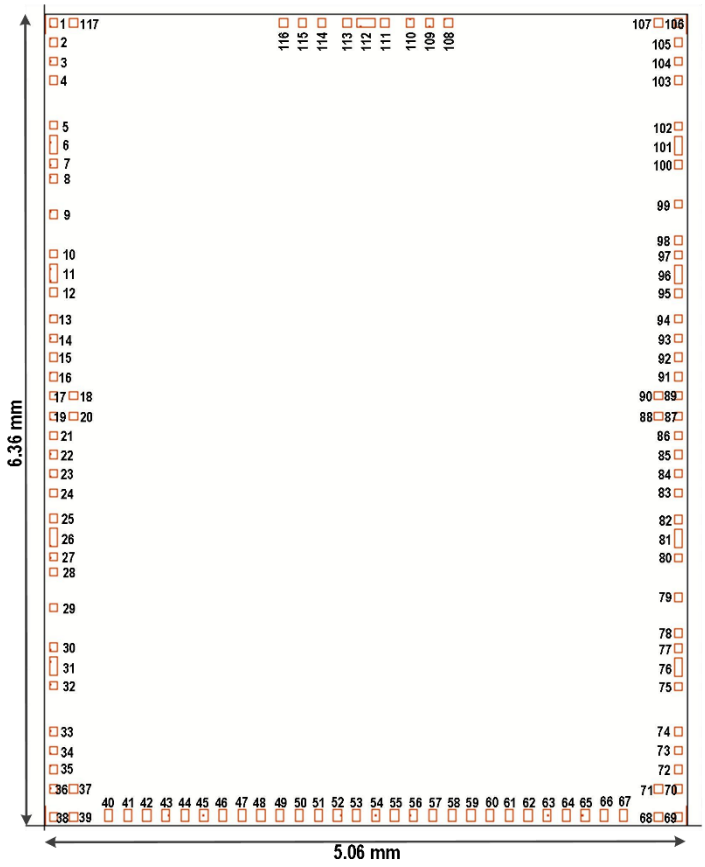

Figure 2.

VII. Chip pad layout

Table 4. Chip pad function information

SERIAL NUMBER	NAME	X COORDINATE IN UM	Y COORDINATE UM	PAD SIZE UM×UM	FUNCTION
1	VDD33		6288.76	70*70	Channel 1 power supply, 3.3V
2	AC1<3>		6138.76	70*70	Gain adjustment, the default is floating, when grounded, the gain of channel 1 is increased by 1dB
3	AC1<2>	71.24	5988.76	70*70	Gain adjustment, the default is floating, when grounded, the gain of channel 1 is reduced by 1dB
4	AC1<1>	71.24	5838.76	70*70	Gain adjustment, the default is floating, when grounded, the gain of channel 1 is reduced by 0.5dB

SERIAL NUMBER	NAME	X COORDINATE IN UM	Y COORDINATE UM	PAD SIZE UM×UM	FUNCTION
5	GND	71.24	5488.76	70*70	Ground
6	T1	71.24	5338.76	70*150	Channel 1 transmit output
7	GND	71.24	5188.76	70*70	Ground
8	NC	71.24	5071.24	70*70	Dangling
9	VD1_RX	71.24	4788.88	70*70	Channel 1 low noise amplifier power modulation output, driving capability > 50mA, subject to the Channel 1 ’ s wave control output RX control. When RX is high, VD1_RX outputs high level (VDD33); when RX is low, VD1_RX outputs 0
10	GND	71.24	4480	70*70	Ground
11	R1	71.24	4330	70*150	Channel 1 receives input
12	GND	71.24	4180	70*70	Ground
13	RX_1	71.24	3971.24	70*70	Channel 1 RX control output
14	TXD_1	71.24	3821.24	70*70	Channel 1 TXD control output
15	TX1_1	71.24	3671.24	70*70	Channel 1 TX1 control output
16	TX0_1	71.24	3521.24	70*70	Channel 1 TX0 control output
17	VDD33	71.24	3371.24	70*70	Channel 1 power supply, 3.3V
18	VDD33	231.24	3371.24	70*70	Channel 1 power supply, 3.3V
19	VDD33	71.24	3208.76	70*70	Channel 2 power supply, 3.3V
20	VDD33	231.24	3208.76	70*70	Channel 2 power supply, 3.3V
21	TX0_2	71.24	3058.76	70*70	Channel 2 TX0 control output
22	TX1_2	71.24	2908.76	70*70	Channel 2 TX1 control output
23	TXD_2	71.24	2758.76	70*70	Channel 2 TXD control output
24	RX_2	71.24	2608.76	70*70	Channel 2 RX control output
25	GND	71.24	2408.76	70*70	Ground
26	T2	71.24	2258.76	70*150	Channel 2 transmit output
27	GND	71.24	2108.76	70*70	Ground
28	NC	71.24	1991.24	70*70	Dangling
29	VD2_RX	71.24	1708.88	70*70	Channel 2 low noise amplifier power modulation output, driving capability > 50mA, subject to the Channel 2 wave control output RX control. When RX is high, VD2_RX outputs high level (VDD33); when RX is low, VD2_RX outputs 0
30	GND	71.24	1400	70*70	Ground
31	R2	71.24	1250	70*150	Channel 2 receives input
32	GND	71.24	1100	70*70	Ground
33	AC2<1>	71.24	741.24	70*70	Gain adjustment, the default is floating, when grounded, the gain of channel 2 is reduced by 0.5dB
34	AC2<2>	71.24	591.24	70*70	Gain adjustment, the default is floating, when grounded, the gain of channel 2 is reduced by 1dB
35	AC2<3>	71.24	441.24	70*70	Gain adjustment, the default is floating, when grounded, the gain of channel 2 is increased by 1dB

SERIAL NUMBER	NAME	X COORDINATE IN UM	Y COORDINATE UM	PAD SIZE UM×UM	FUNCTION
36	VDD33	71.24	291.24	70*70	Channel 2 power supply, 3.3V
37	VDD33	231.24	291.24	70*70	Channel 2 power supply, 3.3V
38	VDD33	71.24	71.24	70*70	Channel 2 power supply, 3.3V
39	VDD33	231.24	71.24	70*70	Channel 2 power supply, 3.3V
40	EN	505	80.51	68*101	Input, wave control enable, weak pull-down, wave control is valid when low
41	TR1	655	80.51	68*101	Input, wave control input control signal, weak pull-down, generate receiving control signal
42	TR2	805	80.51	68*101	Input, wave control input control signal, weak pull-down, generate pulse emission control signal
43	DIN	955	80.51	68*101	Serial signal input, weak pull-up
44	DEN	1105	80.51	68*101	Input, serial data enable, weak pull-up, input valid when low
45	CLK	1255	80.51	68*101	Clock input, weak pull-down, recommended 1~20MHz
46	VDD33	1405	80.51	68*101	3.3V power supply for wave control circuit
47	VDD12	1555	80.51	68*101	The wave control circuit has an internal 1.2V power supply. It is recommended to connect an external 0.1uF voltage stabilizing capacitor to prevent electromagnetic interference.
48	OE	1705	80.51	68*101	Input, wave control output enable, weak pull-down, output valid when low
49	DOUT	1855	80.51	68*101	Serial data output, weak pull-up
50	FIN	2005	80.51	68*101	Function register serial input, weak pull-up
51	FEN	2155	80.51	68*101	Input, function register enable, weak pull-up, FIN input valid when low
52	CLKSEL	2305	80.51	68*101	CLK clock when high, CLKAUX clock when low, connect to 3.3V power supply in normal application
53	CLKAUX	2455	80.51	68*101	Input, system auxiliary clock, weak pull-down, grounded when not in use
54	GND	2605	80.51	68*101	Digital ground
55	TR3	2755	80.51	68*101	Input, wave control input control signal, weak pull-down, generate continuous wave emission control signal, grounded when not in use
56	TR3_SEL	2905	80.51	68*101	Input, TR3 mode selection control, weak pull-up, when low, the internal tr3_in signal is input from port TR3, when high, the tr3_in signal is input from the internal register reg_fun2[1][7], connect to 3.3V power supply when not in use
57	EEEN	3055	80.51	68*101	Input, EEPROM/MTP serial data input enable, weak pull-up, connect to 3.3V power supply when not in use
58	EEIN	3205	80.51	68*101	Input, EEPROM/MTP serial data input, weak pull-down, grounded when not in use
59	CLK_EE	3355	80.51	68*101	Output, EEPROM/MTP system clock, left floating when not in use

SERIAL NUMBER	NAME	X COORDINATE IN UM	Y COORDINATE UM	PAD SIZE UM×UM	FUNCTION
60	VDD12	3505	80.51	68*101	The wave control circuit has an internal 1.2V power supply. It is recommended to connect an external 0.1uF voltage stabilizing capacitor to prevent electromagnetic interference.
61	VDD33	3655	80.51	68*101	3.3V power supply for wave control circuit
62	EEOUT	3805	80.51	68*101	Output, EEPROM/MTP serial output, weak pull-up, floating when not in use
63	BUSY_IN	3955	80.51	68*101	Input, EEPROM/MTP write operation flag, weak pull-down, grounded when not in use
64	EEOE	4105	80.51	68*101	Output, EEPROM/MTP serial output enable, floating when not in use
65	RD_UPDATE	4255	80.51	68*101	Output, EEPROM/MTP read enable, floating when not in use
66	WR_EE	4405	80.51	68*101	Output, write EEPROM enable, floating when not in use
67	WR_MTP	4555	80.51	68*101	Output, write MTP enable, floating when not in use
68	VDD33	4828.76	71.24	70*70	Channel 3 power supply, 3.3V
69	VDD33	4988.76	71.24	70*70	Channel 3 power supply, 3.3V
70	VDD33	4988.76	291.24	70*70	Channel 3 power supply, 3.3V
71	VDD33	4828.76	291.24	70*70	Channel 3 power supply, 3.3V
72	AC3<3>	4988.76	441.24	70*70	Gain adjustment, the default is floating, when grounded, the gain of channel 3 is increased by 1dB
73	AC3<2>	4988.76	591.24	70*70	Gain adjustment, the default is floating, when grounded, the gain of channel 3 is reduced by 1dB
74	AC3<1>	4988.76	741.24	70*70	Gain adjustment, the default is floating, when grounded, the gain of channel 3 is reduced by 0.5dB
75	GND	4988.76	1091.24	70*70	Ground
76	T3	4988.76	1241.24	70*150	Channel 3 transmit output
77	GND	4988.76	1391.24	70*70	Ground
78	NC	4988.76	1508.76	70*70	Dangling
79	VD3_RX	4988.76	1791.12	70*70	Channel 3 low noise amplifier power modulation output, driving capability > 50mA, controlled by channel 3 wave control output RX. When RX is high, VD3_RX output
					High level (VDD33); when RX is low, VD3_RX outputs 0
80	GND	4988.76	2100	70*70	Ground
81	R3	4988.76	2250	70*150	Channel 3 receives input
82	GND	4988.76	2400	70*70	Ground
83	RX_3	4988.76	2608.76	70*70	Channel 3 RX control output
84	TXD_3	4988.76	2758.76	70*70	Channel 3 TXD control output
85	TX1_3	4988.76	2908.76	70*70	Channel 3 TX1 control output
86	TX0_3	4988.76	3058.76	70*70	Channel 3 TX0 control output

SERIAL NUMBER	NAME	X COORDINATE IN UM	Y COORDINATE UM	PAD SIZE UM×UM	FUNCTION
87	VDD33	4988.76	3208.76	70*70	Channel 3 power supply, 3.3V
88	VDD33	4828.76	3208.76	70*70	Channel 3 power supply, 3.3V
89	VDD33	4988.76	3371.24	70*70	Channel 4 power supply, 3.3V
90	VDD33	4828.76	3371.24	70*70	Channel 4 power supply, 3.3V
91	TX0_4	4988.76	3521.24	70*70	Channel 4 TX0 control output
92	TX1_4	4988.76	3671.24	70*70	Channel 4 TX1 control output
93	TXD_4	4988.76	3821.24	70*70	Channel 4 TXD control output
94	RX_4	4988.76	3971.24	70*70	Channel 4 RX control output
95	GND	4988.76	4171.24	70*70	Ground
96	T4	4988.76	4321.24	70*150	Channel 4 transmit output
97	GND	4988.76	4471.24	70*70	Ground
98	NC	4988.76	4588.76	70*70	Dangling
99	VD4_RX	4988.76	4871.12	70*70	Channel 4 low noise amplifier power modulation output, driving capability > 50mA, Channel 4 ’ s wave control output RX control. When RX is high, VD4_RX outputs high level (VDD33); when RX is low, VD4_RX outputs 0
100	GND	4988.76	5180	70*70	Ground
101	R4	4988.76	5330	70*150	Channel 4 receives input
102	GND	4988.76	5480	70*70	Ground
103	AC4<1>	4988.76	5838.76	70*70	Gain adjustment, the default is floating, when grounded, the gain of channel 4 is reduced by 0.5dB
104	AC4<2>	4988.76	5988.76	70*70	Gain adjustment, the default is floating, when grounded, the gain of channel 4 is reduced by 1dB
105	AC4<3>	4988.76	6138.76	70*70	Gain adjustment, the default is floating, when grounded, the gain of channel 4 is increased by 1dB
106	VDD33	4988.76	6288.76	70*70	Channel 4 power supply, 3.3V
107	VDD33	4828.76	6288.76	70*70	Channel 4 power supply, 3.3V
108	ADC_IN<4>	3178.76	6288.76	70*70	Input, internal ADC analog input signal 4 ports
109	ADC_IN<3>	3028.76	6288.76	70*70	Input, internal ADC analog input signal 3 ports
110	ADC_IN<2>	2878.76	6288.76	70*70	Input, internal ADC analog input signal 2 port
111	GND	2680	6288.76	70*70	land
112	COM	2530	6288.76	150*70	RF common terminal
113	GND	2380	6288.76	70*70	land
114	ADC_IN<1	2181.24	6288.76	70*70	Input, internal ADC analog input signal 1 port
115	RXMOD_SEL	2031.24	6288.76	70*70	The default setting is floating. When grounded, the four transmitting channels of the chip are turned off and the chip enters the four-channel pure receiving mode.
116	NC	1881.24	6288.76	70*70	Dangling
117	VDD33	231.24	6288.76	70*70	Channel 1 power supply, 3.3V

VIII. Typical curves

Unless otherwise specified, the test conditions are 3.3V power supply, room temperature, and phase shift attenuation ground state. All test curves are the test results of the chip on the evaluation board.

The gain in the attenuation and phase shift curves does not deduct the board losses.

8.1. Small signal S parameters

Figure 3. Receive gain (Rn to COM, other channels loaded)

Figure 4. Transmit gain (COM to Tn, other channels loaded)

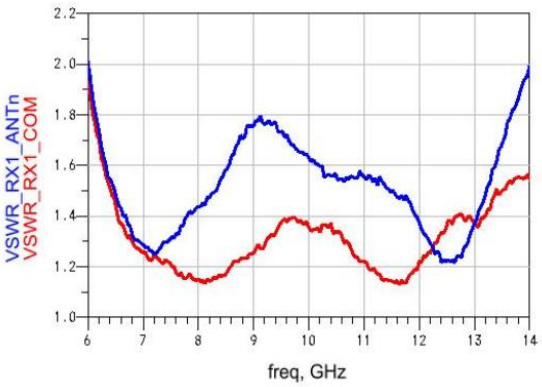

Figure 5. Receive port return loss

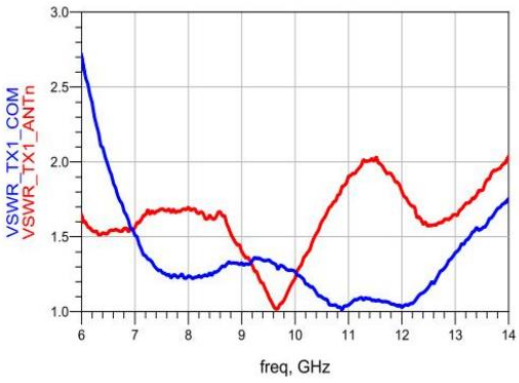

Figure 6. Transmit port return loss

8.2. Receive attenuation performance

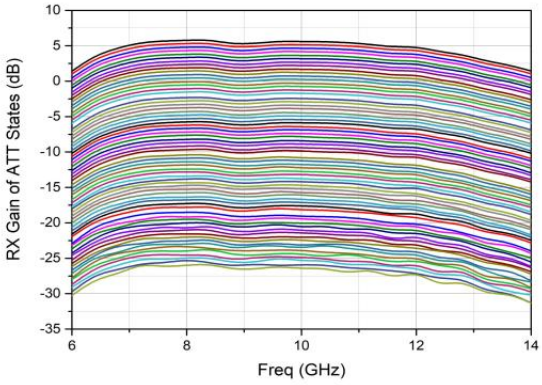

Figure 7. Receive gain 64-state attenuation curve vs. frequency

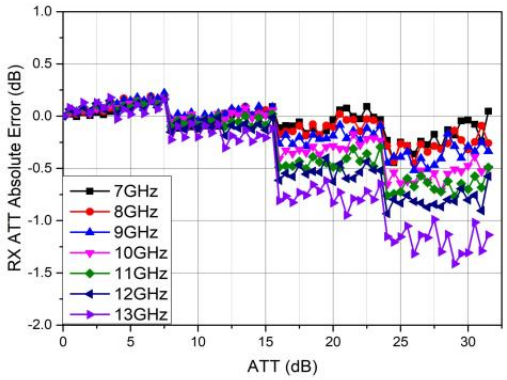

Figure 8. Receive mode attenuation error vs attenuation value

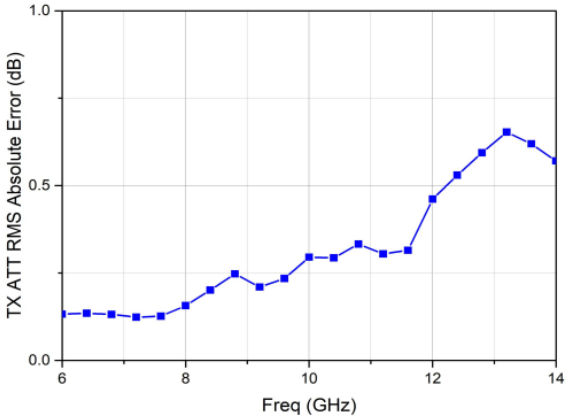

Figure 9. Receive Mode RMS Attenuation Error vs Frequency

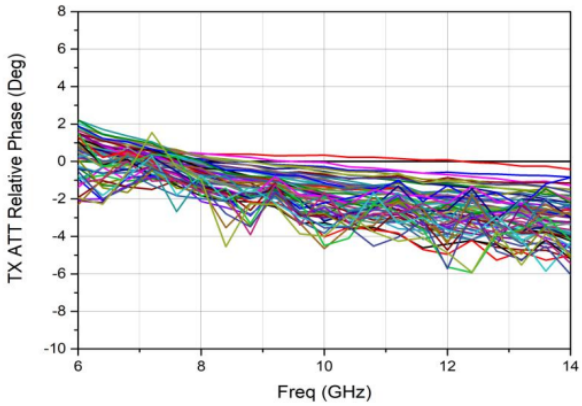

Figure 10. Receive Mode 64-State Attenuation Additive Phase Shift vs. Frequency

8.3. Receive phase shift performance

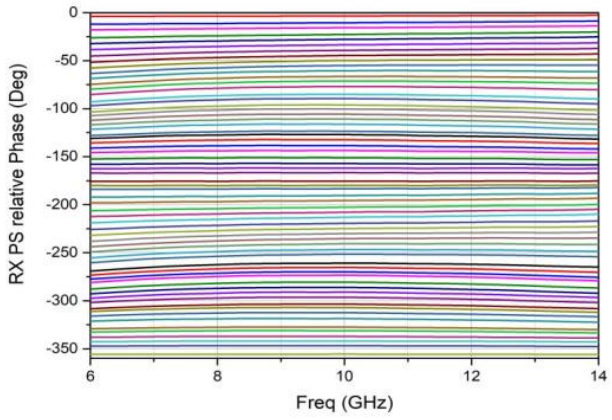

Figure 11. Receiving mode 64-state relative phase shift curve vs. frequency

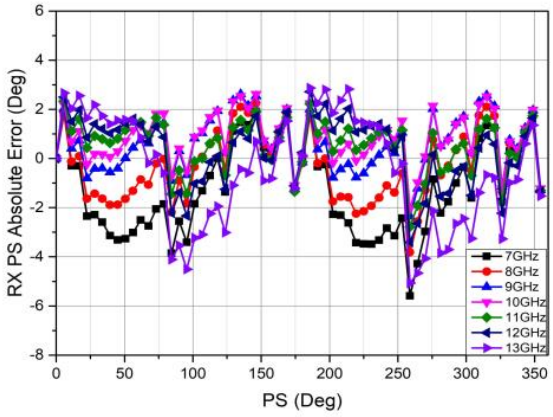

Figure 12. Receive mode phase shift error vs phase shift value

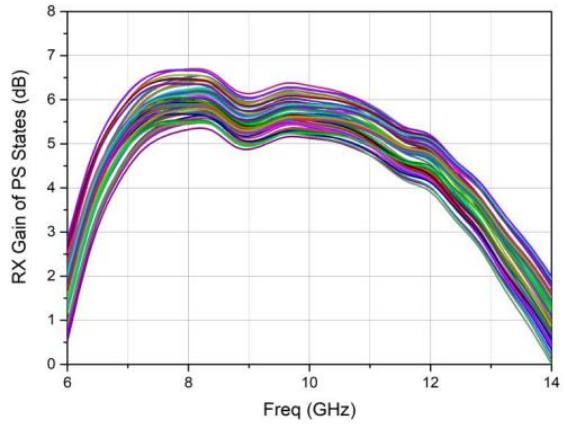

Figure 13. Gain curve vs. frequency in 64-state phase shift in receive mode

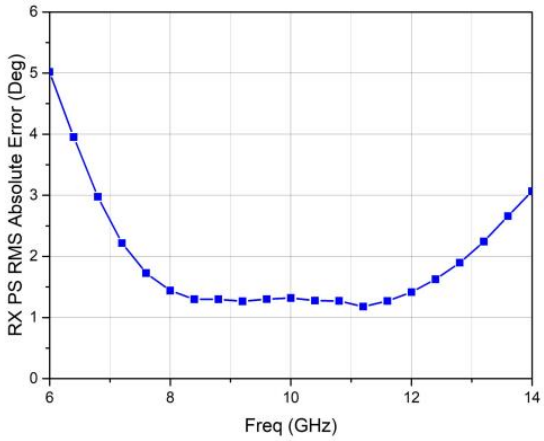

Figure 14. Receive Mode RMS Phase Error vs Frequency

8.4. Transmission attenuation performance

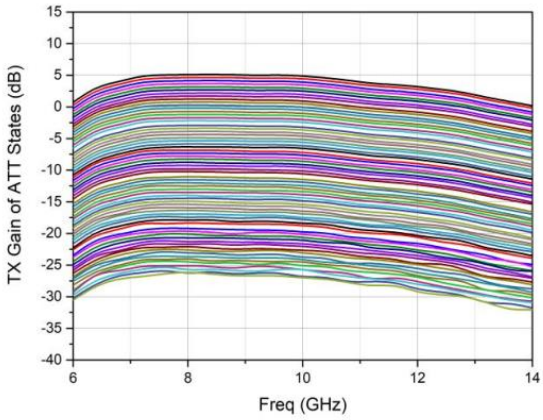

Figure 15. Transmitter gain 64-state attenuation curve vs. frequency

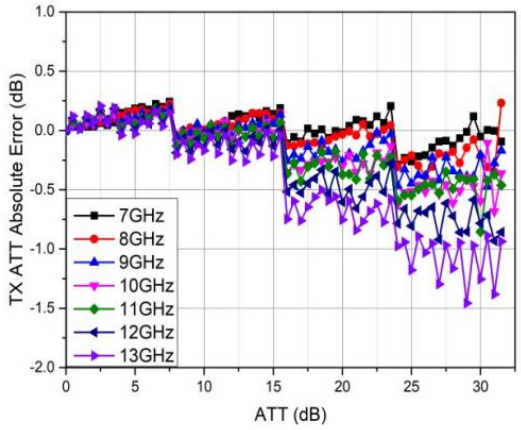

Figure 16. Transmit mode attenuation error vs attenuation value

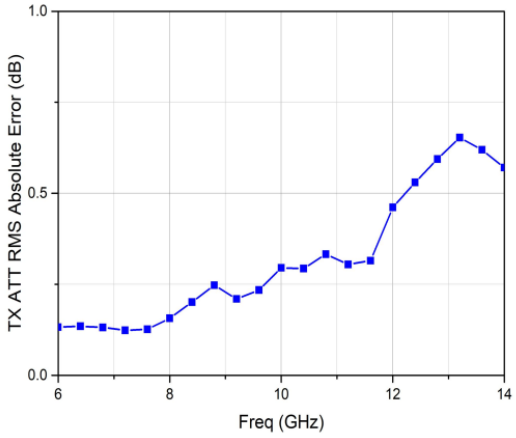

Figure 17. Transmit Mode RMS Attenuation Error vs. Frequency

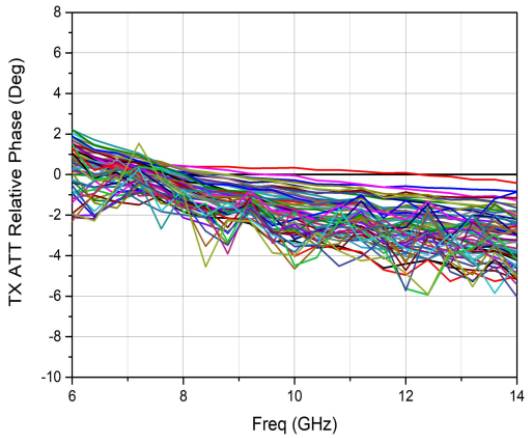

Figure 18. Additional phase shift vs. frequency when transmitting mode 64-state decays

8.5. Transmit phase shift performance

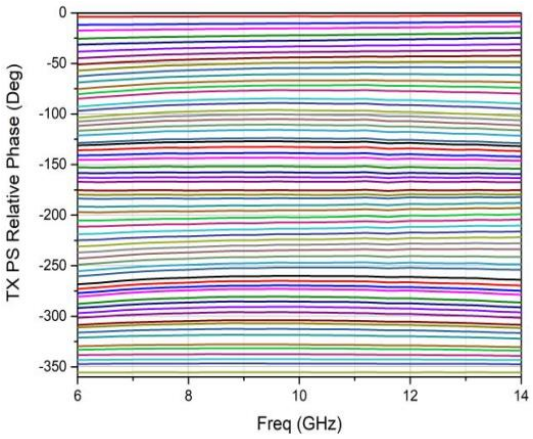

Figure 19. Transmit mode 64-state relative phase shift curve vs. frequency

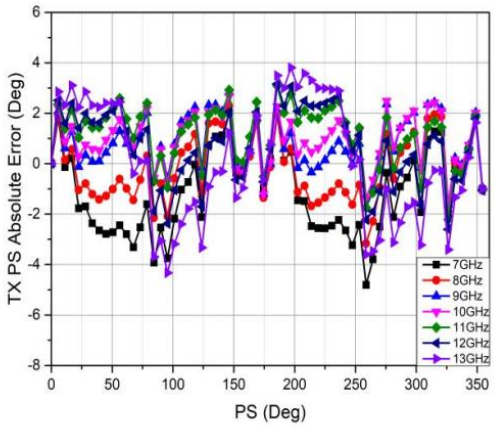

Figure 20. Transmit mode phase shift error vs phase shift value

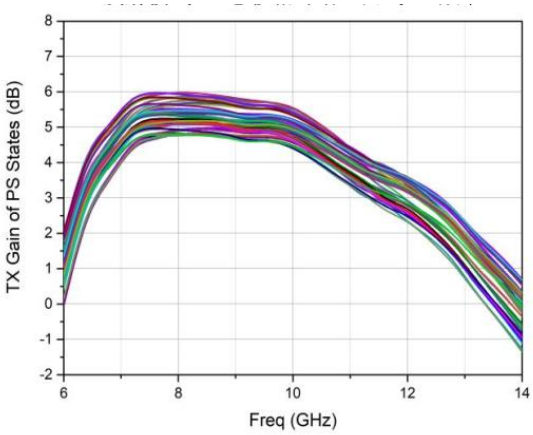

Figure 21. Gain curve vs. frequency in 64-state phase shift in transmit mode

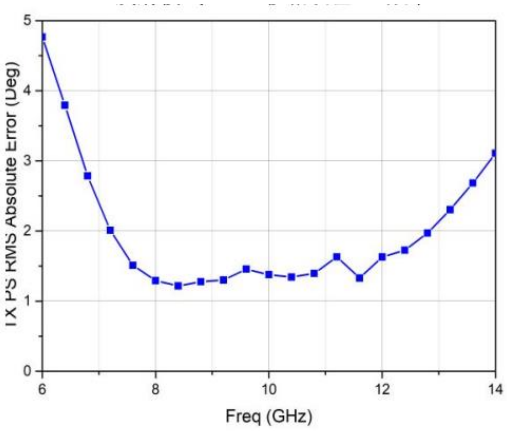

Figure 22. Transmit Mode RMS Phase Error vs Frequency

8.6. Noise and power performance

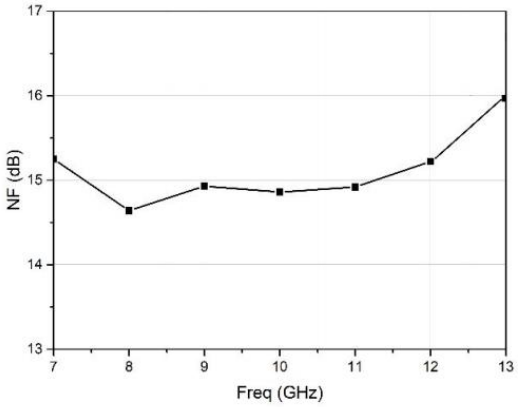

Figure 23. Receive Noise Figure vs. Frequency

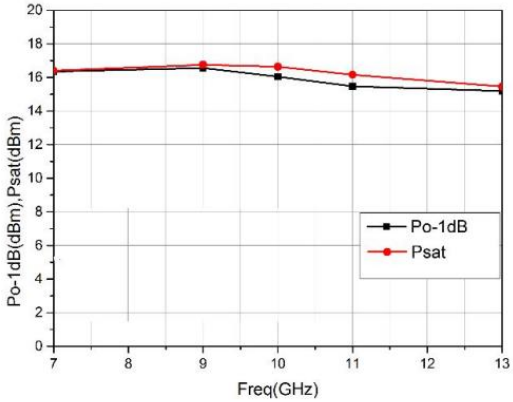

Figure 24. Transmit output 1dB power vs frequency

IX. Digital wave control function

The digital part mainly includes 5 identical control channels and a common logic. The 5 control channels include reg_data1 module, reg_data2 module.

The common logic includes reg_fun1 module, reg_fun2 module, pulse protection module and temperature protection module.

9.1. Serial data register reg_data1

Serial data input: DEN is low, CLK rises, and data is written from the DIN port to the first group of registers reg_data1[0] in sequence; the original data in reg_data1 is moved from reg_data1[0] to reg_data1[25] in sequence.

Serial data output: Single-channel serial data output dout takes reg_data1[25] as output.

Serial self-test data loading: When DEN is detected high on the rising edge of CLK, the self-test data specified by reg_fun2[2][7:0] is written to the serial register reg_data1.

9.2. Serial data register reg_data2

Data selection input: On the first CLK rising edge after the den rising edge, reg_data1 is written to the secondary data register reg_data2 selected by the function register reg_fun2 [0] [4:0]. The 32 groups of data in the secondary data register reg_data2 are defined as shown in Table 5.

Data selection output: A set of reg_data2[n][25:0] outputs selected by reg_fun2[1][4:0] is used for phase attenuation and control.

Table 5. Secondary data register data definition

DATA DEFINITION IN REG_DATA2[N][25:0]																								
D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
AT5	AT4	AT3	AT2	AT1	AT0	MCT	MCR	AR5	AR4	AR3	AR2	AR1	AR0	PT5	PT4	PT3	PT2	PT1	PT0	PR5	PR4	PR3	PR2	PR1	PR0

9.3. Serial data register reg_data3

DEN is low and the DIN serial input {5{26'h15D5A5A}} is internally unlocked.

On the second CLK rising edge after the FEN rising edge, when reg_fun1[11:8]=4'h1, the data dat_seled in the corresponding address of the reg_data2 array specified by reg_fun1[7:0] is written to the reg_data3 register; otherwise, the reg_data3 register remains unchanged.

Every time reg_data3 is updated, reg_fun1 must be written once. If reg_fun1 is not written, no update will occur.

9.4. PH and ATT function control output

Table 6. Phase shift and attenuation function control output logic

INPUT	CHANNEL 1 TO CHANNEL 5 OUTPUT		STATE
TR1	PH[5:0]	ATT[5:0]	
1	PT[5:0]	AT[5:0]	Emitting state
0	PR[5:0]	AR[5:0]	Receiving state

9.5. Switch control output

The switch control logic is listed in Table 7, where the input signal tr3_in is taken from the TR3 selection module, PTR2 is taken from the pulse width protection module, MCT, MCR is taken from reg_data3, and ot_flag is the output signal of the internal temperature protection module.

Table 7. Channel 1~4 switch control output logic

ENTER							OUTPUT				CORRESPONDING CHANNEL STATUS
EN	ot_flag	TR1	PTR2	tr3_in	MCT	MCR	RX	TX0	TX1	TXD	
0	0	0	0	0	x	0	1	0	0	0	Receiving state
0	0	1	0	0	x	0	0	0	0	0	Transition state
0	0	1	1	0	0	x	0	1	0	1	Pulsed emission state
0	0	1	0	1	0	x	0	0	1	1	Continuous wave emission state
Other combinations							0	0	0	0	Load state

9.6. Function register reg_fun1

Serial data input: FEN is low, CLK rises, data is written into reg_fun1[0] from FIN port, and the original data in reg_fun1 is written into reg_fun1[1] from FIN port.

reg_fun1[0] moves to reg_fun1[11]. When FEN is high, the data transmission is completed. At this time, reg_fun1[11:8] is selected as the address of the secondary function register, and reg_fun1[7:0] is selected as the input data of the secondary function register.

9.7. Function register reg_fun2

According to the address determined by reg_fun1[11:8], on the first CLK rising edge after the rising edge of FEN, write the data of reg_fun1[7:0] into reg_fun2 register.

The function registers are described in Table 8. The high and low bits of the function register group bytes in the table are consistent with the high and low order of the internal function register bit definitions.

Table 8. Function register description

REG_FUN2 REGISTER NUMBER	REG_FUN 2 EGISTER DEFINITION	D7	D6	D5	D4	D3	D2	D1	D0	ILLUSTRATE	DEFAULT VALUE
reg_fun2 [0]	Second-level mail register reg_dat a2 write address				reg2_addr_w[4:				0]		8'h1f
reg_fun2 [1]	Second-level mail register reg_dat a2 output address	tr3en	Rsten 1: Enable		reg2_addr_r[4:0				]		8'h1f
reg_fun2 [2]	Self-test data loading selection address			bit_addr[7:0]							8'hff
reg_fun2 [3]	Control and protection function selection	bit_en	clkee_sel 0:1'b0 1:clk	chip0 0: ch5 1: ch4	pro_en[4:0]						8'h9f
reg_fun2 [4]	Accumulated number			pro_add[7:0]						Protection duty cycle $\frac{pro\_dec}{pro\_add + pro\_dec}$	8'h0 9
reg_fun2	Decrement number			pro_dec[7:0]							8'h0
[5]											1

REG_FUN2 REGISTER NUMBER	REG_FUN 2 EGISTER DEFINITION	D7	D6	D5	D4	D3	D2	D1	D0	ILLUSTRATE	DEFAULT VALUE
reg_fun2 [6]	Timing protection threshold	pro_threshold[7:0]								Protection pulse width *pro_threshold* $\frac{pro\_threshold}{pro\_add \times f_{clk}}$	8'h9 5
reg_fun2 [7]		pro_threshold[15:8]									8'h1 1
reg_fun2 [8]		pro_threshold[23:16]									8'h0 0
reg_fun2 [9]		pro_threshold[31:24]									8'h0 0
reg_fun2 [10]	AD sampling and over-temperature protection options	ad_en	ref_sel : default 1,5V Reference Level	temp _sel 1: Positive coefficient			ot_ pro _en		dlt_th[3:0]	ad_en:1 means AD work enable is valid, ot_pro_en:1 table Indicates that protection is enabled	8'hC 0
reg_fun2 [11]	Frequency setting	freq_addr[7:0]									8'h0 0
reg_fun2 [12]	Frequency setting and frequency compensation control parameters	freq_addr[9:8]		-			freq_sel[1:0]	cal _e n	wr_en =1:wri te =0:rea d	cal_en:0 means serial input and Perform calculations on EEPROM data, wr_en : 1 means write EEPROM Operation	8'h0 2
reg_fun2 [13]	Overtemperature threshold	ot_threshold[7:0]									8'h0 0
reg_fun2 [14]											8'h0 0
reg_fun2 [15]	AD register	ad_auto _en: =1: Automatic polling =0: Register configuration polling	When ad_ch_sel_ov ad_auto_en=1, the Value controls ADC conversion channel	clkadc_mux 00: /2 01: /4 10: /8 11: /16	ad_ov_num : 00: Read 1st indication position 01: Read Second indication position 10: Read 4 times indication position 11: Read 8 times indicator bit					test_sel=0,ad_a uto_en=1; test_sel=1,ad_a uto_en is configurable ; test_sel=0,ad_c h_sel_ov=0; test_sel=1,ad_c h_sel_ov configurable	8'h0f

X. Function register input timing

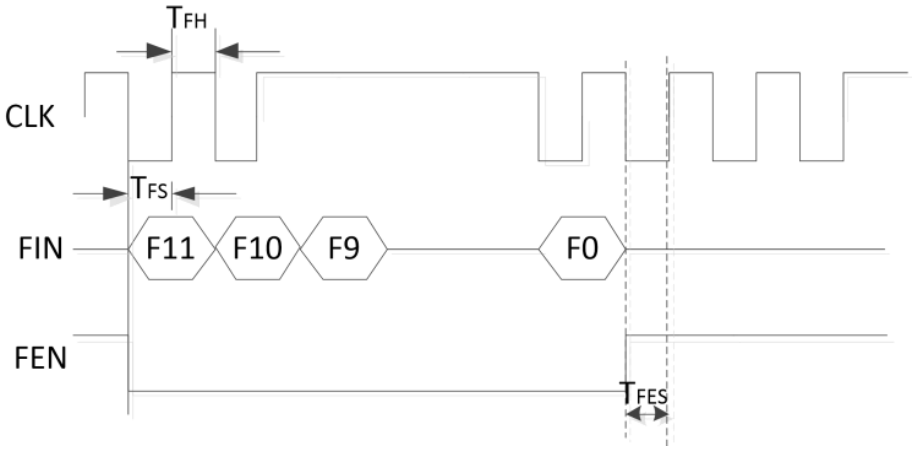

Figure 25. Function register input timing

FEN is low, FIN is sampled on the rising edge of the clock and serialized internally to reg_fun1[11:0]. Reg_fun1[7:0] is stored in the secondary function register reg_fun2 on the first rising edge of clk after the rising edge of FEN. The storage address is determined by reg_fun1[11:8].

10.1. Serial Data Register Input Timing

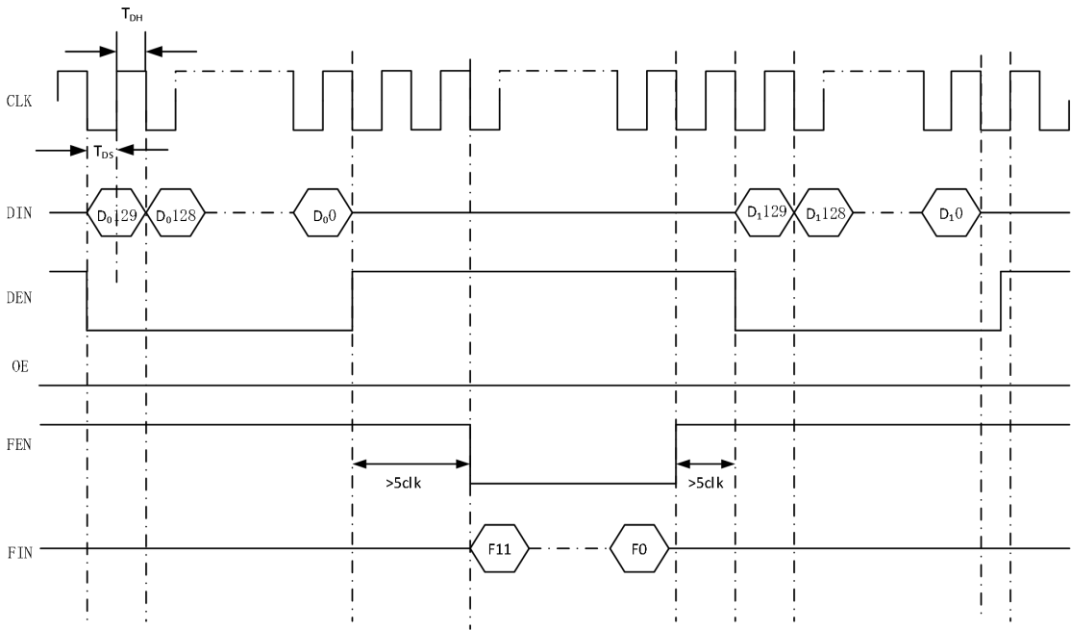

Figure 26. Function register input timing

10.2. Serial data input timing

Before performing the phase shift attenuation control operation, the command unlocking operation is performed first: DEN is low, and the DIN serial input {5{26'h15D5A5A}} is used for

internal unlocking. After the unlocking is completed, the phase shift attenuation and control code are input.

DEN is low, the rising edge of the clock samples DIN, which is internally serialized and transferred to reg_data1[25:0]. Reg_data1 is stored in the rising edge of DEN.

Secondary data storage area, the address is determined by the function register reg_fun2[0], the default is address 31. On the second CLK rising edge after the FEN rising edge, when reg_fun1[11:8] = 4'h1 and the internal unlock is on, the data in the corresponding address of the reg_data2 array specified by reg_fun1[7:0] is written to the reg_data3 register; otherwise, the reg_data3 register remains unchanged.

10.3. Serial Data Register Output Timing

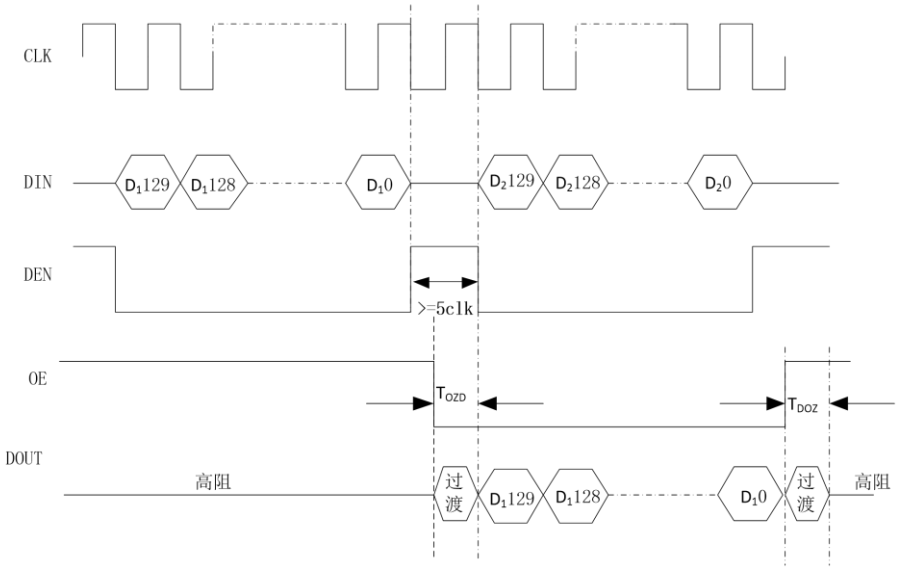

Figure 27. Serial data output timing

10.4. Serial data register input timing

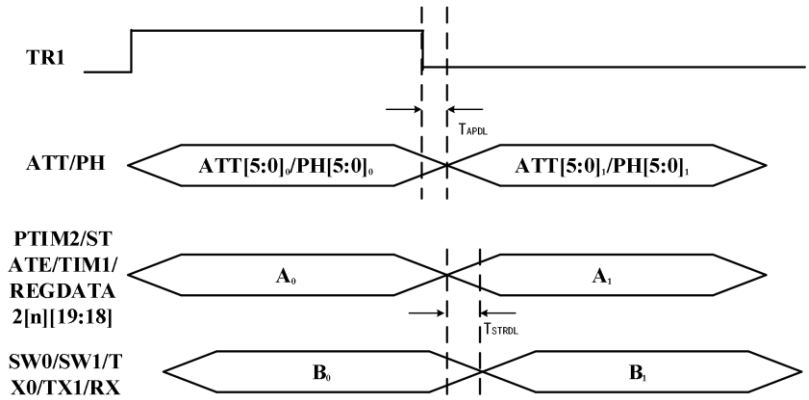

Figure 28. Discrete parallel port output timing

XI. Typical Application and Assembly Diagrams

The figure below shows the application circuit and assembly diagram of the BSTCC33-0713S chip.

The RF port and common port of each channel need to be bonded with two gold wires to the 50-ohm transmission line on the board. The length of the gold wire should be as short as possible. At the same time, the GND pads on both sides of the RF port should be downbonded to the ground on both sides of the signal to improve the RF performance and port isolation. The RF port does not require external DC isolation.

The power supply voltage of this chip is 3.3V. When using it, place a 0.1uF chip capacitor to ground near the power pad of the chip. As shown in the figure, the main circuit of the chip

VDD33 is powered from the middle of the left and right sides. The main circuit of the chip can also be powered by VDD33 at the four corners. If the chip can be powered from the middle of the left and right sides and the four corners

The effect will be better if VDD33 is powered at the same time.

In addition, this four-channel chip requires at least 100uF tantalum capacitor filtering to reduce the fluctuation of the chip end power supply voltage during pulse switching. When the chip is working, it is necessary to first power up the power port VDD33 and then give the control signal to the wave control I/O port.

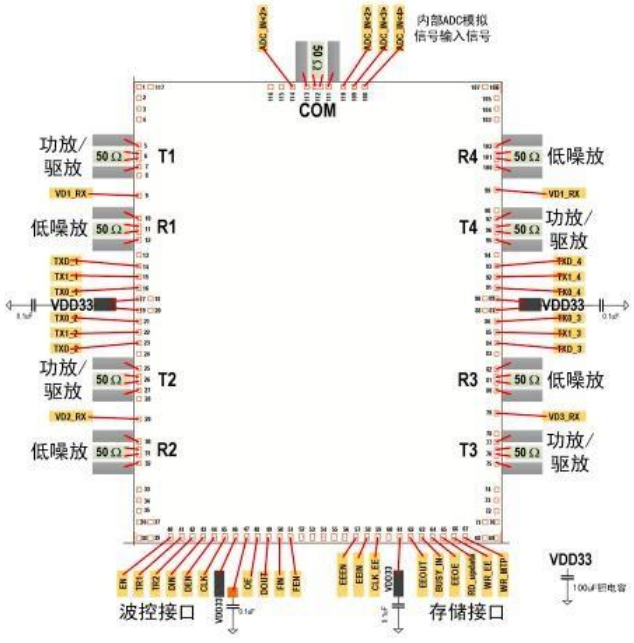

Figure 29. Typical application and assembly diagrams