BSTCC33-0713Q

7–13GHz Quad-Channel Multifunction Chip

Data Sheet

I. Product Introduction

BSTCC33-0713Q is a broadband four-channel multi-function chip.

The operating frequency range is 7GHz to 13GHz. The chip integrates low noise amplifier, power amplifier, transmit and receive switch, 6-digital controlled attenuator, 6-digital controlled phase shifter, power divider, beam control, low noise amplifier power modulation, on-chip ADC and other modules. It can provide a maximum attenuation range of 31.5dB, step 0.5dB, and a 360° phase shift range, step 5.6 °. The chip adopts plastic QFN package, with a total of 68 pins and a chip size of 8 × 8mm.

II. Application Areas

- Radar Communication
- Key technical indicators

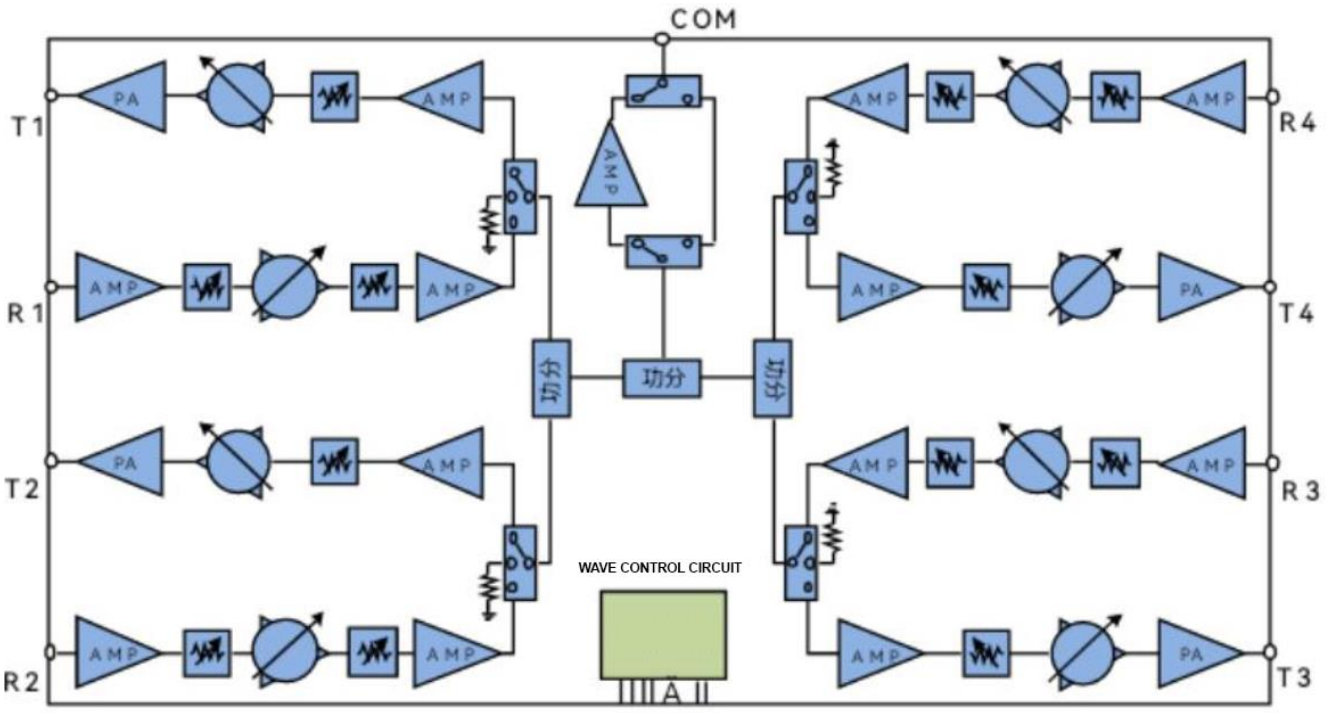

Figure 1. BSTCC33-0713Q module schematic

- Working power supply voltage: 3.3V
- Operating frequency: 7GHz~13GHz
- 6 -bit attenuation control, step 0.5dB
- 6 phase shift, step 5.6°
- Receive gain: 5dB (Rn port to COM port)
- Transmit gain: 5dB (COM port to Tn port)
- Gain flatness in receiving band: <3dB
- Port standing wave ratio VSWR: <2
- Receive noise factor NF: <16dB
- Receive input Pin-1dB: -1dBm
- Transmitter output Po-1dB: 15dBm
- RMS phase shift error: <3°
- Amplitude consistency during phase shift: <±0.8dB
- Attenuation accuracy: <0.2+5%Ai
- RMS attenuation error: <0.7dB
- Attenuation additional phase shift: <±8°
- Transmit/receive switching time: <100ns
- Single channel operating current: 70mA/70(140)mA
  @ receiving / static (Po-1dB, 16dBm) Transmitter
- Package and size: QFN 8mm×8mm
- Process: SiGe BiCMOS

III. Electrical Characteristics

Table 1. Basic electrical properties

PARAMETER	CONDITION	MINIMUM	TYPICAL VALUE	MAXIMUM	UNIT
Frequency range		7		13	GHz
Receive linear gain	Rn port to COM port	3			dB
Transmit linear gain	COM port to Tn port	2			dB
In-band gain flatness				3	dB
Port VSWR				2	-
Receive noise figure				16	dB
Receive input P-1dB		-3			dBm

PARAMETER	CONDITION	MINIMUM	TYPICAL VALUE	MAXIMUM	UNIT
Transmit output P-1dB		13.5			dBm
Transmit output Psat		14			dBm
RMS Phase Error				3	Deg
Phase shift amplitude consistency		-0.8		0.8	dB
RMS attenuation error				0.7	dB
Attenuation of additional phase shift		-8		8	Deg
Transmit/receive switching time				100	ns
Single channel receiving current			70		mA
Single channel static emission current			70		mA
Single channel Po-1dB transmission current		110	140	170	mA
Single channel load current			10		mA

Table 2. Digital port electrical parameters

PARAMETER	SYMBOL	CONDITION	MINIMUM	MAXIMUM	UNIT
Input high level voltage	VIH	VCC = 2.7 V to 3.6 V,	1.7		V
Input low level voltage	VIL	VCC = 2.7 V to 3.6 V,		0.8	V
Input high level current	IIH	VCC = 2.7 V to 3.6 V,	-500	500	uA
Input low level current	IIL	VCC = 2.7 V to 3.6 V,	-500	500	uA
Output high level voltage	VOH	VCC = 2.7 V to 3.6 V, IOH = –100 uA	VCC-0.2	VCC	V
Output high level voltage	VOH	VCC = 2.7 V IOH = –4mA	2.4	VCC	V
Output low level voltage	VOL	VCC = 2.7 V to 3.6 V, IOL= 100uA	0	0.2	V
Output low level voltage	VOL	VCC = 2.7 V, IOL = 4 mA	0	0.4	V

IV. Limit parameters

Table 3.

PARAMETER	VALUE
Maximum supply voltage	3.6V
Maximum RF input power	TBD
Storage temperature	-65~150 ℃
Operating temperature	-55~125 ℃

Note: For the above listed maximum limits, if the device is operated in an environment exceeding these limits, it is likely to cause permanent damage to the device.

In actual application, it is best not to operate the device in an environment where the limit value or the value exceeds this limit value.

4.1. ESD Protection

The anti-static level (HBM) of BSTCC33-0713Q is at least Class 1B: ≥500V, <1000V. When handling, take appropriate ESD protection measures to avoid performance degradation or functional failure.

V. Pin Configuration

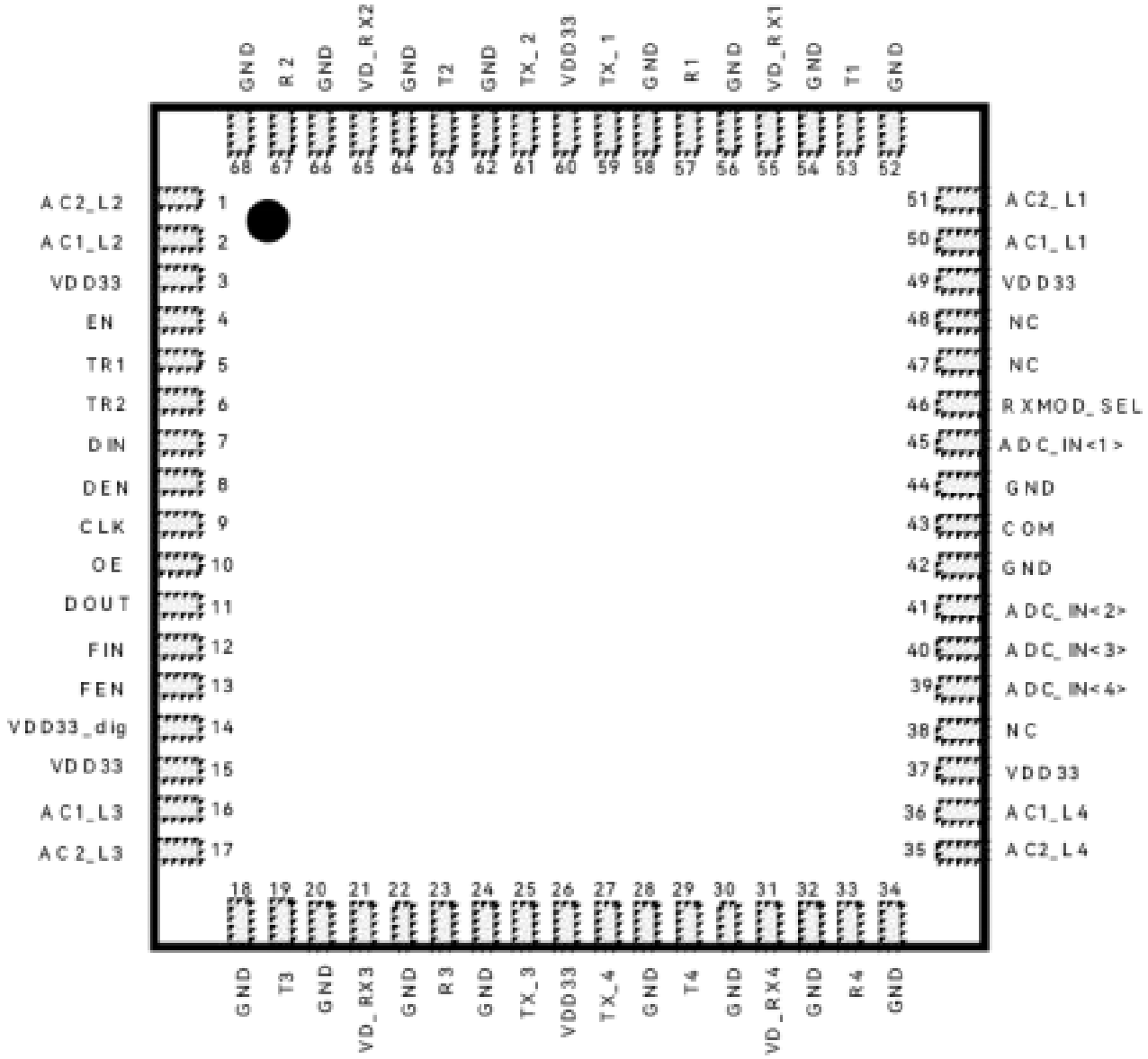

Figure 2. Chip pad layout

Table 4. Chip pad function information table

PIN NUMBER	PIN NAME	PORT ATTRIBUTES	REMARK
1	AC2_L2	control	Gain adjustment, the default setting is floating, when grounded, the receiving gain of channel 2 is reduced by 1dB
2	AC1_L2	control	Gain adjustment, the default setting is floating, when grounded, the receiving gain of channel 2 is reduced by 1dB
3	VDD33	power supply	Channel 2 3.3V power supply terminal
4	EN	Digital Input	Input, wave control enable, weak pull-down, wave control is effective when it is low
5	TR1	Digital Input	Input, wave control input control signal, weak pull-down, generate receiving control signal
6	TR2	Digital Input	Input, wave control input control signal, weak pull-down, generate pulse emission control signal
7	DIN	Digital Input	Serial signal input, weak pull-up
8	DEN	Digital Input	Input, serial data enable, weak pull-up, input valid when low
9	CLK	Digital Input	Clock input, weak pull-down, recommended 1~20MHz
10	OE	Digital Input	Input, wave control output enable, weak pull-down, output valid when low
11	DOUT	Digital Input	Serial data output, weak pull-up
12	FIN	Digital Input	Function register serial input, weak pull-up
13	FEN	Digital Input	Input, function register enable, weak pull-up, FIN input is valid when low
14	VDD33_dig	power supply	Wave control circuit 3.3V power supply terminal
15	VDD33	power supply	Channel 3 3.3V power supply terminal
16	AC1_L3	control	Gain adjustment, the default setting is floating, when grounded, the receiving gain of channel 3 is increased by 1dB
17	AC2_L3	control	Gain adjustment, the default setting is floating, when grounded, the receiving gain of channel 3 is reduced by 1dB
18	GND	Ground	
19	T3	Radio Frequency	Channel 3 Transmitter Output
20	GND	Ground	
21	VD_RX3	Output	Channel 3 LNA power modulation output, driving capability >50mA, output high level (VDD33) in receiving state, output low level in non-receiving state
22	GND	Ground	
23	R3	Radio Frequency	Channel 3 Receive Input
24	GND	Ground	
25	TX_3	Output	Channel 3 emission control output, driving capability <2mA, output high level in emission state (VDD33), non-emitting state outputs low level
26	VDD33	power supply	Channel 3 and Channel 4 3.3V power supply terminal
27	TX_4	Output	Channel 4 emission control output, driving capability <2mA, output high level in emission state (VDD33), non-emitting state outputs low level

PIN NUMBER	PIN NAME	PORT ATTRIBUTES	REMARK			
28	GND	Ground				
29	T4	Radio Frequency	Channel 4 Transmitter Output			
30	GND	Ground				
31	VD_RX4	Output	Channel 4 LNA power modulation output, driving capability >50mA, output high level (VDD33) in receiving state, output low level in non-receiving state			
32	GND	Ground				
33	R4	Radio Frequency	Channel 4 Receive Input			
34	GND	Ground				
35	AC2_L4	control	Gain adjustment, the default setting is floating, when grounded, the receiving gain of channel 3 is reduced by 1dB			
36	AC1_L4	control	Gain adjustment, the default setting is floating, when grounded, the receiving gain of channel 3 is increased by 1dB			
37	VDD33	power supply	Channel 4 3.3V power supply terminal			
38	NC					
39	ADC_IN<4>	Input	Input, Internal	Analog input signal to ADC	4	port
40	ADC_IN<3>	Input	Input, Internal	Analog input signal to ADC	3	port
41	ADC_IN<2>	Input	Input, Internal	Analog input signal to ADC	2	port
42	GND	Ground				
43	COM	Radio Frequency		RF common port		
44	GND	Ground				
45	ADC_IN<1>	Input	Input, Internal	Analog input signal to ADC	1	port
46	RXMOD_SEL	control	The default setting is floating. When grounded, the four transmitting channels of the chip are turned off and the chip enters the four-channel pure receiving mode.			
47	NC					
48	NC					
49	VDD33	power supply	Channel 1 3.3V power supply terminal			
50	AC1_L1	control	Gain adjustment, the default setting is floating, when grounded, the receiving gain of channel 1 is increased by 1dB			
51	AC2_L1	control	Gain adjustment, the default setting is floating, when grounded, the receiving gain of channel 1 is reduced by 1dB			
52	GND	Ground				
53	T1	Radio Frequency	Channel 1 Transmit Output			
54	GND	Ground				
55	VD_RX1	Output	Channel 1 LNA power modulation output, driving capability > 50mA, output high level (VDD33) in receiving state, output low level in non-receiving state			

PIN NUMBER	PIN NAME	PORT ATTRIBUTES	REMARK
56	GND	Ground	
57	R1	Radio Frequency	Channel 1 Receive Input
58	GND	Ground	
59	TX_1	Output	Channel 1 transmit control output, drive capability <2mA, output high level in transmit state (VDD33), non-emitting state outputs low level
60	VDD33	power supply	Channel 1 and channel 2 3.3V power supply terminal
61	TX_2	Output	Channel 2 emission control output, driving capability <2mA, output high level in emission state (VDD33), non-emitting state outputs low level
62	GND	Ground	
63	T2	Radio Frequency	Channel 2 Transmit Output
64	GND	Ground	
65	VD_RX2	Output	Channel 2 LNA power modulation output, driving capability > 50mA, output high level (VDD33) in receiving state, output low level in non-receiving state
66	GND	Ground	
67	R2	Radio Frequency	Channel 2 Receive Input
68	GND	Ground	

VI. Typical curve

(Unless otherwise specified, the test conditions are 3.3V power supply, room temperature, phase shift attenuation base state. All test curves are the test results of the chip on the evaluation board, and the gain in the attenuation and phase shift curves does not deduct the board loss).

* To be tested

6.1. Digital wave control function

The digital part mainly includes 5 identical control channels and a common logic. The 5 control channels include reg_data1 module, reg_data2 module

block, reg_data3 module, self-test module and switch control logic; the public logic includes reg_fun1 module, reg_fun2 module, pulse protection module and temperature protection module.

6.2. Single channel control logic function description

6.2.1. Serial data register reg_data1

Serial data input: DEN is low, CLK rises, and data is written from the DIN port to the first group of registers reg_data1[0] in sequence; the original data in reg_data1 is moved from reg_data1[0] to reg_data1[25] in sequence.

Serial data output: The single-channel serial data output dout takes reg_data1[25] as output.

Serial self-test data loading: When When DEN is high and the rising edge of CLK is detected, the self-test data specified by reg_fun2[2][7:0] is written to the serial register reg_data1.

6.2.2. Serial data register reg_data2

Data selection input: On the first CLK rising edge after the den rising edge, reg_data1 is written to the function register reg_fun2 [0] [4:0] selected

Secondary data register reg_data2. The 32 groups of data in the secondary data register reg_data2 are defined as shown in Table 4. Data selection output: A group of reg_data2[n][25:0] selected by reg_fun2[1][4:0] is output for phase attenuation and control.

Table 5. Secondary data register data definition

DATA DEFINITION IN REG_DATA2[N][25:0]																								
D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
AT5	AT4	AT3	AT2	AT1	AT0	MCT	MCR	AR5	AR4	AR3	AR2	AR1	AR0	PT5	PT4	PT3	PT2	PT1	PT0	PR5	PR4	PR3	PR2	PR1	PR0

6.2.3. Serial data register reg_data3

DEN is low and the DIN serial input {5{26'h15D5A5A}} is internally unlocked.

At the second CLK rising edge after the FEN rising edge, when reg_fun1[11:8]=4'h1, the data dat_seled in the corresponding address of the reg_data2 array specified by reg_fun1[7:0] is written to the reg_data3 register; otherwise, the reg_data3 register remains unchanged.

reg_data3 is updated, reg_fun1 must be written once. If reg_fun1 is not written, it will not be updated.

6.2.4. PH and ATT function control output

Table 6. Phase shift and attenuation function control output logic

ENTER	CHANNEL 1~ CHANNEL 5 OUTPUT		STATE
TR1	PH[5:0]	ATT[5:0]	
1	PT[5:0]	AT[5:0]	Emission state
0	PR[5:0]	AR[5:0]	Receiving state

6.3. Switch control output

The switch control logic is listed in Table 6, where the input signal PTR2 is taken from the pulse width protection module, and MCT and MCR are taken from reg_data3.

Table 7. Channel 1~4 switch control output logic

ENTER						LOSE	OUT	CORRESPONDING CHANNEL STATUS
EN	TR1	PTR2	MCT	MCR	RX		TX	
0	0	0	x	0	1		0	Receiving state
0	1	1	0	x	0		1	Emission state
		Other combinations			0		0	Load state

VII. Function Register Input Timing

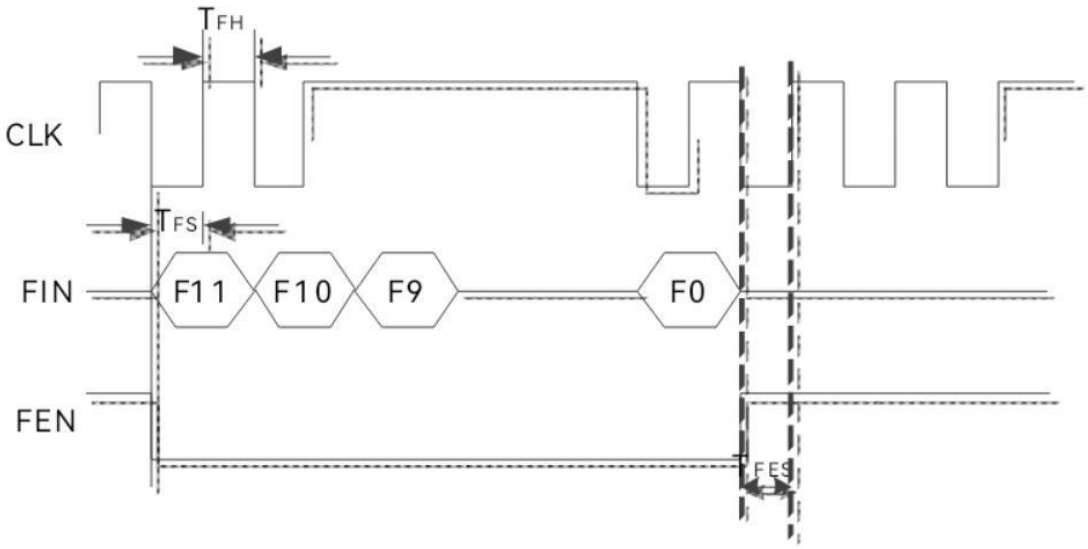

Figure 3. Function Register Input Timing

FEN is low, FIN is sampled on the rising edge of the clock and internally serialized to reg_fun1[11:0]. At the first rising edge of clk after the rising edge of FEN, reg_fun1[7:0] is stored

in the secondary function register reg_fun2. The storage address is determined by reg_fun1[11:8].

7.1. Serial Data Register Input Timing

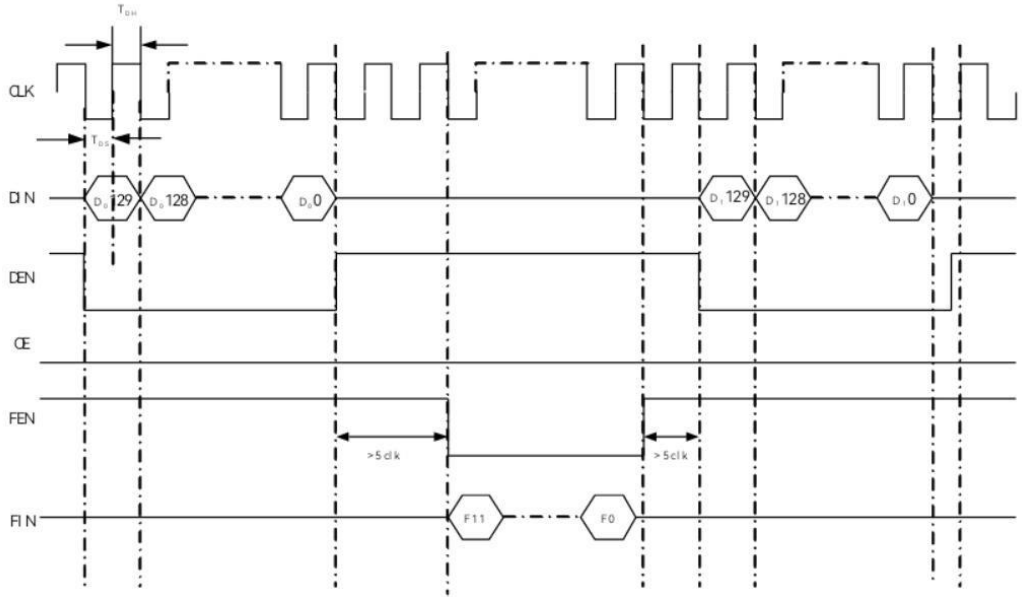

Figure 4. Serial Data Input Timing

Before performing the phase shift attenuation control operation, the command unlocking operation is performed first: DEN is low, DIN serial input {5{26'h15D5A5A}} performs internal unlocking, and after the unlocking is completed, the phase shift attenuation and control code are input.

DEN is low, the rising edge of the clock samples DIN, which is internally serialized and transferred to reg_data1[25:0], and reg_data1 is stored in the rising edge of DEN.

Secondary data storage area, the address is determined by the function register reg_fun2[0], the default address is 31. At the second CLK rising edge after the FEN rising edge, when reg_fun1[11:8]=4'h1 and internal unlocking, the data in the corresponding address of the reg_data2 array specified by reg_fun1[7:0] is written to the reg_data3 register; otherwise, the reg_data3 register remains unchanged.

7.2. Serial Data Register Output Timing

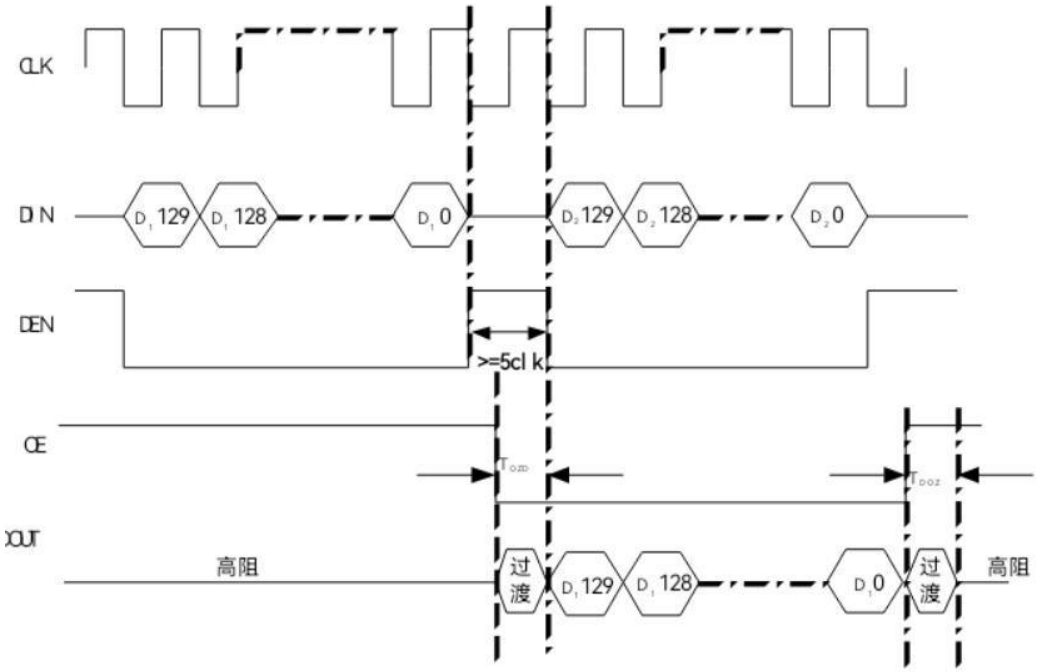

Figure 5. Serial Data Output Timing

VIII. Packaging Solutions

The chip adopts QFN68 pin package with a size of 8mm×8mm. The detailed size information is shown in the figure below.

The metal on the back of the chip after packaging is the ground terminal of the DC and AC signals of the entire chip and the main heat dissipation output terminal of the chip. When used, it needs to have a fully ideal connection with the ground plane on the board and fully good heat dissipation.

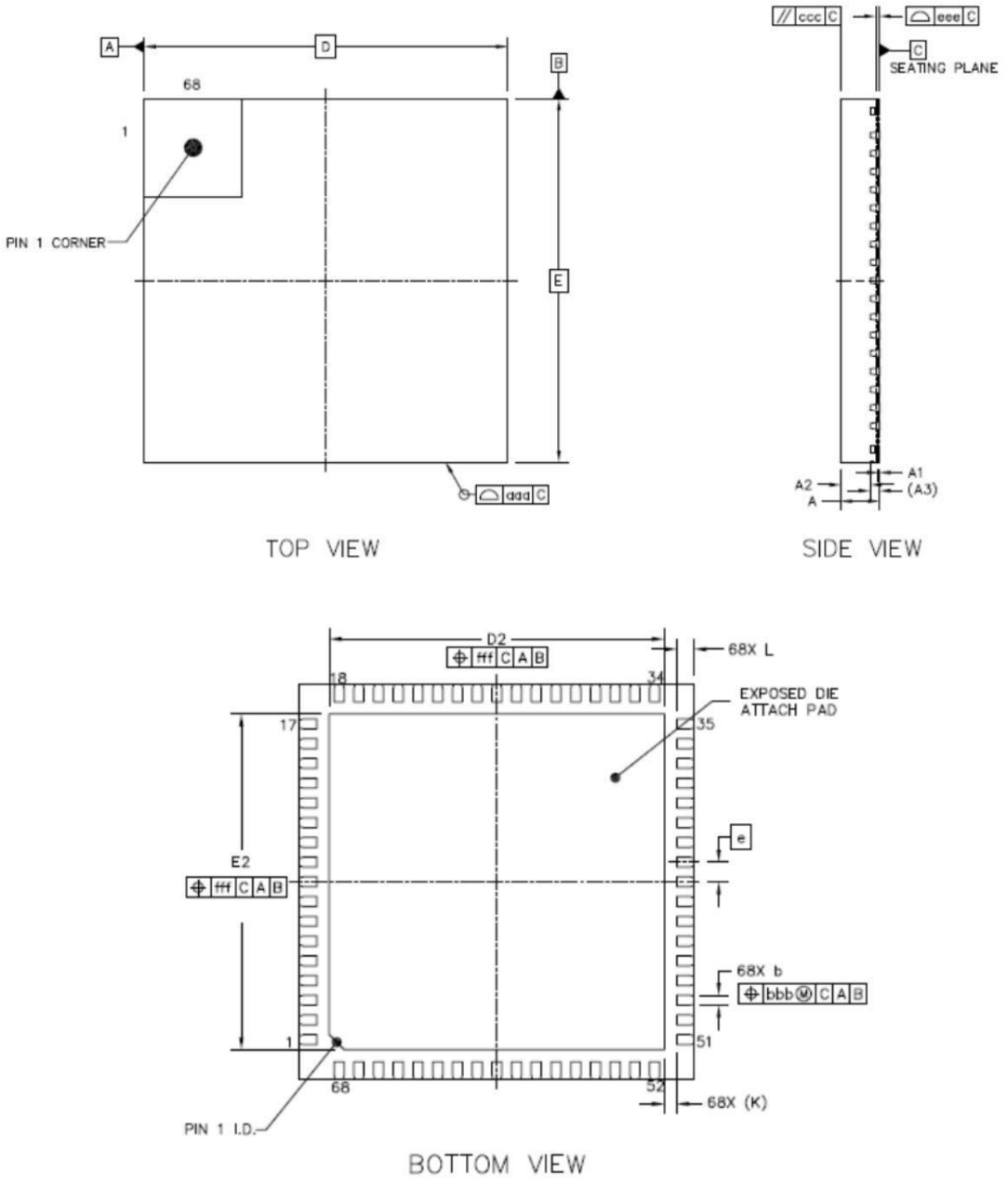

Figure 6. Package front view, side view, bottom view

Table 10. Package dimensions

NAME	DIMENSION SYMBOLS	VALUE (MM)		
		MINIMUM	NOMINAL	MAXIMUM
Total thickness	A	0.8	0.85	0.9
Stand off	A1	0	0.02	0.05
Mold thickness	A2	—	0.65	—
L/F thickness	A3		0.203 REF	
Lead width	b	0.15	0.20	0.25
Body size/ X	D		8 BSC	

NAME	DIMENSION SYMBOLS	VALUE (MM)		
		MINIMUM	NOMINAL	MAXIMUM
Body size/ Y	E		8 BSC	
Lead pitch	e		0.4 BSC	
EP size/ X	D2	6.7	6.8	6.9
EP size/ Y	E2	6.7	6.8	6.9
Lead length	L	0.25	0.35	0.45
Lead tip to exposed pad edge	K		0.35 REF	
Package edge tolerance	aaa		0.1	
Mold flatness	ccc		0.1	
Coplanarity	eee		0.08	
Lead offset	bbb		0.07	
Exposed pad offset	fff		0.1	