BSTCC06-0513

Broadband Four-Channel Multi-Function

Chip Data Sheet

I. Product Introduction

BSTCC06-0513 is a broadband four-channel multifunctional chip. The operating frequency range is 5GHz ~ 13GHz. The chip integrates low noise amplifier, power amplifier, RF front-end switch, 6-bit digital controlled attenuator, 6-way CNC phase shifter, power divider, beam control, low noise amplifier power modulation and other modules can provide a maximum attenuation range of 31.5dB, stepping 0.5dB, and a phase shift range of 360 °, stepping 5.6 °.

II. Application Areas

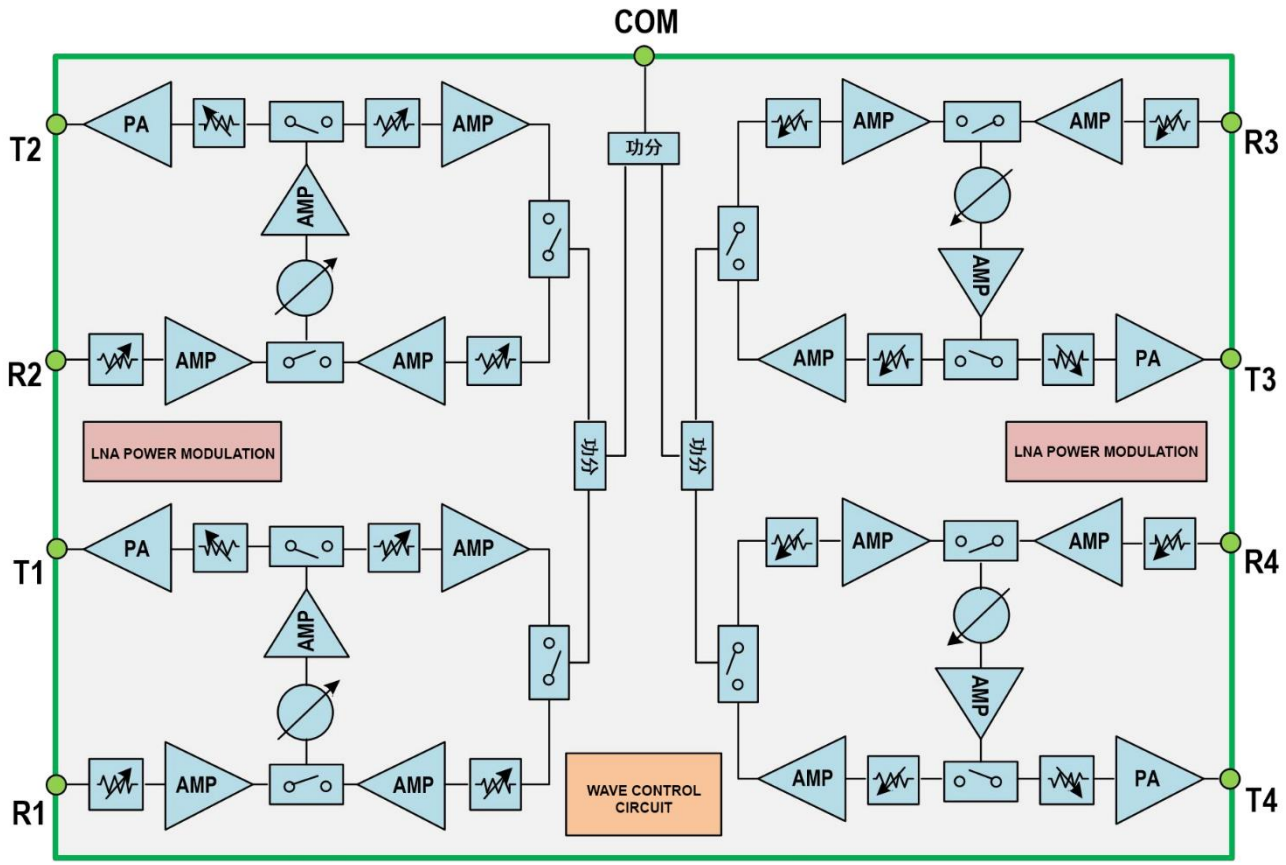

Figure 1. BSTCC06-0513 Functional Block Diagram

III. Key technical indicators

- Working power supply voltage: 3.3V
- Operating frequency range: 5GHz ~ 13GHz
- 6-bit attenuation control, step 0.5dB
- 6 phase shift control bits, 5.6° step
- Receive gain: 4dB (Rn port to COM port)
- Transmitter gain: 16dB (COM port to Tn port)
- Gain flatness in transmit and receive band: 3dB
- Port standing wave ratio VSWR: 1.8
- Receive noise factor NF: 12dB
- Receive input Pin-1dB: 0dBm
- Transmitter output Po-1dB: 17dBm
- RMS phase shift error: <3°
- Amplitude consistency during phase shift: <±0.8dB
- Attenuation accuracy: <0.2 + 5%Ai
- RMS attenuation error: <0.8dB
- Attenuation additional phase shift: <5°
- Transmit/receive switching time: <100ns
- Single channel operating current: 85mA/90(170)mA/2mA @receive/static (Po-1dB) transmit/load
- Package size: QFN 9×9mm
- Process: SiGe BiCMOS

IV. Electrical Characteristics

Table 1. Basic electrical properties

PARAMETER	CONDITION	MINIMUM	TYPICAL VALUE	MAXIMUM	UNIT
Frequency range		5		13	GHz
Receive linear gain	Rn port to COM port		4		dB
Transmit linear gain	COM port to Tn port		16		dB
In-band gain flatness			3		dB
Port VSWR			1.8		—

PARAMETER	CONDITION	MINIMUM	TYPICAL VALUE	MAXIMUM	UNIT
Receive noise figure			13		dB
Receive input P-1dB			0		dBm
Transmit output P-1dB		16	17		dBm
Transmit output Psat			19		dBm
RMS Phase Shift Error				3	Deg
Phase shift amplitude consistency		-0.8		0.8	dB
RMS attenuation error				0.8	dB
Attenuation of additional phase shift		-2		15	Deg
Transmit/receive switching time				100	ns
Single channel receiving current			85		mA
Single channel static emission current			90		mA
Single channel Po-1dB transmission current		150	170	200	mA
Single channel load current			2		mA

Table 2. Digital port electrical parameters

PARAMETER	SYMBOL	CONDITION	MINIMUM	MAXIMUM	UNIT
Input high level voltage	VIH	VCC = 2.7 V to 3.6 V,	1.7		V
Input low level voltage	VIL	VCC = 2.7 V to 3.6 V,		0.8	V
Input high level current	IIH	VCC = 2.7 V to 3.6 V,	-500	500	uA
Input low level current	IIL	VCC = 2.7 V to 3.6 V,	-500	500	uA
Output high level voltage	VOH	VCC = 2.7 V to 3.6 V, IOH = –100 uA	VCC-0.2	VCC	V
Output high level voltage	VOH	VCC = 2.7 V IOH = –4mA	2.4	VCC	V
Output low level voltage	VOL	VCC = 2.7 V to 3.6 V, IOL= 100uA	0	0.2	V
Output low level voltage	VOL	VCC = 2.7 V, IOL = 4 mA	0	0.4	V

V. Limit parameters

Maximum supply voltage 3.6V

Maximum RF input power 20dBm

Storage temperature 65 ～ 150 ℃

Operating temperature	55 ～ 125 ℃

Note: For the above listed maximum limits, if the device is operated in an environment exceeding these limits, it is likely to cause permanent damage to the device.

In actual application, it is best not to operate the device in an environment where the limit value or the value exceeds this limit value.

5.1. ESD Protection

BSTCC06-0513 is at least Class 2: ≥2000V. When handling, take appropriate ESD protection measures to avoid performance degradation or functional failure.

VI. Pin Configuration

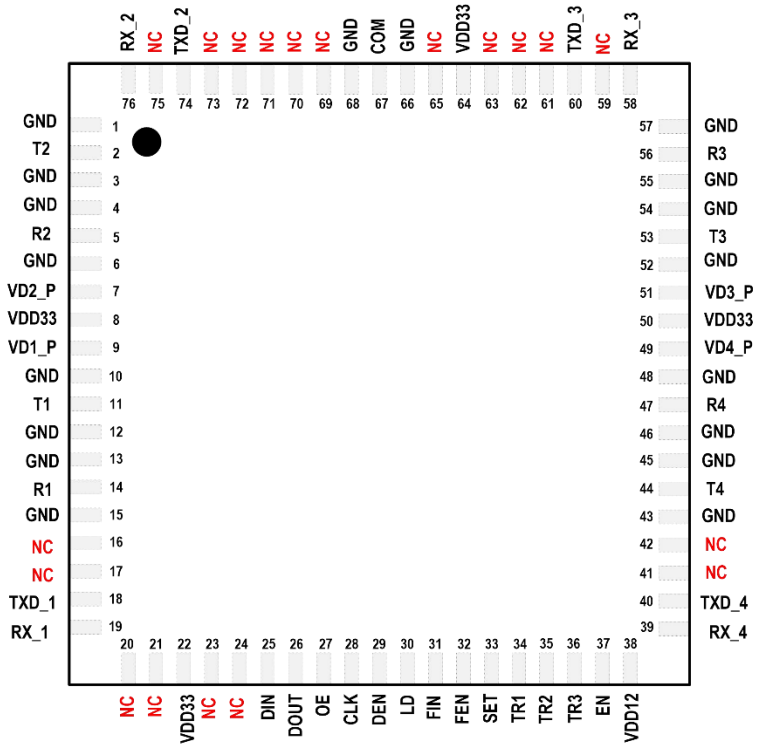

Figure 2. Chip pad layout Figure 3 Pin function information table

Table 3. Digital port electrical parameters

PIN NUMBER	PIN NAME	PORT ATTRIBUTES	REMARK	PIN NUMBER	PIN NAME	PORT ATTRIBUTES	REMARK
1	GND	Ground		39	RX_4	Output	Channel 4 receiving control output, output low level in receiving state, driving capability 2mA
2	T2	Radio Frequency	Channel 2 RF transmit output	40	TXD_4	Output	Channel 4 emission control output, output high level in emission

PIN NUMBER	PIN NAME	PORT ATTRIBUTES	REMARK	PIN NUMBER	PIN NAME	PORT ATTRIBUTES	REMARK
							state, driving capability 2mA
3	GND	Ground		41	NC		
4	GND	Ground		42	NC		
5	R2	Radio Frequency	Channel 2 RF receiving input	43	GND	Ground	
6	GND	Ground		44	T4	Radio Frequency	Channel four RF transmission output
7	VD2_P	Output	Channel 2 low noise amplifier power supply modulation Output, driving capability 100mA, output high level in receiving state	45	GND	Ground	
8	VDD33	power supply	Channel 1 and 2 3.3V power supply terminal	46	GND	Ground	
9	VD1_P	Output	Channel 1 low noise amplifier power supply modulation Output, driving capability 100mA, output high level in receiving state	47	R4	Radio Frequency	Channel 4 RF receiving input
10	GND	Ground		48	GND	Ground	
11	T1	Radio Frequency	Channel 1 RF transmit output	49	VD4_P	Output	Channel 4 low noise amplifier power supply modulation Output, driving capability 100mA, output high level in receiving state
12	GND	Ground		50	VDD33	power supply	Channel 3 and 4 3.3V power supply terminal
13	GND	Ground		51	VD3_P	Output	Channel 3 low noise amplifier power supply modulation Output, driving capability 100mA, output high level in receiving state
14	R1	Radio Frequency	Channel 1 RF receiving input	52	GND	Ground	
15	GND	Ground		53	T3	Radio Frequency	Channel three RF transmission output
16	NC			54	GND	Ground	
17	NC			55	GND	Ground	

PIN NUMBER	PIN NAME	PORT ATTRIBUTES	REMARK	PIN NUMBER	PIN NAME	PORT ATTRIBUTES	REMARK
18	TXD_1	Output	Channel 1 transmit control output, output high level in transmit state, driving capability 2mA	56	R3	Radio Frequency	Channel 3 RF receiving input
19	RX_1	Output	Channel 1 receives the control output, outputs low level in receiving state, driving capability 2mA	57	GND	Ground	
20	NC			58	RX_3	Output	Channel 3 receiving control output, output low level in receiving state, driving capability 2mA
21	NC			59	NC		
22	VDD33	power supply	Wave control circuit power supply terminal	60	TXD_3	Output	Channel three transmit control output, output high level in transmit state,
23	NC			61	NC		Driving capability 2mA
24	NC			62	NC		
25	DIN	Input	Serial signal input, weak pull-down	63	NC		
26	DOUT	Input	Serial data output, weak pull-up	64	VDD33	power supply	Control circuit 3.3V power supply terminal
27	OE	Input	Input, wave control output enable, weak pull-down, output valid when low	65	NC		
28	CLK	Input	Clock input, weak pull-down, recommended 1~20MHz	66	GND	Ground	
29	DEN	Input	Serial data enable, weak pull-up, input valid when low	67	COM	Radio Frequency	RF common port
30	LD	Input	Self-test control signal, weak pull-down	68	GND	Ground	
31	FIN	Input	Function register serial	69	NC		

PIN NUMBER	PIN NAME	PORT ATTRIBUTES	REMARK	PIN NUMBER	PIN NAME	PORT ATTRIBUTES	REMARK
			input, weak pull-up				
32	FEN	Input	Function register enable, weak pull-up, FIN input is valid when low	70	NC		
33	SET	Input	Three-level register latch, weak pull-down	70	NC		
34	TR1	Input	Wave control input control signal, weak pull-down, generate receiving control signal	72	NC		
35	TR2	Input	Wave control input control signal, weak pull-down, generate pulse emission control signal	73	NC		
36	TR3	Input	Wave control input control signal, weak pull-down, generate continuous wave emission control signal, grounded when not in use	74	TXD_2	Output	Channel 2 emission control output, output high level in emission state, driving capability 2mA
37	EN	Input	Wave control enable, weak pull-down, wave control is effective when it is low	75	NC		
38	VDD12	power supply	1.2V power supply lead of the wave control circuit is recommended to be connected externally 0.1uF voltage stabilizing capacitor to prevent electromagnetic interference	76	RX_2	Output	Channel 2 receives the control output, outputs low level in receiving state, driving capability 2mA

VI. Typical curves

(unless otherwise specified, the test conditions are power 3.3V, normal temperature environment, phase shift attenuation ground state)

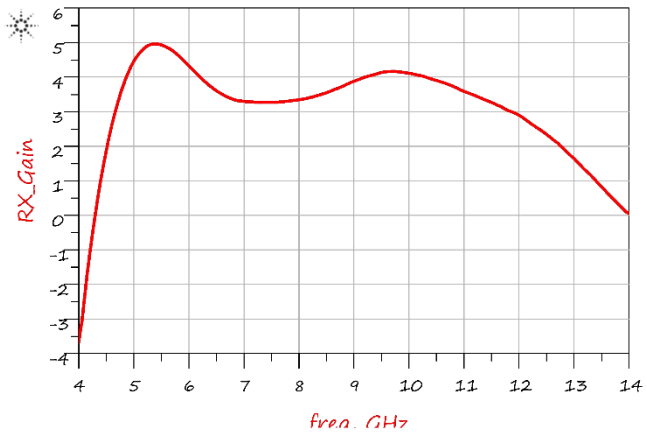

Figure 3. Receiver Gain (Rn to COM)

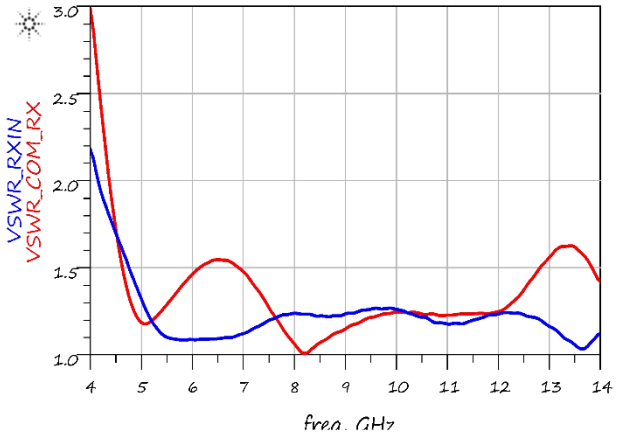

Figure 4. Receiver Port Standing Wave

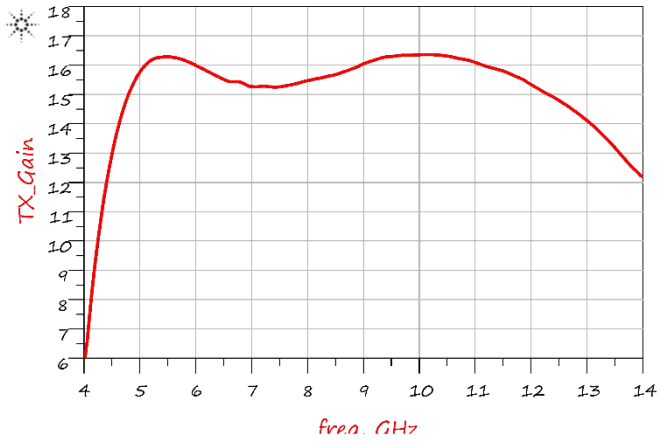

Figure 5. Transmitter Gain (COM to Tn)

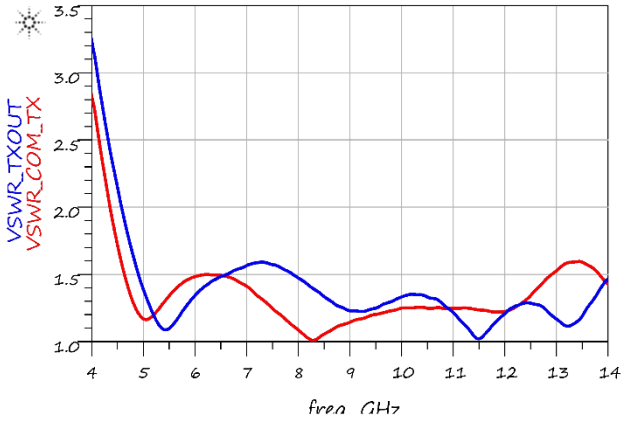

Figure 6. Transmitter Port Standing Wave

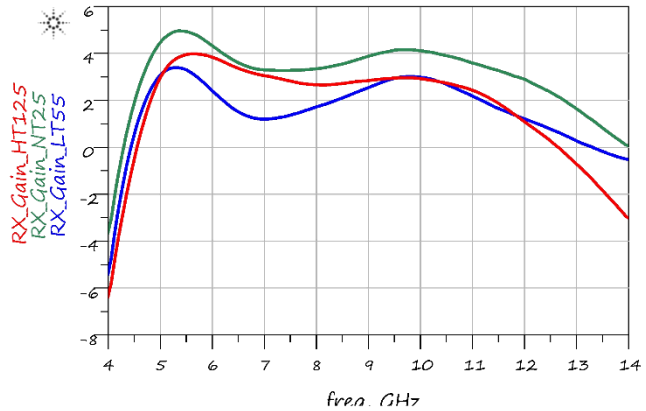

Figure 7. Receive high and low temperature gain (-55 ℃ ~ +125 ℃)

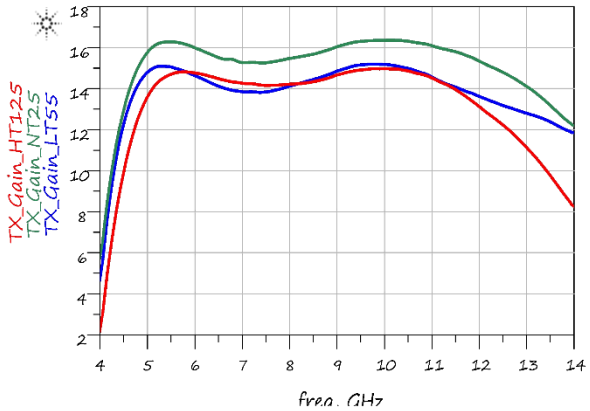

Figure 8. Transmit high and low temperature gain (-55 ℃ ~+ 125 ℃)

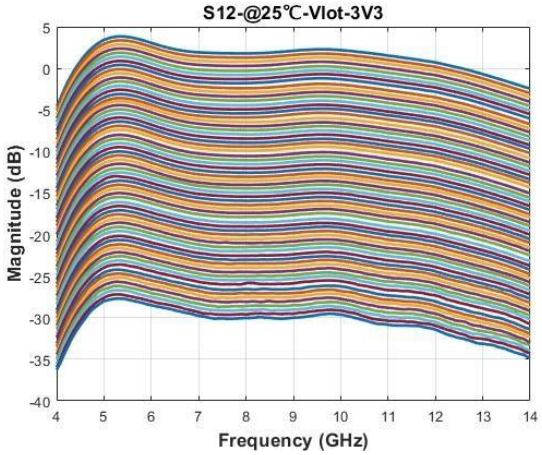

Figure 9. Receive gain 64-state attenuation curve vs frequency

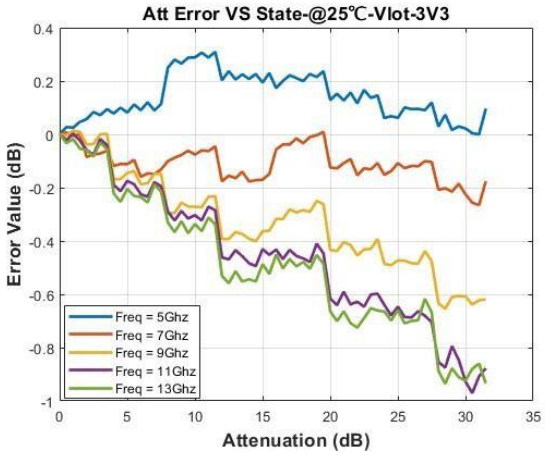

Figure 10. Receive mode attenuation error vs attenuation value

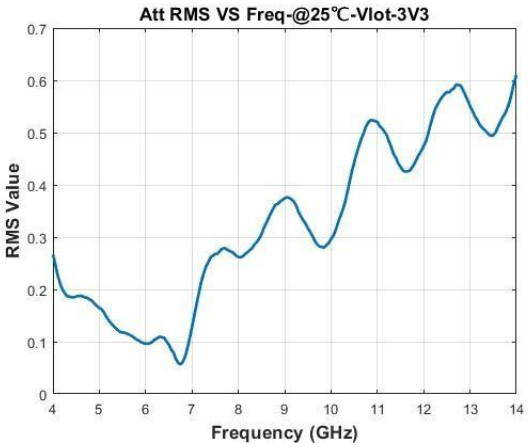

Figure 11. RMS attenuation error vs. frequency in receive mode

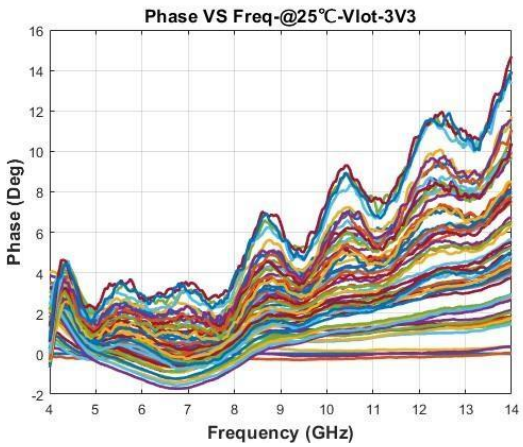

Figure 12. Additional phase shift vs. frequency in receive mode with 64-state attenuation

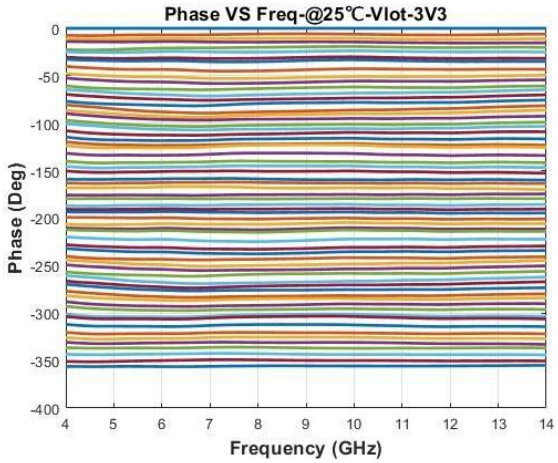

Figure 13. Relative phase shift curve of 64 states in receiving mode vs. frequency

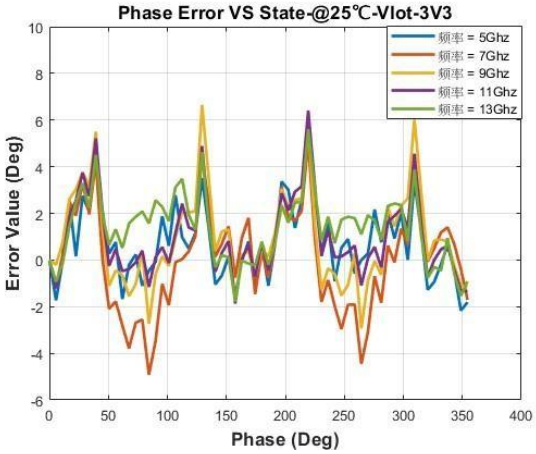

Figure 14. Phase shift error vs. phase shift value in receiving mode

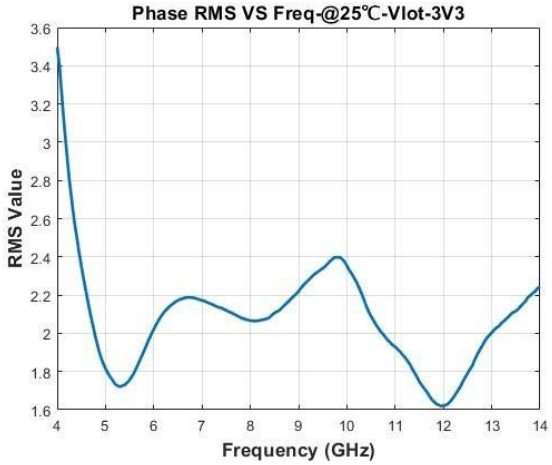

Figure 15. RMS phase shift error vs. frequency in receiving mode

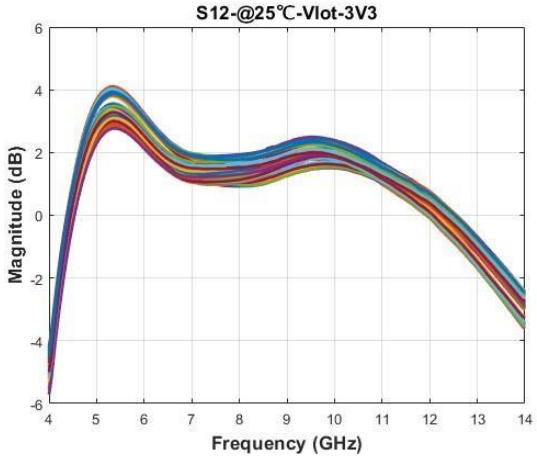

Figure 16. Gain curve vs. frequency in receiving mode 64-state phase shift

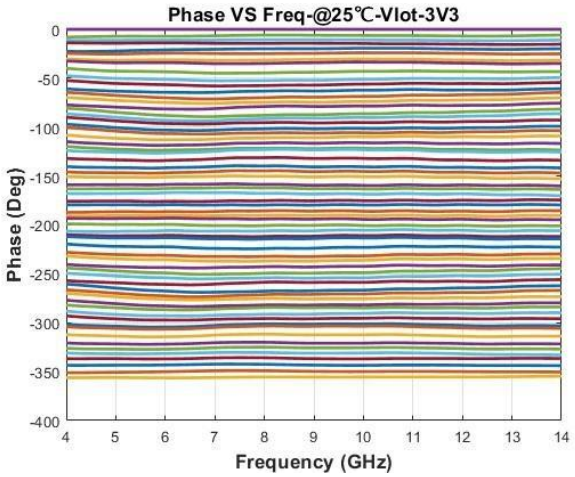

Figure 17. Transmit mode 64-state relative phase shift curve vs. frequency

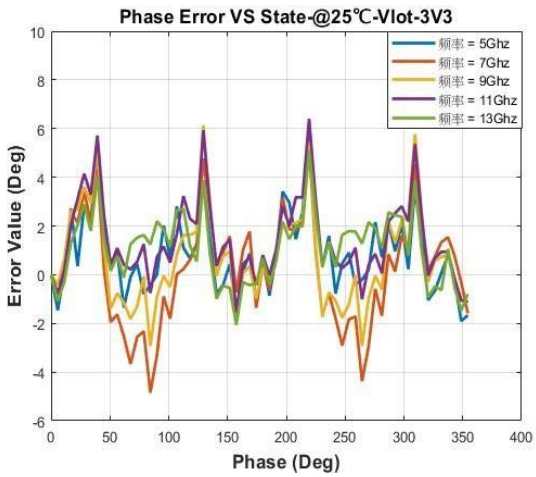

Figure 18. Transmit mode phase shift error vs. phase shift value

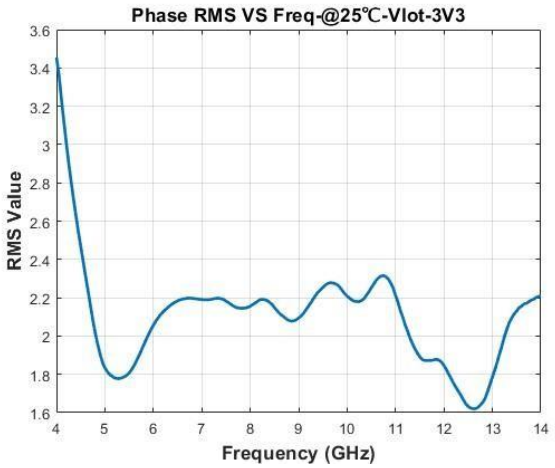

Figure 19. Transmit mode RMS phase shift error vs. frequency

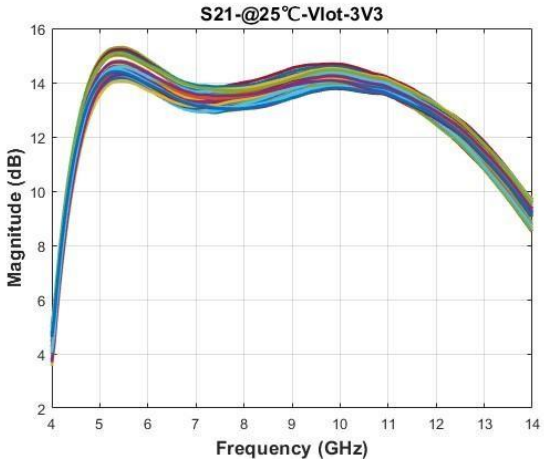

Figure 20. Transmit mode 64-state phase shift gain curve vs. frequency

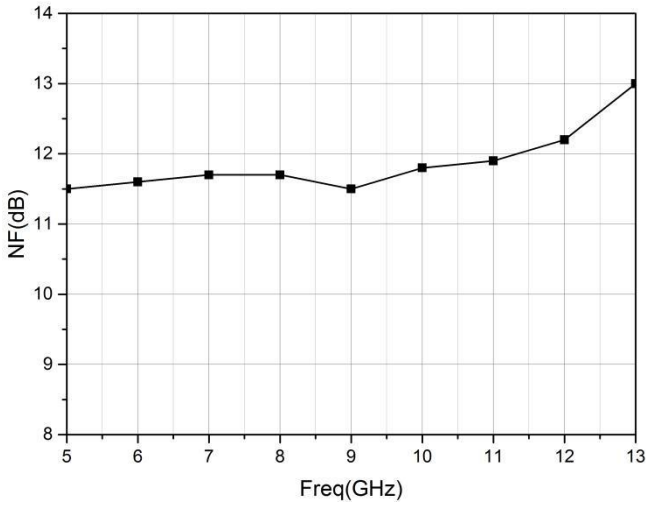

Figure 21. Receive noise coefficient vs. frequency

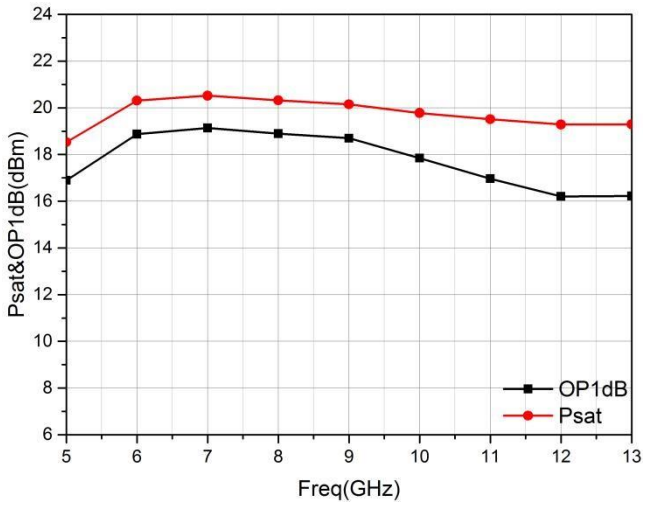

Figure 22. Transmit output 1dB power, saturation power vs. frequency

6.1. Digital wave control function

The digital part mainly includes 5 identical control channels and one common logic. The 5 control channels include reg_data1 module, reg_data2 module, reg_data3 module, self-test module and switch control logic; the common logic includes reg_fun1 module, reg_fun2 module, pulse protection module and temperature protection module.

6.2. Single channel control logic function description

6.2.1. Serial data register reg_data1

Serial data input: When DEN is low, LD is low, and CLK rises, data is written from the DIN port to the first group of registers reg_data1[0] in sequence, and each group of registers reg_data1[25] writes the next group of registers reg_data1[0] ; the original data in each group of reg_data1 is moved from reg_data1[0] to reg_data1[25] in sequence ; the reset value of reg_data1 is all 1.

Serial data output: At the falling edge of CLK, data is written from the fifth group reg_data1[25] to the reg_dout output register, and reg_dout is output through the DOUT port. The DOUT port outputs normally when OE is low, and outputs high configuration when OE is high.

Serial self-test data loading: LD is high, CLK rising edge, the self-test data specified by the reg_fun2[2][7:0] register is written to the serial register reg_data1.

6.2.2. Serial data register reg_data2

Data selection input: Three cycles after the rising edge of DEN, when cal_en is high (default value is 1'b1), the serial data register

The data in (reg_data1) is written to the secondary data register (reg_data2) selected by the function register reg_fun2[0][4:0]. The reset value of reg_data2 is all 1s.

Data selection output: On the rising edge of SET, the secondary data register (reg_data2) is output by 32:1 mux, and a set of data selected by the function register reg_fun2[1][4:0] is written into the tertiary data register (reg_data3); the reset value of reg_data3 is all 1.

Table 4. Three-level data register

Data definition in reg_data3[25:0]

D25	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
AT5	AT4	AT3	AT2	AT1	AT0	MCT	MCR	AR5	AR4	AR3	AR2	AR1	AR0	PT5	PT4	PT3	PT2	PT1	PT0	PR5	PR4	PR3	PR2	PR1	PR0

6.2.3. PH and ATT function control output

Table 5. Phase shift and attenuation control

INPUT	**OUTPUT**		**STATE**
TR1	PH[5:0]	ATT[5:0]	
1	PT[5:0]	AT[5:0]	Emission state
0	PR[5:0]	AR[5:0]	Receiving state

VII. Switch control output

For the transmit/receive status control, the five channels use the same logic control input, and the transmit/receive status control bits of each channel output the status of the corresponding channel respectively.

The RX and TXD control outputs of each channel are finally brought out from the pads, with 0 or 3.3V control output and approximately 2mA driving capability.

The output status is determined by the external input TR1, TR3, EN and the internal configuration mct, mcr signals, as well as the pulse protection output PTR2 state.

Table 6. Status Control Description

INPUT						OUTPUT			CORRESPONDING CHANNEL STATUS
EN	TR1	PTR2 (Pulse protection logic output)	TR3	MCR	MCT	VD_P	RX	TXD	
0	0	0	0	0	x	1	0	0	Receiving state
0	1	0	0	0	x	0	1	0	Transition state
0	1	1	0	x	0	0	1	1	Pulse emission state
0	1	0	1	x	0	0	1	1	Continuous wave emission state
Other combinations						0	1	0	Load state

7.1. Function register reg_fun1

Serial data input: FEN is low, CLK rises, data is written from the FIN port to reg_fun1[0] in sequence, the original data in reg_fun1 is moved from reg_fun1[0] to reg_fun1[11] in sequence, and the reset value of reg_fun1 is all 1.

7.2. Function Register reg_fun2

According to the address determined by reg_fun1[11:8], the reg_fun1[7:0] data is written to the specified location of the reg_fun2 register three cycles after the rising edge of FEN.

The function register description is listed in Table 7. The high and low bits of the function register group bytes in the table are consistent with the high and low order of the internal function register bit definition.

Table 7. Function register description

SERIAL NUMBER	REGISTER NAME	INITIAL VALUE	REMARK
1	reg_fun2[0]	8'hff	reg_fun2[0][4:0] L2 data cache reg_data2 register group write address
2	reg_fun2[1]	8'hff	reg_fun2[1][4:0] L2 data cache reg_data2 register group output address
3	reg_fun2[2]	8'hff	reg_fun2[3][7:0] Serial output self-test data load selection address
4	reg_fun2[3]	8'hff	reg_fun2[3][4:0] Pulse width protection is valid. Each channel has one bit, and the protection function can be turned on and off separately.
5	reg_fun2[4]	8'h2	Accumulated number pro_add[7:0] Decrement number pro_dec[7:0]
6	reg_fun2[5]	8'h1	
7	reg_fun2[6]	8'h68	Default protection threshold 205μs(4MHz)
8	reg_fun2[7]	8'h6	
9	reg_fun2[8]	8'h0	

SERIAL NUMBER	REGISTER NAME	INITIAL VALUE	REMARK
10	reg_fun2[9]	8'h0	
11	reg_fun2[10]	8'hff	Temperature sensor enable, temperature protection enable, protection threshold 6'h3F
12	reg_fun2[11]	8'hff	Temperature protection status flag, temperature sensor feedback temperature 6 bits
13	reg_fun2[12]	8'h02	reg_fun2[12][7:6] reads the upper 2 bits of the MTP address, reg_fun2[12][0] reads and writes MTP/EEPROM enable, reg_fun2[12][1] compensation enable (cal_en)
14	reg_fun2[13]	8'h00	Read MTP lower 8 bits address
15	reg_fun2[14]	0x01	Hardware version low (initial version number, chip upgrade version number increases)
16	reg_fun2[15]	8'h10	Hardware version: High-end Meichen 8'h10
17	reg_data1	26'h3ffffff	
18	reg_data2[31:0]	26'h3ffffff	
19	reg_data3	26'h3ffffff	
20	pro_cnt	32'h0	
21	pro_out	5'h0	

VIII. Wave control timing requirements

8.1. Function register input timing

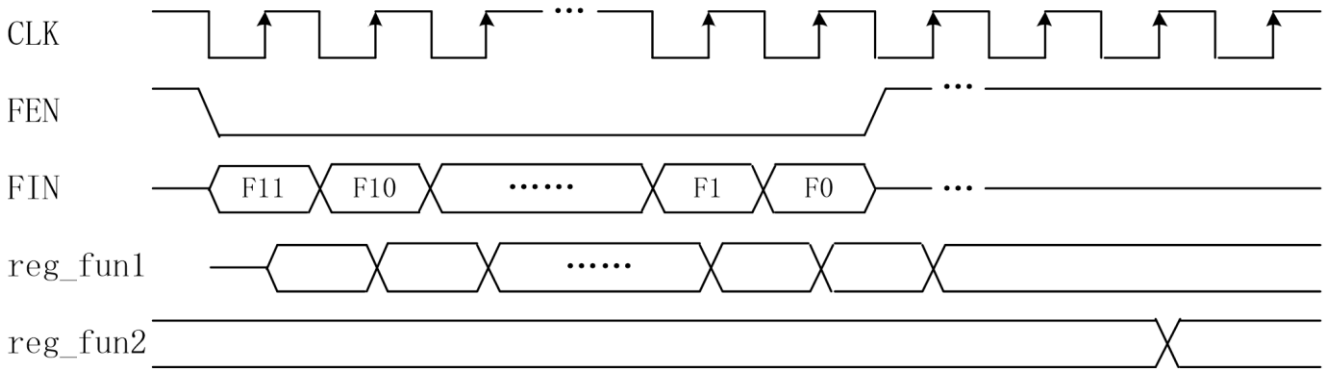

Figure 23. Function register input timing

FEN is low, FIN is sampled on the rising edge of the clock and internally serialized to reg_fun1[11:0]. Three cycles after the rising edge of FEN, reg_fun1[7:0] is stored in the secondary function register reg_fun2. The stored address is determined by reg_fun1[11:8].

Serial Data Register Input Timing

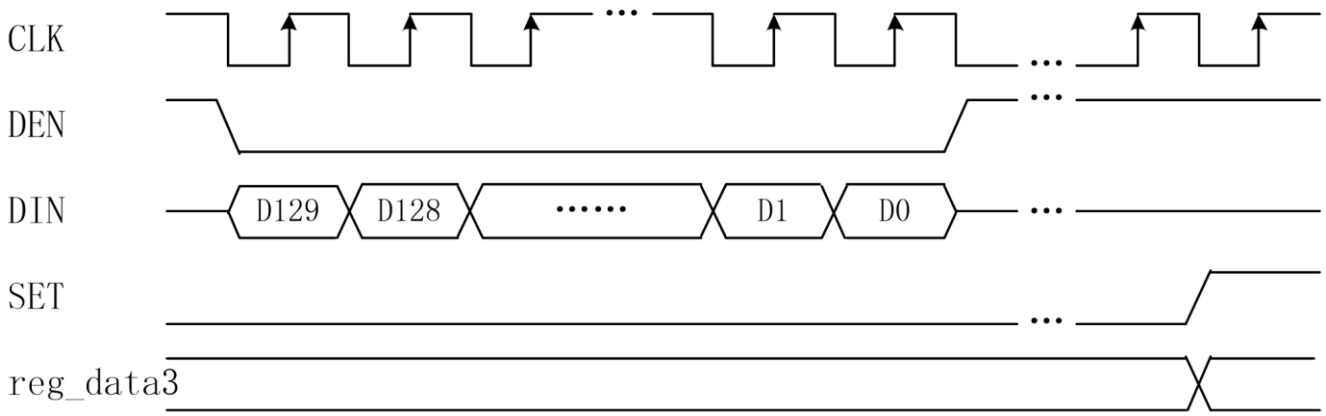

Figure 24. Serial data input timing

DEN is low, the rising edge of the clock samples DIN, which is internally serialized and transferred to reg_data1[25:0]. At the rising edge of DEN, reg_data1 is stored in the secondary data storage area. The address is determined by the function register reg_fun2[0] and the default address is 31. At least 3 cycles after DEN is pulled high, the SET signal is pulled high. At the rising edge of SET, the data at a certain address in the secondary data storage area is updated to reg_data3. The address is determined by reg_fun2[1] and the default address is 31.

8.2. Serial Data Register Output Timing

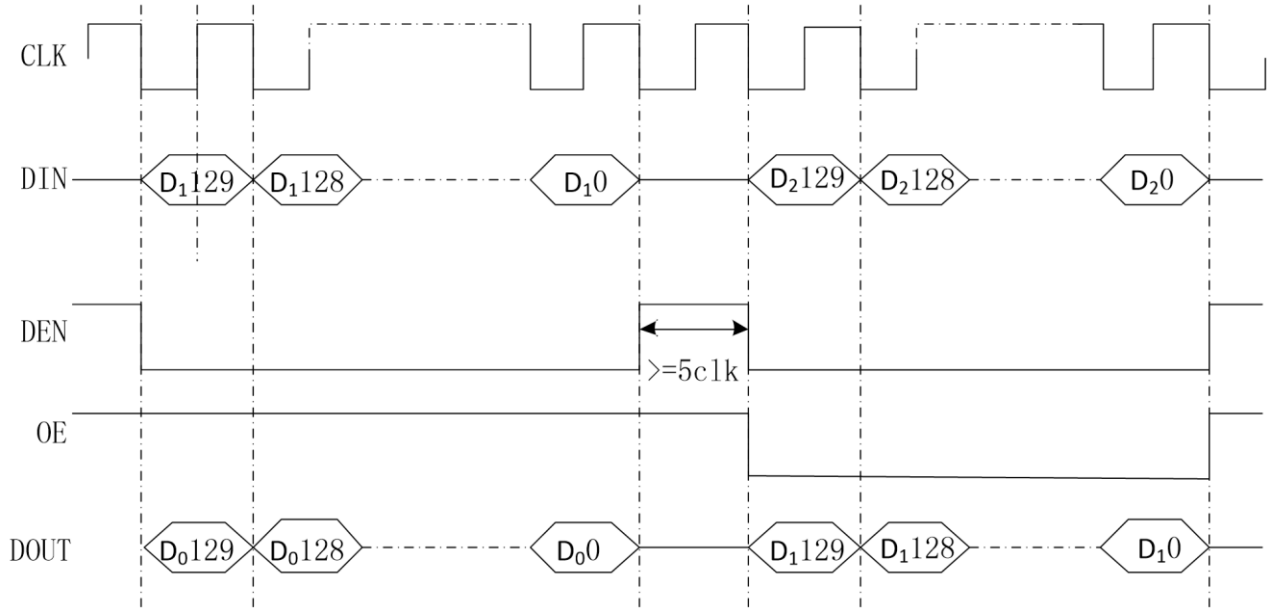

Figure 25. Serial data output timing

When continuous input is performed, pull OE low, and DOUT will output the 130-bit data of the last input in sequence, which can be used in chip cascading scenarios.

8.3. Typical Application and Assembly Schematics

The chip is packaged in plastic QFN with 76 pins and a chip size of 9×9mm. COM, Rn and Tn are all RF signal ports.

50 ohm transmission line connection, the RF signal port does not require an off-chip DC blocking capacitor.

The power supply voltage of this chip is 3.3V. When used, place a 0.1uF chip capacitor to ground near the chip VDD33 pin. In addition, this four-channel chip requires at least 100uF tantalum capacitor filtering to reduce the fluctuation of the chip power supply voltage during pulse switching. Pins 25-37 are wave control input and output ports. When the chip is working, the power supply port VDD33 must be powered on first, and then the wave control I/O port control signal must be given.

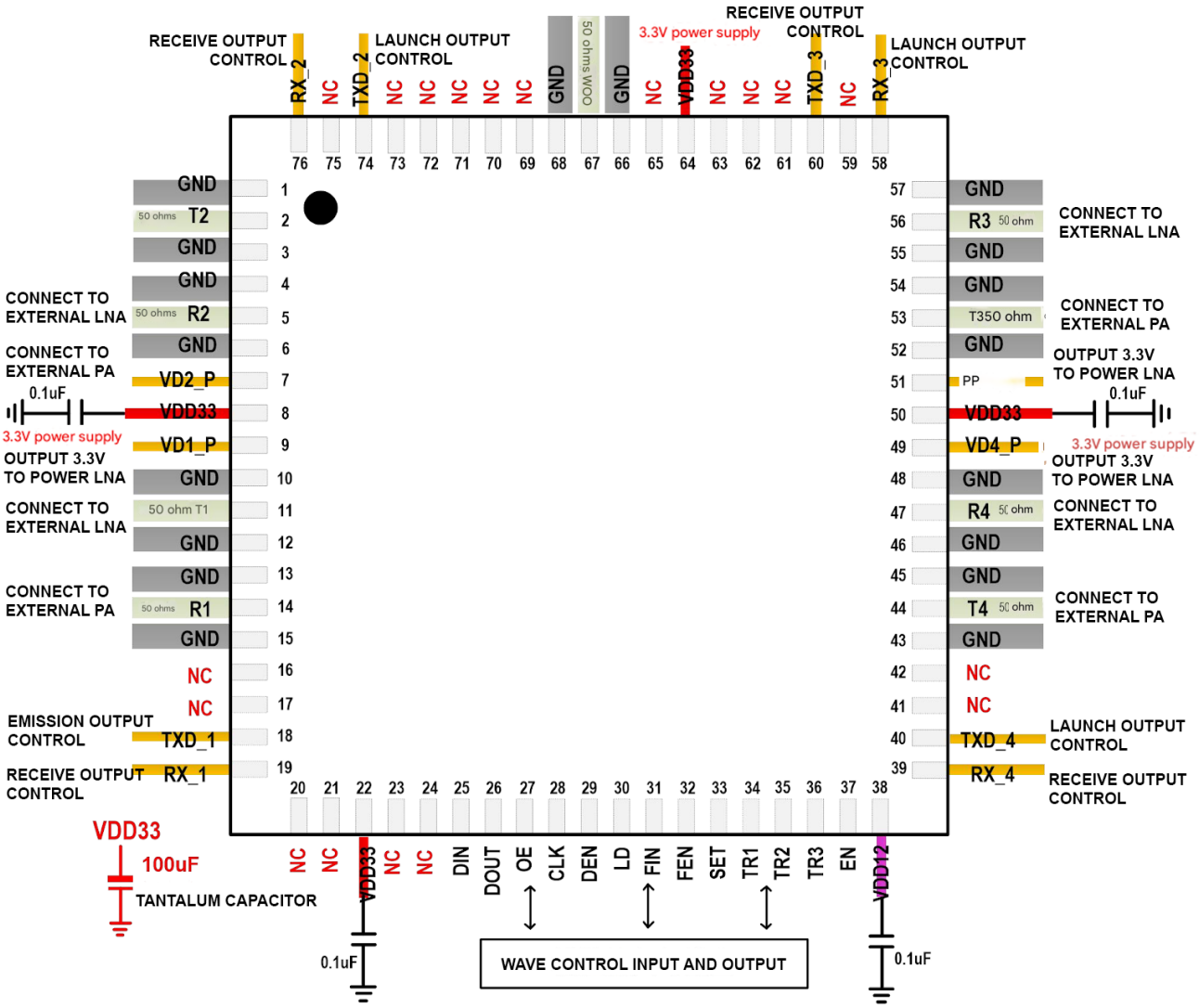

Figure 26. Typical application and assembly diagram

IX. Packaging Solutions

The chip adopts QFN76 pin package with a size of 9mm×9mm. The detailed size information is shown in the figure below.

The metal on the back of the chip after packaging is the ground terminal of the DC and AC signals of the entire chip and the main heat dissipation output terminal of the chip. It needs to be level with the ground on the board when used.

The surface has a fully ideal connection and good heat dissipation.

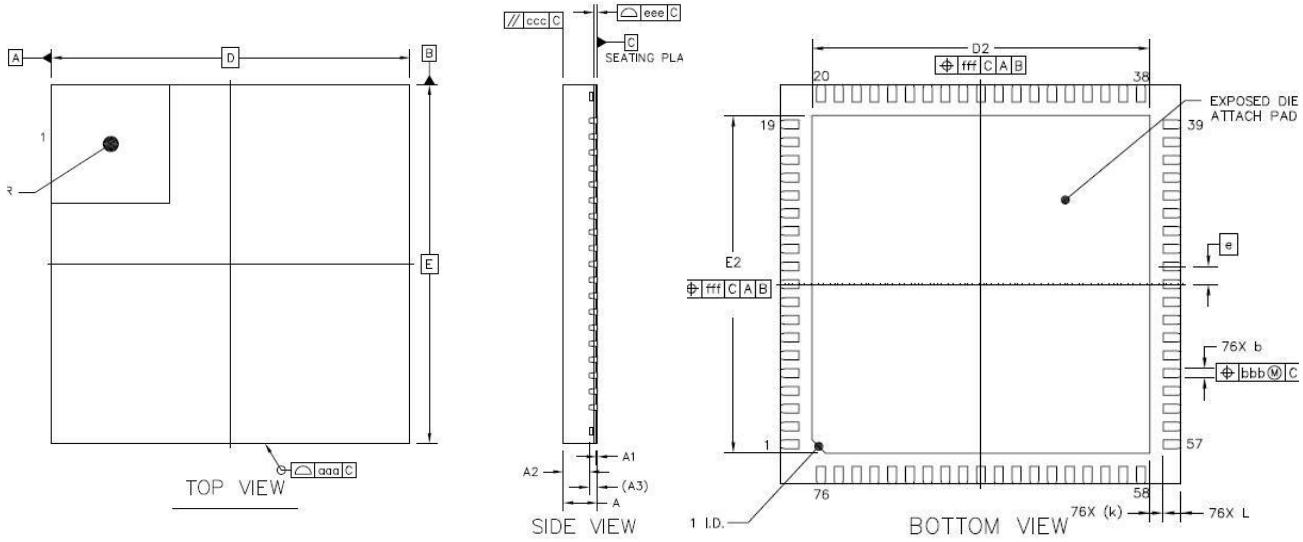

Figure 27. Package front view, side view, bottom view

Table 8. Package dimensions

DIMENSION SYMBOLS	VALUE (MM)		
	MINIMUM	NOMINAL	MAXIMUM
A	0.8	0.85	0.9
A1	0	0.02	0.05
A2	—	0.65	—
A3		0.203 REF	
b	0.15	0.20	0.25
D		9 BSC	
E		9 BSC	
e		0.4 BSC	
D2	7.6	7.7	7.8
E2	7.6	7.7	7.8
L	0.2	0.3	0.4
K		0.35 REF	
aaa		0.1	
ccc		0.1	
eee		0.08	
bbb		0.07	
fff		0.1	