

1 Product Overview

BST9739 14bit 2.5GSPS High performance RF DAC that can generate DC Up to 3GHz The DAC core uses a four-phase switching structure to provide outstanding low-distortion performance and industry-leading direct RF output capability. When the chip works in baseband mode, it can generate multi-carrier signals within the first Nyquist frequency, and when working in mixing mode, it can output multi-carrier signals in the second and third Nyquist intervals. The output current can be configured from 8.66mA to 31.66mA.

The on-chip controller greatly simplifies system integration. The chip has a dual-ended, source-synchronous LVDS interface, thus simplifying the integration with FPGA/ASIC The on-chip controller manages the internal and external clock domain interfaces over a wide temperature range, ensuring that data is transmitted from the host to the DAC. The multi-chip synchronization function is realized by the on-chip synchronization controller. The chip is configured and registers are accessed through the serial peripheral interface (SPI).

BST9739 Using 0.18μm CMOS Process implementation, working at 1.8V and 3.3V Dual power supply. Package adopts 160 foot

BGA Plastic packaging to reduce packaging parasitic parameters and be compatible with foreign products.

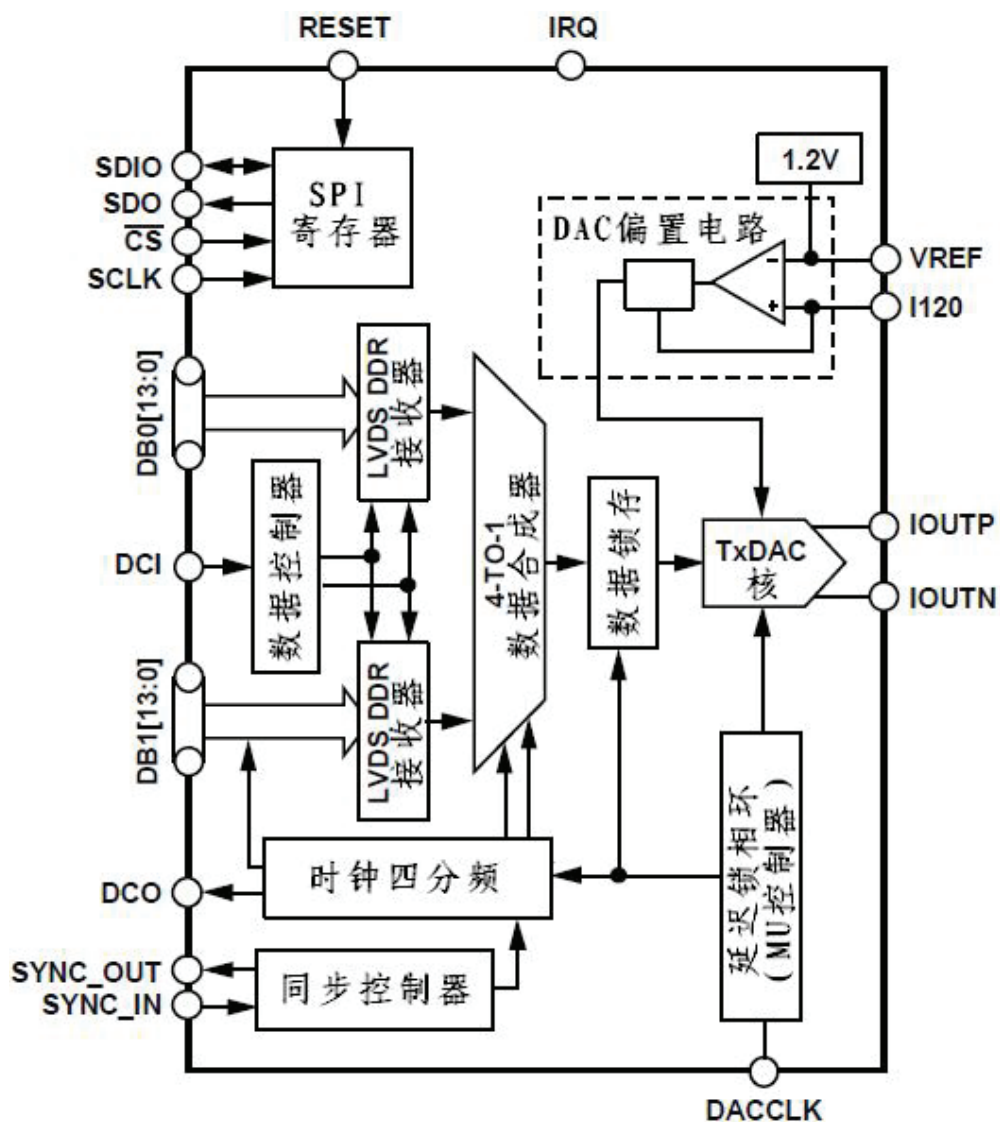
2 Features

- Resolution: 14 Bit
- Supply voltage: 3.3V, 1.8V Dual power supply
- Output range: 8.66mA ~ 31.66mA
- Differential nonlinearity: $\leq \pm 0.8\text{LSB}$
- Integral nonlinearity: $\leq \pm 1.3\text{LSB}$
- Spurious Free Dynamic Range: 69.5dBc (100MHz@2.4GSPS Typical value)
- Power consumption: 1.2W@2.5GSPS
- Quality grade: QJB, refer to GJB7400-2011 N class
- Operating temperature range: -55 ~ + 105°C

3 Corresponding to the situation of replacing foreign products

BST9739 With ADI The company's AD9739 The circuits are compatible and can be plugged in and used as a replacement

4 Circuit Function Block Diagram



Functional Block Diagram

5 Electrical characteristics parameters

DC Performance Specifications

VDDA = VDD33 = 3.3 V, VDDC = VDD = 1.8 V, IOUTFS = 20 mA.

Table 1.

parameter	Minimum	Typical Value	Maximum	unit
Resolution		14		Bit
Accuracy				
Integral Nonlinearity (INL)		±1.3		LSB
Differential Nonlinearity (DNL)		±1.3		LSB
Analog Output				
Gain Error (Using Internal Reference)		5.5		%
Full scale output current	8.66	20.2	31.66	mA
Output voltage range	-1		1	V
Common mode output impedance		10		MΩ
Differential output impedance		70		Ω
Output Capacitor		1		pF
DAC Clock input (DACCLK_P, DACCLK_N)				
Differential Peak-to-Peak	1.2	1.6	2	V
Common mode voltage		900		mV
DAC Clock rate	0.8		2.5	GHz
Temperature Drift				
Gain		60		ppm/°C
Reference voltage		20		ppm/°C
Reference Benchmark				
External reference voltage	1.15	1.2	1.25	V
Output Impedance		5		kΩ
Analog supply voltage				
VDDA	3.1	3.3	3.5	V
VDDC	1.7	1.8	1.9	V
Digital supply voltage				
VDD33	3.1	3.3	3.5	V
VDD	1.7	1.8	1.9	V
Supply Current and Power Dissipation, 2.0GSPS				
I _{VDDA}		37	38	mA
I _{VDDC}		159	166	mA
I _{VDD33}		34	37	mA
I _{VDD}		233	238	mA
Power consumption		0.94	0.976	W
Sleep mode, I _{VDDA}		2.5	2.75	mA
Power-down mode (register 0x01=0x03, 0x02=0x80)		0.02		mA
I _{VDDA}		3.8		mA
I _{VDDC}		0.5		mA
I _{VDD33}		0.1		mA
I _{VDD}				
Supply Current and Power Dissipation, 2.5GSPS				
I _{VDDA}		223		mA
I _{VDDC}		34		mA
I _{VDD33}		290		mA
I _{VDD}		1.16		W
Power consumption		0.02		mA

LVDS digital performance indicators

VDDA = VDD33 = 3.3 V, VDDC = VDD = 1.8 V, IOUTFS = 20 mA. Unless otherwise specified, the LVDS driver and receiver are IEEE Standard 1596.3-1996.

Table 2.

parameter	Minimum	Typical Value	Maximum	unit
LVDS Data input (DB0[13:0], DB1[13:0])¹				
Input common-mode voltage range, V_{COM}	825		1575	mV
Differential Input Logic High Threshold, V_{IH_DTH}	175	400		mV
Differential Input Logic Low Threshold, V_{IL_DTH}	-175	-400		mV
Receiver differential input impedance, R_{IN}	80		120	Ω
Input Capacitance		1.2		pF
LVDS Input rate	1250			MSPS
LVDS Minimum data valid period, t_{VALID}			344	ps
LVDS Clock Input (DCI and SYNC_IN)²				
Input common-mode voltage range, V_{COM}	825		1575	mV
Differential Input Logic High Threshold, V_{IH_DTH}	175	400		mV
Differential Input Logic Low Threshold, V_{IL_DTH}	-175	-400		mV
Receiver differential input impedance, R_{IN}	80		120	Ω
Input Capacitance		1.2		pF
Maximum clock rate	625			MHz
VDS Clock output (DCO and SYNC_OUT)³				
Output voltage high level (x_P or x_N)			1375	mV
Output voltage low level (x_P or x_N)	1025			mV
Output differential voltage, $ V_{OD} $	150	200	250	mV
Output offset voltage, V_{OS}	1150		1250	mV
Output impedance, single-ended, R_O	80	100	120	Ω
R O Single-ended mismatch			10	%
Maximum clock rate	625			MHz

Serial port performance indicators

VDDA = VDD33 = 3.3 V, VDDC = VDD = 1.8 V.

Table 3.

parameter	Minimum	Typical Value	Maximum	unit
Write Operation (See Figure 36)				
SCLK Clock rate, f_{SCLK} (or t_{SCLK})			20	MHz
SCLK Clock High, t_{HI}	18			ns
SCLK Clock High, t_{LOW}	18			ns
SDIO to SCLK Settling time, t_{DS}	2			ns
SCLK to SDIO Hold time, t_{DH}	1			ns
CS to SCLK Settling time, t_{S}	3			ns
SCLK To CS hold time, t_{H}	2			ns
Write operation (see Figure 37 and Figure 38)				
SCLK Clock rate, f_{SCLK} (or t_{SCLK})			20	MHz
SCLK Clock High, t_{HI}	18			ns
SCLK Clock low, t_{LOW}	18			ns
SDIO to SCLK Settling time, t_{DS}	2			ns
SCLK to SDIO Hold time, t_{DH}	1			ns
CS to SCLK Settling time, t_{S}	3			ns
SCLK To SDIO (or SDO) data valid time, t_{DV}			15	ns
CS to SDIO (or SDO) to High-Z Effective output, t_{EZ}		2		ns
Input (SDIO, SCLK, CS)				
Input high level voltage, V_{IH}	2	3.3		V
Input low level voltage, V_{IL}		0	0.8	V
Input high level current, I_{IH}	-10		10	μA
Input Low Level Current, I_{IL}	-10		10	μA
Output (SDIO)				
Output high level voltage, V_{OH}	2.4			V
Output low level voltage, V_{OL}	0		3.5	V
Output high level current, I_{OH}		4	0.4	mA
Output low level current, I_{OL}		4		mA

AC Performance Index

VDDA = VDD33 = 3.3 V, VDDC = VDD = 1.8 V, IOUTFS = 20 mA, fDAC = 2400 MSPS.

Table 4.

parameter	Minimum	Typical	Maximum	unit
Dynamic performance				
DAC Clock rate	800	2500		MSPS
Adjustable DAC Update rate range 4	800	2500		MSPS
Output stabilization time (tst) to 0.1 %		13		ns
Spurious Free Dynamic Range (SFDR)				
fOUT = 100MHz		69.5		dBc
fOUT = 350MHz		58.5		dBc
fOUT = 550MHz		54		dBc
fOUT = 950MHz		60		dBc
Two - tone signal intermodulation distortion (IMD), fOUT2 = fOUT1 +1.25 MHz				
fOUT = 100MHz		94		dBc
fOUT = 350MHz		78		dBc
fOUT = 550MHz		72		dBc
fOUT = 950MHz		68		dBc
Noise spectral density (NSD), 0dBFS Single tone signal				
fOUT = 100MHz		-166		dBm/Hz
fOUT = 350MHz		-161		dBm/Hz
fOUT = 550MHz		-160		dBm/Hz
fOUT = 850MHz		-160		dBm/Hz
WCDMA ACLR (single carrier), adjacent / alternate adjacent channels				
fDAC =2457.6MSPS, fOUT = 350MHz		80/80		dBc
fDAC =2457.6MSPS, fOUT = 950MHz		78/79		dBc
fDAC =2457.6MSPS, fOUT = 1700MHz (Mixed Mode)		74/74		dBc
fDAC =2457.6MSPS, fOUT = 2100MHz (Mixed Mode)		69/72		dBc