BST9643

Analog-to-Digital Converter Product Manual

Ver1.0

Product overview

The BST9643-250 is a dual-channel, 14-bit, 250 MSPS analog-to-digital converter (ADC) with a sampling rate of up to 250 MSPS. It is designed to support communications applications that require low cost, small size, wide bandwidth and versatility.

This dual-channel ADC core uses a multi-stage, differential pipeline architecture and integrates output error correction logic. Each ADC has a wide bandwidth input to support a variety of user-selectable input ranges; an integrated voltage reference simplifies design; and a duty cycle stabilizer can be used to compensate for fluctuation of the ADC clock duty cycle; gives the converter superior performance.

The ADC output data can be directly sent to the 14-bit parallel LVDS output port, and the output format is two optional modes: interleaved or channel multiplexing. In addition, the flexible power-down mode option can significantly save power consumption. The device is available in a 64-pin QFN package and operates over the −55°C to +125°C temperature range.

Product features

- Signal-to-Noise Ratio (SNR): 70 dBFS (fin=185 MHz@ 250 MSPS)
- Spurious Free Dynamic Range (SFDR): 83 dBc (fin=185 MHz@250 MSPS)
- -150 dBFS/Hz Input Noise (185 MHz -1 dBFS AIN@250 MSPS)
- Total power consumption: 1.10W @ 250 MSPS
- 1.8V single voltage supply
- LVDS (ANSI-644 level) output

- 1~8 integer input clock divider (625 MHz maximum frequency input)
- ADC internal reference voltage source
- Analog input range:1.4~2.0 Vpp (recommended value 1.75 Vpp)
- Built-in clock duty cycle stabilization module
- 90 dB channel-to-channel isolation/crosstalk suppression
- SPI serial port control
- Energy-saving power-down mode
- User-configurable built-in self-test (BIST) function

Functional Block Diagram

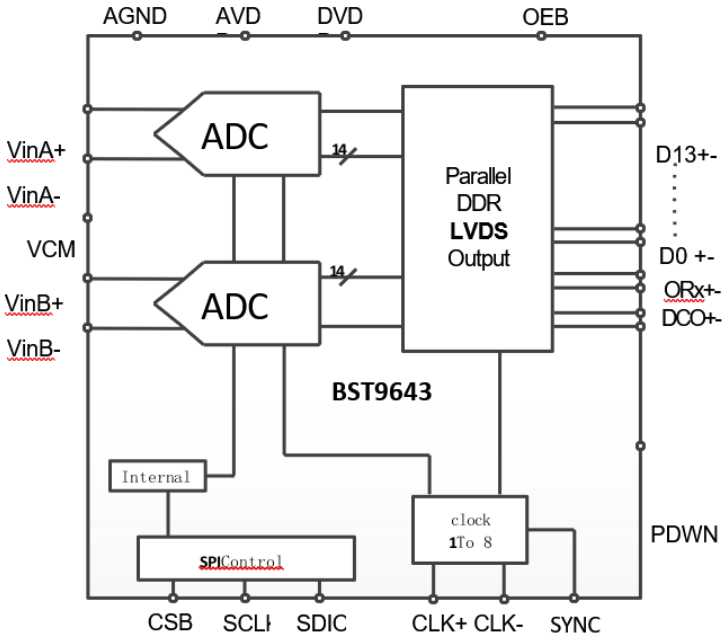

Figure 1. BST9643 functional block diagram

Electrical Parameters

Unless otherwise specified, the general test conditions are AVDD = 1.8V, DRVDD = 1.8V, VIN = −1.0dBFS differential input,1.75 Vpp input range, DCS is turned on.

Table 1.

Parameter	Temperature	BST9643-250 Minimum	Typical Value	Maximum	Unit
Resolution	Complete		14		Bit
Accuracy					
No missing codes	Complete		ensure		
Offset Error	Complete		±10		mV
Gain Error	Complete		±4		%FSR
Differential Nonlinearity (DNL)	Complete		±0.8		LSB
	25°C		±0.3		LSB
Integral Nonlinearity (INL)	Complete		±3.5		LSB
	25°C		±2		LSB
Matching characteristics					
Offset Error	Complete		±13		mV
Gain Error	Complete		±3.5		%FSR
Temperature drift					
Offset Error	Complete		±5		ppm/°C
Gain Error	Complete		±100		ppm/°C
Input referred noise VREF=1.75V	25°C		1.29		LSB rms
Analog Input					
Input Range	Complete		1.75		Vp-p
Input Capacitance[2]	Complete		2.5		pF
Input resistance[3]	Complete		20		kΩ
Input common mode voltage	Complete		0.9		V
Supply voltage					
AVDD	Complete		1.7	1.8	V
DRVDD	Complete		1.9		V

Power consumption			
Sine wave input	Complete	1100	mW
Standby power consumption[4]	Complete	90	mW
Power-off power consumption	Complete	10	mW

[1] When measuring, input a low frequency full-scale sine wave

[2] Input capacitance refers to the capacitance between the positive and negative terminals of the input

[3] Input resistance refers to the equivalent resistance between the positive and negative terminals of the input

[4] Standby power consumption refers to the power consumption when the ADC input is DC and there is no signal on the clock pin. Note: "Full" refers to the temperature range of -55°C~+125°C (the same below)

Electrical Parameters

Unless otherwise specified, the general test conditions are AVDD = 1.8V, DRVDD = 1.8V, VIN = −1.0dBFS differential input,1.75 Vpp input range, DCS is turned on.

Table 2.

Parameter	Temperature	BST9643-250 Minimum Typical Value Maximum	Unit
Signal-to-Noise Ratio (SNR)			
fIN=30 MHz	25°C	71.0	dBFS
fIN=90 MHz	25°C	70.5	dBFS
fIN= 140 MHz	25°C	70.3	dBFS
fIN= 185 MHz	25°C	70.0	dBFS
fIN= 220 MHz	25°C	69.0	dBFS

Signal-to-Noise/Distortion Ratio (SINAD)			
fIN= 30 MHz	25°C	69.0	dBFS
fIN= 90 MHz	25°C	68.8	dBFS
fIN= 140 MHz	25°C	68.6	dBFS
fIN= 185 MHz	25°C	68.2	dBFS
fIN= 220 MHz	25°C	68.0	dBFS
Effective Number of Bits (ENOB)			
fIN= 30 MHz	25°C	11.2	Bits
fIN= 90 MHz	25°C	11.1	Bits
fIN= 140 MHz	25°C	11.1	Bits
fIN= 185 MHz	25°C	11.0	Bits
fIN= 220 MHz	25°C	11.0	Bits

Spurious Free Dynamic Range (SFDR)			
fIN= 30 MHz	25°C	90	dBc
fIN= 90 MHz	25°C	87	dBc
fIN= 140 MHz	25°C	85	dBc
fIN= 185 MHz	25°C	83	dBc
fIN= 220 MHz	25°C	83	dBc
Two-tone spurious-free dynamic range (SFDR) fIN=184.12MHz(-7 dBFS), 187.12 (-7 dBFS)	25°C	85	dBc
Crosstalk between channels (100MHz IF input hour)	Complete	90	dB
Full Power Bandwidth	25°C	600	MHz

Numeric parameters

Unless otherwise specified, the general test conditions are AVDD = 1.8V, DRVDD = 1.8V, VIN = −1.0dBFS differential input,1.75 Vpp full scale.

Table 3.

Parameter	Temperature	Minimum	Typical Value	Maximum	Unit
Differential clock input (CLK+, CLK-)					
Logic Compatibility	Complete	CMOS/LVDS/LVPECL			
Internal common mode bias	Complete		0.9		V
Differential input voltage	Complete	0.3		3.6	V p p
Input voltage range	Complete	AGND		AVDD	V
Input common mode range	Complete	0.9		1.4	V
High level input current	Complete	10		22	μA
Low level input current	Complete	-22		-10	μA
Input Capacitance	Complete		4		pF
Input resistance	Complete	8	10	12	kΩ
Sync Input					
Logic Compatibility	Complete		CMOS/LVDS		
Internal bias	Complete		0.9		V
Input voltage range	Complete	AGND		AVDD	V
High level input voltage	Complete	1.2		AVDD	V
Low level input voltage	Complete	AGND		0.6	V
High level input current	Complete	-5		+5	μA
Low level input current	Complete	-5		+5	μA
Input Capacitance	Complete		1		pF
Input resistance	Complete	12	16	20	kΩ
Logic Input (CSB)[1]					
High level input voltage	Complete	1.22		2.1	V
Low level input voltage	Complete	0		0.6	V
High level input current	Complete	-5		+5	μA
Low level input current	Complete	-80		+45	μA
Input resistance	Complete		26		kΩ
Input Capacitance	Complete		2		pF
Logic Input (SCLK)[2]					
High level input voltage	Complete	1.22		2.1	V

Low level input voltage	Complete	0		0.6	V
High level input current	Complete	45		70	µA
Low level input current	Complete	-5		+5	µA
Input resistance	Complete		26		kΩ
Input Capacitance	Complete		2		pF
Logic Input (SDIO)[1]					
High level input voltage	Complete	1.22		2.1	V
Low level input voltage	Complete	0		0.6	V
High level input current	Complete	45		70	µA
Low level input current	Complete	-5		+5	µA
Input resistance	Complete		26		kΩ
Input Capacitance	Complete		5		pF
Logic input (OEB, PDWN)[2]					
High level input voltage	Complete	1.22		2.1	V
Low level input voltage	Complete	0		0.6	V
High level input current	Complete	45		70	µA
Low level input current	Complete	-5		+5	µA
Input resistance	Complete		26		kΩ
Input Capacitance	Complete		5		pF
Digital Output					
LVDS data and OR output					
Differential Output Voltage (VOD), ANSI mode	Complete	250	350	450	mV
Output offset voltage (VOS), ANSI mode	Complete	1.15	1.22	1.35	V
Differential Output Voltage (VOD), small swing mode	Complete	150	200	280	mV
Output offset voltage (VOS), small swing mode	Complete	1.15	1.22	1.35	V

Switch parameters

Table 4.

Parameter	Temperature	BST9643-250			Unit
		Minimum	Typical Value	Maximum	
Clock Input					
Input clock rate	Complete			625	MHz
Sampling rate	Complete	40		250	Msps
CLK Period – Divide by 1 Mode	Complete	4			ns
Clock high pulse width high (tCH)					
Divide by 1 mode, DCS enabled	Complete	1.8	2.0	2.2	ns
Except 1 mode, DCS off	Complete	1.9	2.0	2.1	ns
Remove2 to Divide by 8 Mode	Complete	0.8			
			1.0		ns ns
Aperture delay (tA) Aperture jitter (tJ)	All		0.12		ps rms
Data output parameters					
LVDS Mode					
Data transmission delay (tPD)	Complete		6.0		ns
DCO propagation delay (tDCO)	Complete		6.7		ns
DCO to Data Skew (tSKEW)	Complete	0.4	0.7	1.0	ns
Pipeline Delay	Complete		10		cycle
Aperture delay (tA)	Complete		1.0		ns
Aperture jitter (tJ)	Complete		0.1		ps rms
Sleep wake-up time	Complete		10		us
Power-off wake-up time	Complete		250		us
Overload recovery time	Complete		3		cycle

Timing parameters

Table 5.

Parameter	Condition	Minimum	Typical Value	Maximum	Unit
Synchronous timing requirements					
tSSYNC	SYNC to CLK rising edge setup time	1	0.3		ns
tHSYNC	SYNC to CLK rising edge hold time	1	0.4		ns
SPI Timing Requirements					
tDS	Setup time between data and SCLK rising edge		2		ns
tD	Hold time between data and SCLK rising edge		2		ns
tCLK	SCLK period		40		ns
tS	Setup time between CSB and SCLK		2		ns
tH	Hold time between CSB and SCLK		2		ns
tHIGH	Minimum time that SCLK is in high logic state		10		ns
tLOW	The minimum time that SCLK is in the low logic state		10		ns
tEN_SDIO tDIS_SDIO	When SDIO changes from input to output, the time required relative to the falling edge of SCLK When SDIO changes from input to output, the time required relative to the rising edge of SCLK		10 10		ns ns

Ordering Information

Product Model	Packaging materials	Package	Quality Grade	Detailed specification number
BST9643EQFN64	plastic	QFN64	Military Temperature	Q/ BST 20424-2018