

BST9361

RF Agile Transceiver

Data Sheet

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I. General Description

BST9361 is a high-integration radio frequency (RF) transceiver applied to communication base stations, signal chain, etc. It integrates the RF, mixed signal, and digital modules required for a transceiver on a single chip. It has a wide operating frequency range (transmitter: 47 MHz - 6 GHz, receiver: 70 MHz - 6 GHz) and supports a large channel bandwidth (<200 kHz - 56 MHz). Its programmable characteristics make it suitable for time division duplex (TDD) and frequency division duplex (FDD) communication modes. The on-chip PLL has a frequency-hopping function, which can complete a single-time local oscillator frequency switch at 100 us intervals. It adopts a single-end CMOS or differential LVDS digital interface to connect with various baseband processors (BBP).

The receiver section is equipped with automatic gain control (AGC) and manual gain control (MGC) functions. The transmitter section is equipped with a high-precision power monitor. This chip also has a self-calibration function. As a result, this chip can maintain high performance under various temperature and input signal conditions. In addition, the chip supports multiple

test modes, facilitating design debugging and radio optimization. BST9361 is packaged in a 10 mm×10 mm PBGA144.

II. Product Features

- RF 2×2 transceiver with integrated 12-bit DACs and ADCs
- TX band: 47 MHz to 6 GHz
- RX band: 70 MHz to 6 GHz
- Supports TDD and FDD operation
- Tunable channel bandwidth: <200 KHz to 56 MHz
- Dual receivers: 6 differential inputs or 12 single-ended input
- Receiver sensitivity: noise figure is 3 dB
- RX gain control: automatic gain control (AGC), manual gain control (MGC)
- Dual transmitters: 4 differential outputs
- Highly linear broadband transmitter: TX EVM≤-40dB, TX noise ≤-150dBm/Hz, TX monitor ≥66dB dynamic range with 1 dB accuracy
- Integrated fractional-N synthesizer; the on-chip PLL supports frequency-hopping function
- Supports Multichip synchronization
- Integrates CMOS/LVDS digital interfaces

III. Functional Block Diagram

The functional block diagram of the BST9361 is shown in Figure 1. Its typical application scenarios include point to point communication systems, general-purpose radio systems, and various cellular base stations.

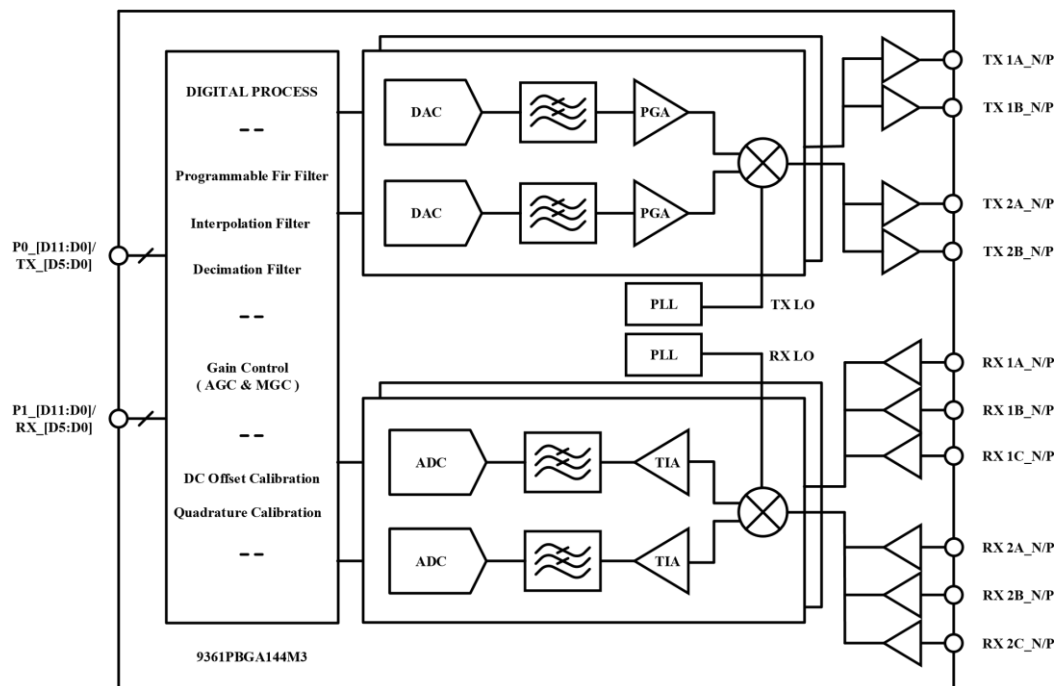


Figure 1. Functional Block Diagram

IV. Packaging Information

4.1. Packaging and Pin Information

BST9361 adopts PBGA144 packaging. The outline dimensions is shown in Figure 2.

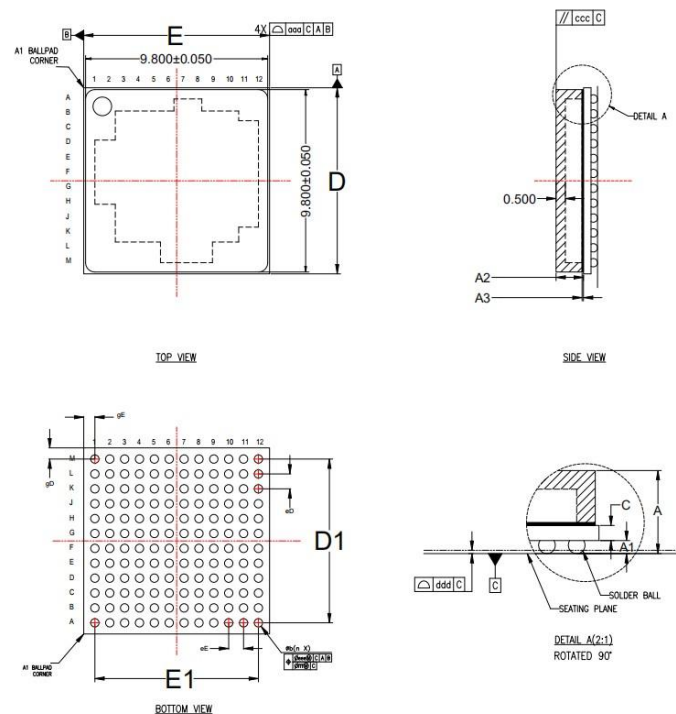


Figure 2. Outline Dimensions

Table 1

DIMENSION SYMBOL	NUMERICAL VALUE, UNIT: MILLIMETRE		
	Minimum	Nominal Value	Maximum
Total Thickness (A)	2.131	2.231	2.331
Substrate Thickness (C)	0.366	0.406	0.446
Ball Stand Off (A1)	0.300	0.350	0.400
Top of PKG To Substrate (A2)	1.475REF		
Glue Thickness (A3)	0.075REF		
Ball Width (b)	0.400	0.450	0.500
Body Size (D/E)	9.900	10.000	10.100
Edge Ball Center to Center (D1/E1)	8.800		
Ball Pitch (eD/eE)	0.800		
Edge Ball Center to Package Edge (gD/gE)	0.600		

BST9361 pin layout diagram is shown in Figure 3.

	1	2	3	4	5	6	7	8	9	10	11	12
A	RX2A_N	RX2A_P	NC	VSSA	TX_MON 2	VSSA	TX2A_N	TX2A_P	TX2B_N	TX2B_P	VDDAIP1 TX_VCO	TX_EXT LO_IN
B	VSSA	VSSA	AUXDAC1	GPO_3	GPO_2	GPO_1	GPO_0	VDD_GP O	VDDAIP3 TX_LO	VDDAIP3 TX_VCO LDO	TX_VCO LDO_OUT	VSSA
C	RX2C_P	VSSA	AUXDAC2	TEST/EN ABLE	CTRL_IN 0	CTRL_IN 1	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
D	RX2C_N	VDDAIP3 RX_RF	VDDAIP3 RX_TX	CTRL_OUT T0	CTRL_IN 3	CTRL_IN 2	P0_D9/TX D4_P	P0_D7/TX D3_P	P0_D5/TX D2_P	P0_D3/TX D1_P	P0_D1/TX D0_P	VSSD
E	RX2B_P	VDDAIP3 RX_LO	VDDAIP3 TX_LO BUFFER	CTRL_OUT T1	CTRL_OUT T2	CTRL_OUT T3	P0_D11/T X_D5_P	P0_D8/TX D4_N	P0_D6/TX D3_N	P0_D4/TX D2_N	P0_D2/TX D1_N	P0_D0/TX D0_N
F	RX2B_N	VDDAIP3 RX_VCO LDO	VSSA	CTRL_OUT T6	CTRL_OUT T5	CTRL_OUT T4	VSSD	P0_D10/T X_D5_N	VSSD	FB_CLK P	VSSD	VDDIP3 DIG
G	RX_EXT LO_IN	RX_VCO LDO_OUT	VDDAIP1 RX_VCO	CTRL_OUT T7	EN_AGC	ENABLE	RX_FRAM E_N	RX_FRAM E_P	TX_FRAM E_P	FB_CLK N	DATA_CLK P	VSSD
H	RX1B_P	VSSA	VSSA	TXNRX	SYNC_IN	VSSA	VSSD	P1_D11/R X_D5_P	TX_FRAM E_N	VSSD	DATA_CLK N	VDD_INT ERFACE
J	RX1B_N	VSSA	VDDAIP3 RX_SYN TH	SPI_DI	SPI_CLK	CLK_OUT T	P1_D10/R X_D5_N	P1_D9/RX D4_P	P1_D7/RX D3_P	P1_D5/RX D2_P	P1_D3/RX D1_P	P1_D1/RX D0_P
K	RX1C_P	VSSA	VDDAIP3 TX_SYN TH	VDDAIP3 _BB	RESETB	SPI_ENB	P1_D8/RX D4_N	P1_D6/RX D3_N	P1_D4/RX D2_N	P1_D2/RX D1_N	P1_D0/RX D0_N	VSSD
L	RX1C_N	VSSA	VSSA	RBIAS	AUXADC	SPI_DO	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
M	RX1A_P	RX1A_N	NC	VSSA	TX_MON 1	VSSA	TX1A_P	TX1A_N	TX1B_P	TX1B_N	XTALP	XTALN

Figure 3. Pin Layout Diagram

V. Electrical Characteristics

5.1. Technical Specifications

Unless otherwise noted, VDD_INTERFACE = VDD_GPO = 1.8V, VDDD1P3_DIG = 1.3V, and all VDDA1P3_x pins = 1.3V, temperature = ambient temperature.

Table 2. Specifications

PARAMETER	BST9361			UNIT
	Min	Typ	Max	
Receivers				
Center Frequency	70		6000	MHz
Minimum Gain		70		dB
Noise Figure (NF)		3		dB
Third-Order Input Intermodulation Intercept Point under Minimum Gain (IIP3)		-18		dBm
Second-Order Input Intermodulation Intercept Point under Minimum Gain (IIP2)		45		dBm
Local Oscillator (LO) Leakage		-120		dBm
Modulation Accuracy (EVM)		-40		dB
Input S11		-10		dB
Transmitters				
Center Frequency	47		6000	MHz
Power Control Range		90		dB
Power Control Accuracy		0.25		dB
Maximum Output Power		7.5		dBm
Noise Floor		-150		dBm/Hz
Third-Order Output Intermodulation Intercept Point (OIP3)		19		dBm
Carrier Leakage		-50		dBc
Modulation Accuracy (EVM)		-40		dB
Output S22		-10		dB

5.2. Performance Testing

Test conditions: VDD_INTERFACE = VDD_GPO = 1.8V, VDDD1P3_DIG = 1.3V, and all VDDA1P3_x pins = 1.3V.

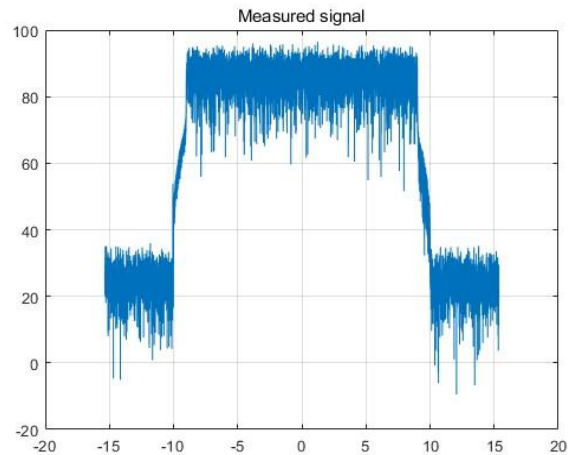


Figure 4. RX LTE20M Test Result (Spectrum Diagram)

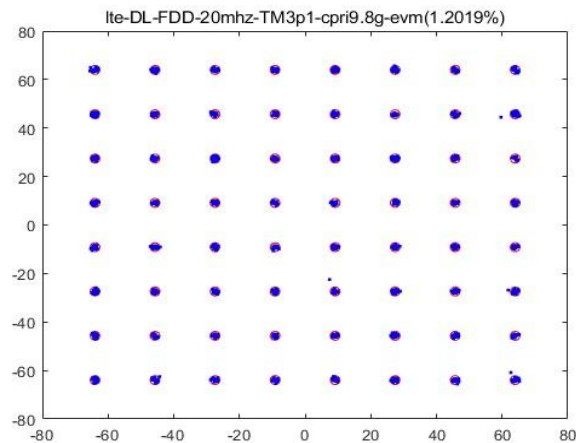


Figure 5. RX LTE20M Test Result (constellation diagram, EVM = -40 dB)

VI. Ordering Information

Table 3. Ordering Information

MODEL	PACKAGE TYPE	PACKAGE MATERIAL	QUALITY ASSURANCE LEVEL	PIN MATERIAL	WEIGHT	DETAILED SPECIFICATION
BST9361	PBGA144	Plastic seal	N1 level	Sn63Pb37	-	-

Notes:

1. N/N1 devices meet the screening requirements of GJB 7400A <General Specification for Semiconductor Integrated Circuits for Certification by Qualified Manufacturer> at level N/N1.
2. The product ordering information is our existing products or devices determined to develop, and according to user needs, we can develop other packaging forms of devices.