BST860-A

1. Product Overview

BST860-A is an ultra-low noise, high PSRR, four- channel low dropout linear regulator. It can provide a total of 205mA maximum drive current. The output voltage can be adjusted from 2.5V to 5.2V and has an enable control input.

2. Features

- Ultra-low noise:
- 3 nV/√ Hz @10KHz 7 nV /√Hz @ 1 KHz;
- Integrated RMS noise: 1.5μ Vrms @ 10-100KHz.
- Four channels with adjustable output voltage:
- VR1: 75 mA @ 2.5 V to 5.5 V;
- VR2&VR3: 15mA @ 2.5V to 5.2V;
- VR4: 100mA @ 2.5V to 5.2V.
- Thermal protection function.
- Low shutdown current: <5uA (typically <1uA).
- Power supply rejection PSRR: 8 0dB@10KHZ.
- 3mm × 3mm × 0.9mm, QFN1 6 package.

3. Product appearance

The device adopts 16-pin PQFN package, and its dimensions refer to GB/T 7092-1993. The shell shape is shown in Figure 1.

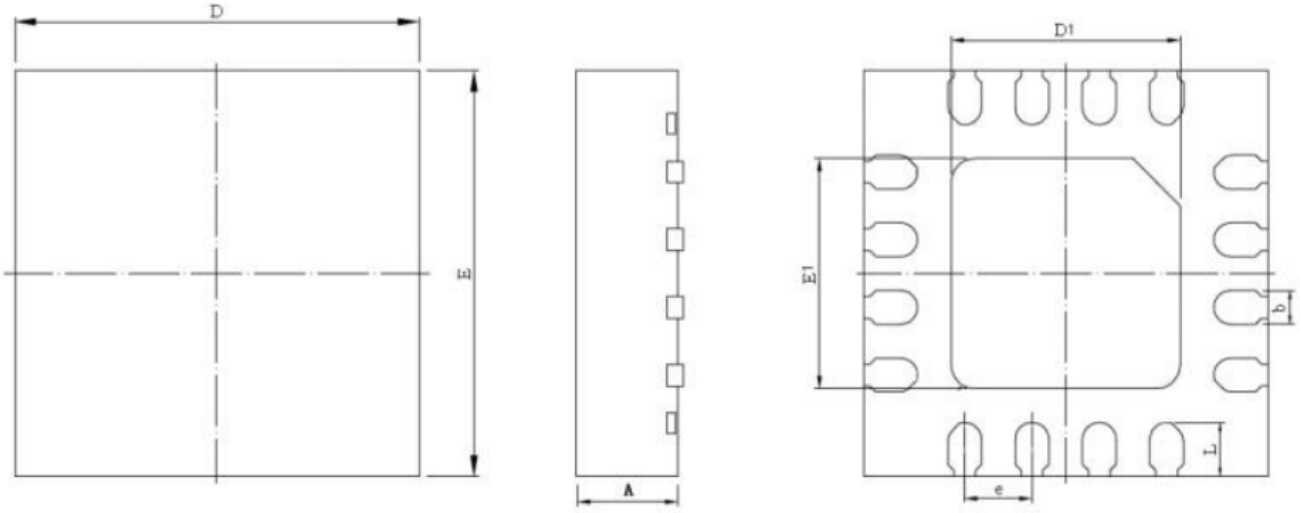

Figure 1. Package outline

Table 1. BST860-A package parameters (Unit is mm)

Dimension symbols	Numeric		
	Minimum	Nominal	maximum
D	2.80	—	3.20
E	2.80	—	3.20
D1	1.50	—	1.90
E1	1.50	—	1.90
e	—	0.50	—
b	0.14	—	0.30
L	0.22	—	0.38
A	0.50	—	0.90

4. Electrical parameters

Table 2. BST860-A electrical parameter characteristics

characteristic	symbol	strip Item Unless otherwise specified *VDD* = 5.5 V -5 5 °C ≤ T_A ≤12 5 °C	Limit value			unit
			Minimum	typical	maximum	
All channel output voltage	V_{OUTA}		2.5	—	5.2	V
VR1 foot (first channel) output voltage	V_{OUT1}	I_{OUT1} =75mA	2.95	3. 1	3.15	V
VR2 pin (second path) output voltage	V_{OUT2}	I_{OUT2} =15mA	2.95	3. 1	3.15	V
VR3 pin (third channel) output voltage	V_{OUT3}	I_{OUT3} =15mA	2.95	3. 1	3.15	V
VR4 pin (fourth path) output voltage	V_{OUT4}	I_{OUT4} =100mA	4. 35	4. 5	4.65	V
Input voltage range	V_{IN}		4.8	—	5.6	V
VR1 pin (first channel) output current	I_{OUT1}		—	—	75	mA
VR2 pin (second path) output current	I_{OUT2}		—	—	15	mA
VR3 pin (third channel) output current	I_{OUT3}		—	—	15	mA
VR4 pin (fourth path) output current	I_{OUT4}		—	—	10 0	mA
Total output current	I_{OUT1-4}		—	—	205	mA
Shutdown current	I_p	*VEN=0V*	—	—	5	μA
Enable input high level voltage	V_I		2	—	—	V
Enable input low level voltage	V_{IL}		—	—	0.8	V
Current Regulation (VR4)	$\triangle V_{OUT} / \triangle I_{OUT}$	0 μA to 100mA	—	—	0.1	%/mA
VR1 PSRR [a]	*PSRR*	1KHz , T_A =25°C	70	7 5		dB
Output noise voltage density [a]	ONVD	10kHz, T_A = 25°C	—	3	20	nV /√Hz
		1kHz, T_A = 25°C	—	7	40	
Opening time (VR1)	*t* start		—	—	50	ms
Enable turn-on delay time (VR1)	*ET*		—	—	50	ms

Notes: [a] Sampling at high and low temperatures 5 (0) is only performed for initial qualification or design changes