BST8412

1. Product Overview

The BST8412 is a quad, 12-bit voltage output DAC with readback capability.
Digital control allows the user to load or read back data from any DAC, loading any DAC and transmits data to all DACs at the same time.
RESET When active low, the BST2812 resets all DAC output registers to mid- scale.
The power supply voltage is 5V, the reference voltage is 2.5V, and the power consumption is less than 60mW.
BST8412 can be packaged in ceramic CLCC28 and has an operating temperature range of -55 to 125°C.

2. Product Features

- Power supply voltage 5V.
- Voltage output.
- Double buffered input.
- Output can be reset to mid-range.
- With readback function.
- Total dose ≥ 50Krad(Si).
- SEU LET Threshold ≥ 37MeV.cm²/m.

3. Functional Block Diagram

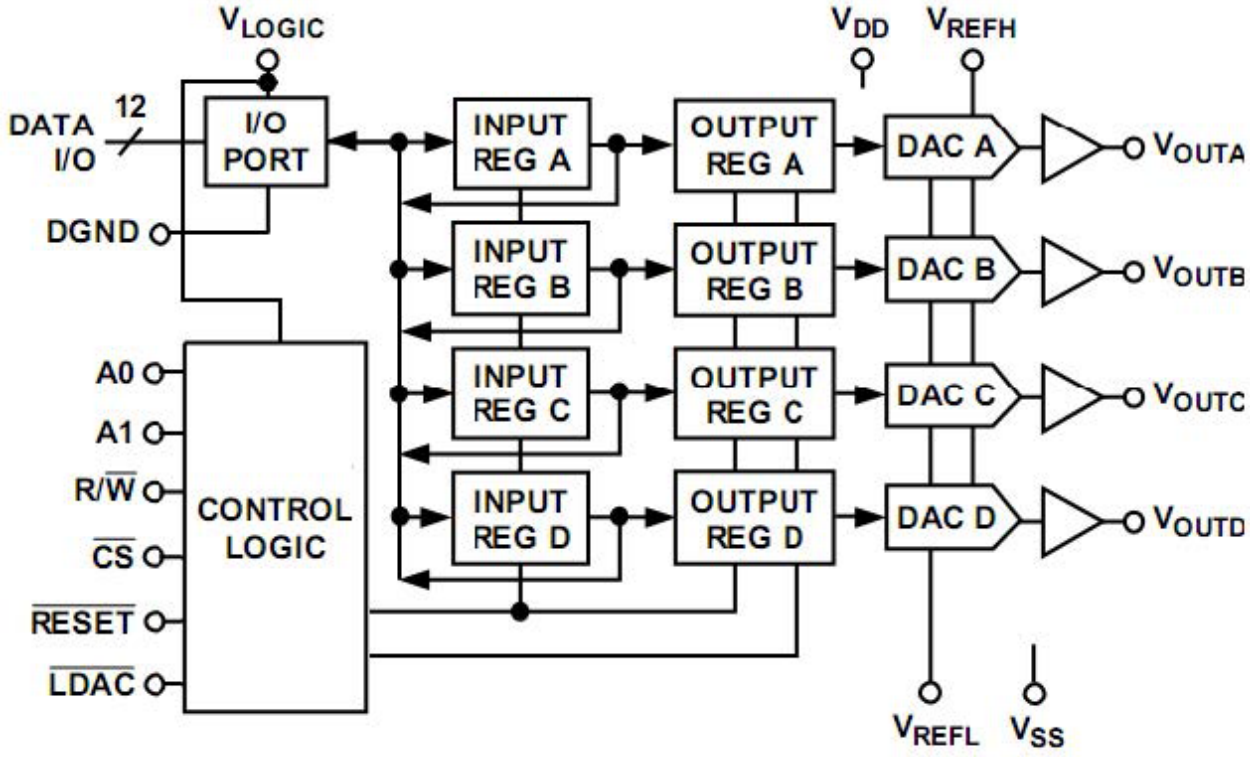

Figure 1. Functional Block Diagram

4. Electrical Parameters

Tabl 1. Unless otherwise specified, Tamb = 25 °C

Characteristic	Symbol	Condition Unless otherwise specified V_{DD} = V_{LOGIC} = 4.75V ~ 5.25V, V_{SS} = 0V, V_{REFH} =2.5V, V_{REFL} =0V- 55°C ≤ T_A ≤ 125°C	Limit value		Unit
			Minimum	maximum	
Integral nonlinearity error	INL	VDD = VLOGIC = 5.0V	—	±3	LSB
Differential nonlinearity error	DNL	VDD = VLOGIC = 5.0V	—	±2	LSB
Resolution	RES	VDD = VLOGIC = 5.0V	12	—	bit
Minimum span error	V_Z	VDD = VLOGIC = 5.0V	—	±20	LSB
Full scale error	V_F	VDD = VLOGIC = 5.0V	—	±20	LSB
Output voltage range	V_{OUT}	VDD = VLOGIC = 4.75 V	0	2.5	V
refer to					
Reference high level input current	I_{REF}	VDD = VLOGIC = 5.25V	- 1.0	1.0	mA
Amplifier Characteristics					
Output Current	I_{OUT}	R_L =2k Ω, C_L = 100pF, VDD = VLOGIC = 5.0V	- 1.25	1.25	mA
Logical parameters					
Logic input high level voltage	V_{INH}	VDD = VLOGIC = 5.0V	2.4	—	V
Logic input low level voltage	V_{INL}	VDD = VLOGIC = 5.0V	—	0.8	V
Logic output high voltage	V	I_{OH} =0.4mA, V DD = V LOGIC = 5.0V	2.4	—	V
Logic output low voltage	V_{OL}	I_{OL} = - 1.6mA, VDD = VLOGIC = 5.0V	—	0.45	V
Logic input current	I_{IN}	VDD = VLOGIC = 5.0V	—	1	μA
Power parameters					
Analog supply current	I_{DD}		—	12	mA
Digital supply voltage	V_{LOGIC}		—	5	V
Analog supply voltage	VDD		—	5	V
Build Time	t_{SUP}	VDD = VLOGIC = 5.0V	—	20	μS
Logic Timing Parameters (V_{DD} = V_{LOGIC} = 5.0V)					
Chip select write pulse width	t_{WCS}		150	—	ns
Write setup time	WS	tWCS = 150ns	0	—	ns
Write hold time	t_W	tWCS = 150ns	0	—	ns
Address creation time	t_{AS}		0	—	ns
Address hold time	tH		0	—	ns
Load build-up time	t_L		70	—	ns
Load holding time	t_H		50	—	ns
Write data setup time	t_{WDS}	tWCS = 150ns	20	—	ns
Write data retention time	WDJ	tWCS = 150ns	0	—	ns
Load data pulse width	tDW		180	—	ns
Reset pulse width	t_{RESET}		150	—	ns
Chip select read pulse width	RCS		170	—	ns
Read data hold time	dH	t RCS =170ns	20	—	ns
Reading settling time	t_{RDS}	t RCS =170ns	0	—	ns
Data to high impedance time	tD		—	200	ns
Chip select to data time	t_{CDS}		—	320	ns

5 Ordering Information

Table 2. Product Ordering Information

Order Model	Quality Grade	Package Name	Packaging materials
BST8412MQI	B class	CLCC28	ceramics