BST7734

1. Product Overview

BST7734 is a high-precision, high-throughput A/D conversion chip. With a total conversion time of 500μs (2kHz channel switching), 16-bit peak-to-peak resolution can be accurately obtained. The maximum data throughput of BST7734 reaches 15.4kHz. The BST7734 analog front end has 4 single-ended input channels to choose from, with a unipolar or bipolar input range of ±10V and operates under a +5V single analog power supply. This part has the ability to detect over-range and under-range voltages. It can withstand analog range input to ±16.5V overvoltage without affecting the performance of other adjacent channels.

2. Product Features

- High precision ADC.
- 24 digits without missing codes.
- ±0.0025% nonlinearity.
- Fast channel conversion optimization.
- 18-bit peak-to-peak resolution (21 bits effective) 500Hz.
- 16-bit peak-to-peak resolution (19 bits effective) 2kHz.
- 14-bit peak-to-peak resolution (18 bits effective) 15kHz.
- System calibration of each channel on a single chip.
- 4 single-ended analog inputs.
- Input range: +5V, ±5V, +10V, ±10V.
- 3- wire serial connection port.
- Schmitt triggers as logic inputs are compatible with SPI, QSPI, MICROWIRE, and DSP.
- Single supply operation.
- 5V analog power supply.
- 3V or 5V digital power supply.
- Package: 28 -pin CSOP.
- Applied to program logic control systems, data communication systems, multiplexed application process control industrial measurement.

3. Functional Block Diagram

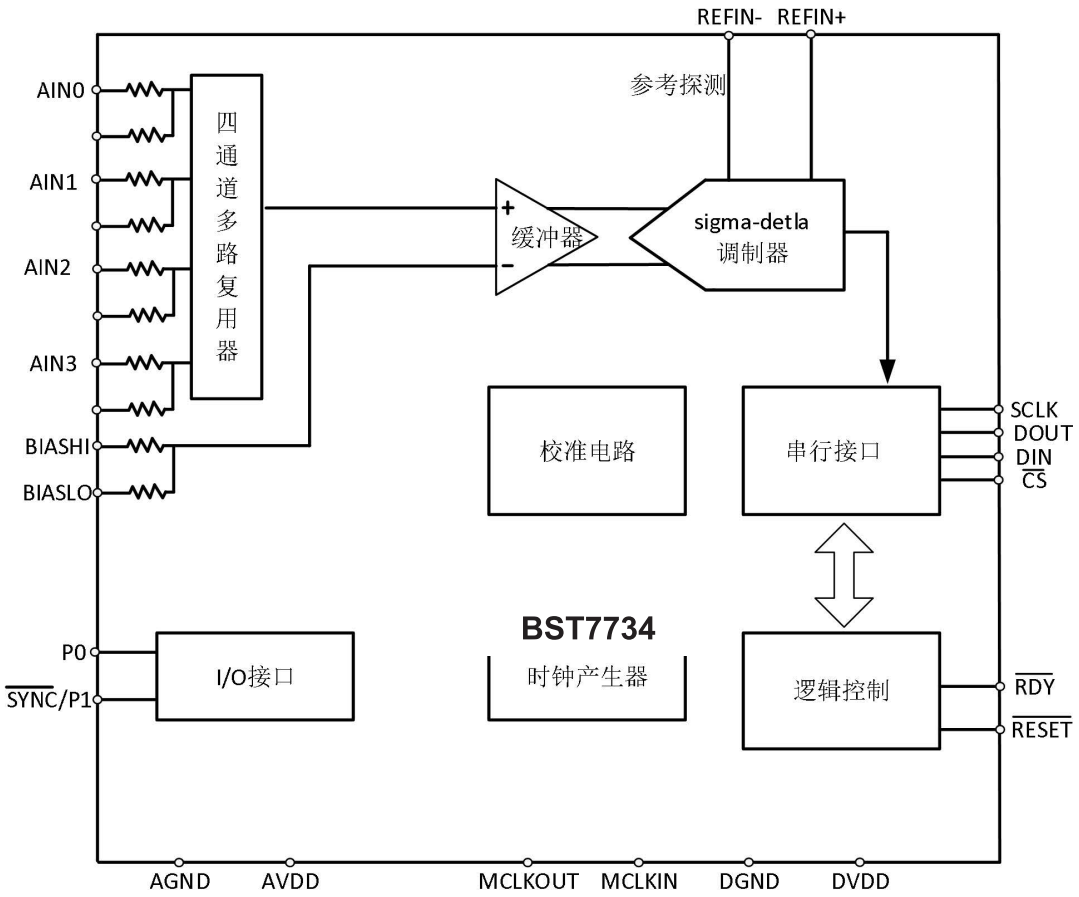

Figure 1. Functional Block Diagram

4. Electrical Parameters

Table 1. Electrical properties

Parameter	Minimum	Typical Value	Maximum	Unit	Experimental conditions / notes
ADC Execute Chopping					
Conversion time rate	372		12190	Hz	Set by time register
parameter	Minimum	Typical Value	Maximum	unit	Experimental conditions / notes
No missing code[1, 2]	24			Bits	FW≥6(conversion time≥165μs)
Integral Nonlinearity (INL)[1, 2]		±0.0010	±0.0030	%ofFSR	f_{MCLKIN} = 2.5MHz
Integral Nonlinearity (INL)[2]		±0.0025	±0.0045	%ofFSR	f_{MCLKIN} =6.144MHz
Offset Error (Unipolar / Bipolar)[3]			±10	mV	Before calibration
Effect of Temperature on Offset Drift[1]			±2.5	μV/ °C	
Gain Error[3]			±0.35	%	Before calibration
Effect of temperature on gain drift[1]			±3.2	ppmofFS/ °C	
Positive full scale error[3]			±0.5	%ofFSR	Before calibration
Temperature for positive full-scale drift Impact[1]			±3	ppmofFS/ °C	
Bipolar Reverse Full Scale Error[4]		±0.0050		%ofFSR	After calibration
Power supply sensitivity		±4	±10	LSB 16	AtDC, AIN=7V, AVDD = 5V ±5%
Channel-to-channel isolation		100		dB	AtDC, Maximum ±16.5VAINVoltage
ADC Execute non-chopping					
Conversion time rate	737		15437	Hz	Set by time register
No missing code[1]	24			Bits	FW≥8(conversion time≥117μs)
Integral Nonlinearity (INL)[2]		±0.0025		%ofFSR	
Offset Error (Unipolar / Bipolar)[3]		±15		mV	Before calibration
Effect of Temperature on Offset Drift		±25		μV/ °C	
Gain Error[3]		±0.1		%	Before calibration
Effect of temperature on gain drift[1]		±5.3		ppmofFS/ °C	
Positive full scale error[3]		±0.2		%ofFSR	Before calibration
Temperature for positive full-scale drift Impact[1]		±4		ppmofFS/ °C	
Bipolar Reverse Full Scale Error[4]		±0.0050		%ofFSR	After calibration
Power supply sensitivity		±4		LSB 16	AtDC, AIN=7V, AVDD = 5V ±5%
Channel-to-channel isolation		100		dB	DC, maximum AIN Voltage ±16.5V
Analog input voltage [1, 6, 7]					
±10V scope		±10		V	
0V to +10V scope		0to+10		V	
±5V scope		±5		V	
Parameter	**Minimum**	**Typical Value**	**Maximum**	**Unit**	**Experimental conditions / notes**
0V to +5V scope		0to+5		V	
BIASLO Voltage		0		V	
BIAS0to3 , BIASHI Voltage		2.5		V	
AIN impedance	100	124		kΩ	

AIN , BIASLO impedance	87.5	108.5		kΩ	
BIAS0to3 , BIASHI impedance	12.5	15.5		kΩ	
Input resistance matching		0.2		%	
Input register temperature coefficient		–30		ppm/ °C	
Reference Input					
REFIN(+)toREFIN(–) voltage	2.475	2.5	2.525	V	
NOREF Trigger voltage		0.5		V	NOREF Channel Status Register
REFIN(+), REFIN(–)					
Common mode voltage[1]	0		AV DD	V	
Reference DC current input[10]			400	μA	
System calibration[1, 11]					
Full scale calibration limit			+1.05×FS	V	
Zero scale calibration limit	–1.05×FS			V	
Input span	0.8×FS		2.1×FS	V	
Logic Input					
Input Current			±1	μA	
Input current CS			±10	μA	CS=DVDD
			–40	μA	CS=DGND, internal pull-up resistor
Input Capacitance		5		pF	
V_{T+}[1]	1.4		2	V	DV DD =5V
V_{T-}[1]	0.8		1.4	V	DV DD =5V
$V_{T+} – V_{T-}$[1]	0.3		0.85	V	DV DD =5V
V_{T+}[1]	0.95		2	V	DV DD =3V
V_{T-}[1]	0.4		1.1	V	DVDD = 3V
$V_{T+} – V_{T-}$[1]	0.3		0.85	V	DVDD = 3V
Master clock INONLY					
Input Current			±10	μA	
Input Capacitance		5		pF	
V_{INL} Input low voltage			0.8	V	DVDD = 5V
V_{INH} Input high voltage	3.5			V	DVDD = 5V
V_{INL} Input low voltage			0.4	V	DVDD = 3V
V_{INH} Input high voltage	2.5			V	DVDD = 3V
Logic Output[12]					
V_{OL} Output low voltage			0.4	V	I_{SINK} = 800μA, DV_{DD} = 5V
V Output high voltage	4.0			V	I_{SOURCE} =200μA, DV_{DD} =5V
V_{OL} Output low voltage			0.4	V	I_{SINK} = 100μA, DV_{DD} = 3V
V Output high voltage	DV DD –0.6			V	I_{SOURCE} =100μA, DV_{DD} =3V
Suspension leakage current			±1	μA	

Parameter	Minimum	Typical Value	Maximum	Unit	Experimental conditions / notes
Suspended leakage capacitor		3		pF	
P0 , P1 Input / Output					Level Referenced Analog Power Supply
I Input Current			±10	μA	

V_{INL} Low voltage			0.8	V	AVDD = 5V
V_{INH} Input high voltage	3.5			V	AVDD = 5V
V_{OL} Output low voltage			0.4	V	I_{SINK} =7mA, See Abs.Max.Ratings
V Output high voltage	4.0			V	I_{SOURCE} =200μA, AV_{DD} =5V
Power supply					
AVDD –AGND Voltage	4.75		5.25	V	
DVDD –DGND Voltage	4.75		5.25	V	
	2.70	3.60		V	
AV_{DD} Current (normal operating mode)		13.5	15.9	mA	AVDD = 5V
DV_{DD} Current (normal operating mode)		2.8	3.1	mA	DVDD = 5V
DV_{DD} Current (normal operating mode)		1.0	1.5	mA	DVDD = 3V
Power dissipation (normal operating mode)		85	100	mW	
AV_{DD} +DV_{DD} Current (Shutdown Mode)		100		μA	
Power dissipation (shutdown mode) 14		525		μW	

Notice: 6 Specifications are not product tested and are guaranteed by design.
7 See Typical Performance Characteristics
8 Pre-calibration specifications. Channel system calibration reduces these errors to normal noise levels.
9 Applies after zero-scale and full-scale calibration. After offset and gain errors have been removed, a negative full-scale error indicates that an error still exists.
10 5ADC zero-scale self-calibration reduces this error to ±10mV. Channel zero-scale system calibration error reduces this error to normal noise.
11 For detailed characteristics. The output data range corresponds to the specified normal input voltage range. Outside the normal input voltage range of the ADC , the performance of the ADC may degrade. Outside the normal input volt age range, the OVR bit of the channel status register and the value of the data register are configured. The value of the channel data register depends on the mode register. For more details, see the register and circuit description section
12 when the AIN voltage range reaches ± 16.5V.
13 from the PIN pin to the internal node is typically 108.5k Ω + 15.5k Ω = 124k Ω in a common circuit configuration.
14 Forspecifiedperformance.PartisfunctionalwithlowerVREF.
15 The dynamic current charges the sigma-delta modulator input switch capacitor.
16 Calibration outside the specified calibration range is possible but performance will be degraded.
17 These logic levels are applied to the MCLKOUT output when using a pure MOS load.
18 When external MCLK and MCLKOUT are disabled (CLKDIS bit is set in the mode register).
19 External MCLKIN = 0V or DVDD, Digital Input = 0V or DVDD, P0 and P1 = 0V or AVDD.Specifications are subject to change without prior notice.

5. Ordering Information

Table 2. Product ordering information

Serial number	Model	Package	Packaging materials	Device level
1	BST7734	CSOP28	ceramics	B class

Note 1: a) Class B devices meet GJB 597A-1996 or GJB 597B-2012 “General Specification for Semiconductor Integrated Circuits” Class B screening requirements.