

#### BST76801PDFN6I

### 1. Product Overview

BST76801PDFN6I LDO voltage regulator is a voltage regulator with 1 A output current and fast transient response. The device uses a  $10\mu\text{F}$  low impedance capacitor to achieve fast transient response. It adopts PMOS output power tube structure, has a low input-output voltage difference and has a good linear relationship with the output current. Because PMOS is a voltage-driven device, its quiescent current is very small and is not affected by the output (the typical value of quiescent current is only  $85\mu\text{A}$  in the output current range from 0mA to 1A). This series of LDOs also provides a sleep mode: when a TTL high level is input to the  $\overline{\text{EN}}$  terminal, the chip will be turned off, and its quiescent current is less than  $1\mu\text{A}$  at room temperature. Power good (PG) can provide a high level output, which can be used for power reset and battery power low voltage indication. This series of products can achieve adjustable output, and its voltage range is 1.2 V to 5.0V. The output accuracy reaches 3 %. This series of products adopts PDFN6 package.

## 2. Product Features

- 1A Miniaturized LDO Voltage Regulator.
- Input voltage range 2.7V~5.5V.
- The output voltage range is 1.2V ~5.0V.
- Ultra-low quiescent current, 85µA typical.
- Fast transient response.
- Open drain output Power Good.
- PDFN 6 package (3mm×3mm).

## 3. Functional Block Diagram

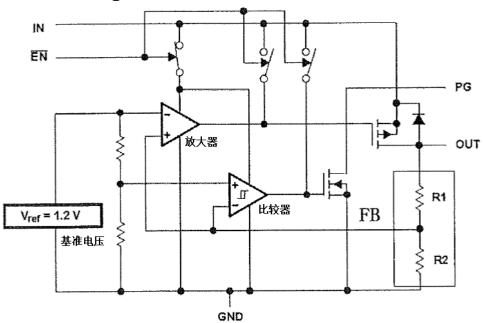
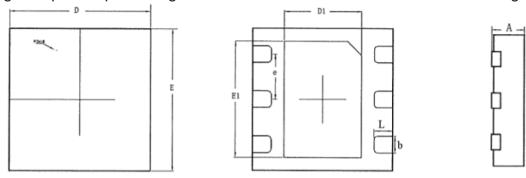


Figure 1. Functional Block Diagram



### **Packaging information**

The package shape and pin arrangement of BST76801PDFN6I are shown in the figure below.



			单位为毫米		
尺寸符号	数值				
	最小	公称	最大		
D	2.90	_	3.10		
Е	2.90	_	3.10		
D1	1.45		1.85		
E1	2.25		2.65		
е	_	0.95	_		
b	0.20	_	0.50		
L	0.25	_	0.55		
A	0.60	_	1.00		

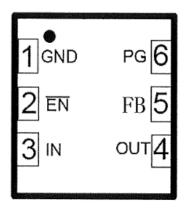


Figure 2. BST76801PDFN6I package outline and pin arrangement

The pin description of BST76801PDFN6I is shown in the following table.

Table 1Pin Description

Pin number	Pin Symbols	bols Functional Description		
	EN	Enable input, low effective		
	IN	Voltage input terminal		
	OUT	Voltage output		
	FB/NC	Adjustable feedback voltage input terminal, fixed as NC		
	PG	PG output		



# 4. Electrical parameters

Unless otherwise specified, the electrical characteristics shall be as specified in Table 2 and shall be applicable to the full operating temperature range of -55 °C≤TA≤125 °C, and shall be tested with reference to GB/T17940-2000.

**Table 2. Electrical properties** 

characteristic	symbol	condition (Unless otherwise specified, V <sub>IN</sub> =2.7V , -40 °C ≤ <i>TA</i> ≤85 °C)	Limit value		unit
			Minimum	maximum	
Input voltage range	V <sub>IN</sub>	•	2.7	5.5	V
Output voltage	Vo	$1.2V \le V \le 5.0V$ , $V_{IN} = 5.5V$	0.97 V <sub>O</sub>	1.03 Vo	V
Feedback voltage	V <sub>FB</sub>		1.164	1.236	V
Feedback input current	I FB	FB = 1.5 V	_	10 0	nA
Quiescent Current	/ q	1mA ≤ <i>I</i> <sub>0</sub> ≤ 1A	_	180	μA
Output current limit	/ limit	V = 0 V	_	2.5	Α
Standby current	/ <sub>sb</sub>	$EN = 0V_{IN}$	_	10	μΑ
High level enable input voltage	V ENH		2.5	_	V
Low level enable input voltage	VENL		_	0.9	V
Enable Input Voltage Leakage Current	/ EN	EN = 0V	-1	1	μΑ
		EN = V <sub>IN</sub>	-1	1	μΑ
Low dropout voltage	V <sub>D</sub>	I <sub>O</sub> =1A , V <sub>OUT</sub> =5V	_	500	mV
Line Regulation	V <sub>REG_line</sub>	2.7V≤ V <sub>IN</sub> ≤5.5V, V <sub>OUT</sub> = V <sub>FB</sub>	_	0.5	%/V
Load Regulation	V REG_load	1mA ≤ I o ≤ 1A VOUT = VFB	_	30	mV
PG effective minimum input voltage	V <sub>PIN</sub>	I <sub>O(PG)</sub> = 300 μA	_	1.5	V
PG output low level voltage	VIR	$I_{O(PG)} = 1m A$	_	0.4	V
PG leakage current	I PG	$V_{(PG)} = 5V$ , $V_{IN} = 5.5V$	_	1	μA
PG trigger threshold voltage	V <sub>TH_PG</sub>	V o decreases	92	98	%V o