BST7606 16 -bit A /D converter

Product manual

V1.3.2

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I. Product Overview

BST7606 is a channel synchronous sampling analog-to-digital data acquisition system (DAS). It has a built-in second-order anti-aliasing filter, a track-and-hold amplifier, a 6-bit charge redistribution successive approximation analog-to-digital converter (ADC), a flexible digital filter, a 2.5V reference voltage source, a reference voltage buffer, and high-speed serial and parallel interfaces. The chip operates in a temperature range of -55 ° C to + 25° C. BST7606 is available in 64-pin plastic and ceramic QFP packages, and its functions, dimensions, and pin definitions are compatible with AD7606.

The BST7606 is powered by a single 5V power supply and can handle ± 0V and ±5V bipolar input signals. All channels can be sampled at a throughput rate of up to 80k SPS. The analog input impedance of the BST7606 is MQ. It uses a single power supply, has on-chip filtering and high input impedance, so there is no need to drive an operational amplifier and an external bipolar power supply.

II. Product Features

- 8/ channel synchronous sampling input
- True bipolar analog input range: ± 0V, ± 5V
- 5V single analog supply, VDRIVE: 2.3V to 5V
- Fully integrated data acquisition solution
- Analog input clamp protection
- with M Q analog input impedance
- Second-order anti-aliasing analog filter
- On-chip precision reference voltage and buffer
- 6 -bit, 80KSPS ADC (all channels)
- Oversampling capability provided by digital filter
- Flexible parallel/serial interface
- Low power consumption: 75mW

III Functional Block Diagram

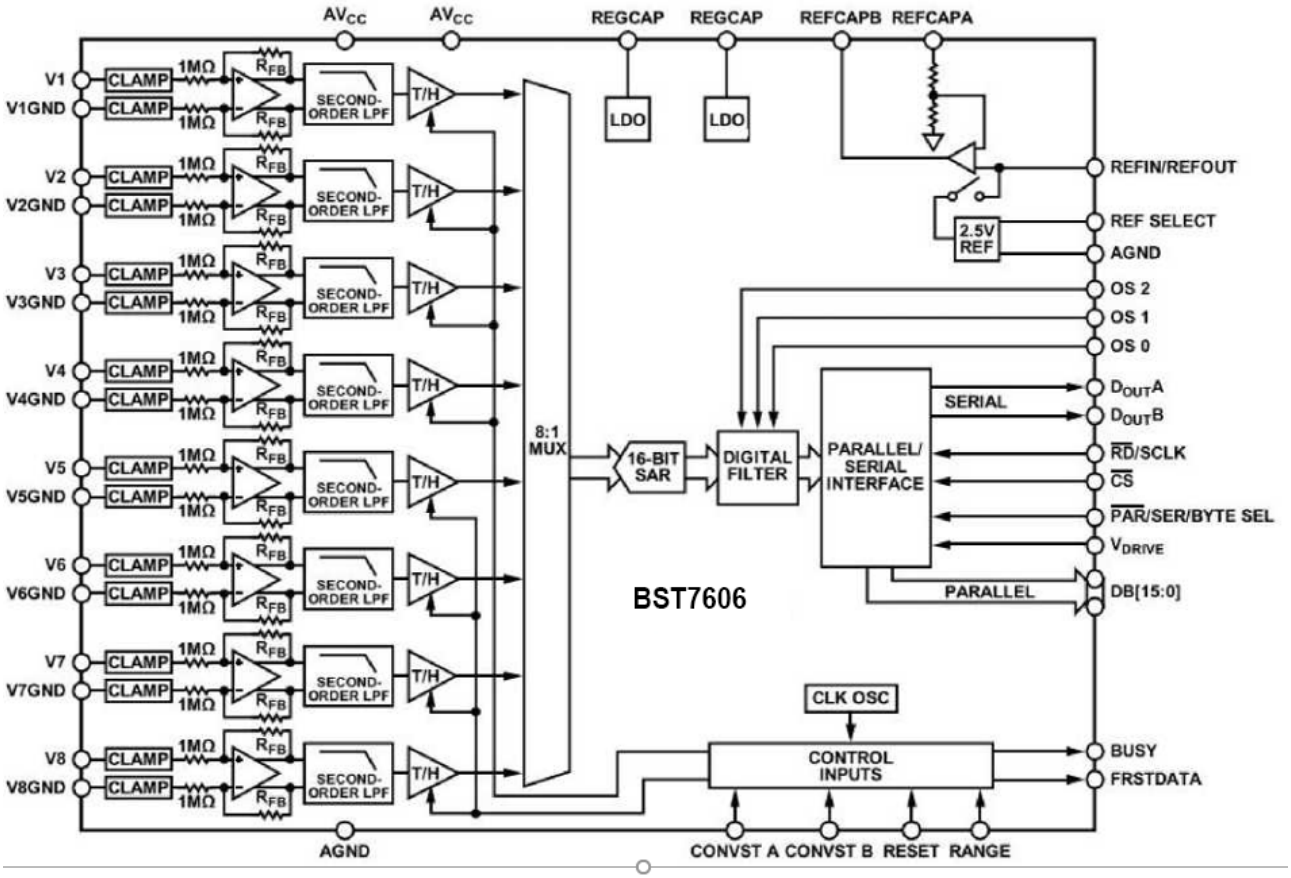


Figure 1. Functional block diagram

IV. Packaging information

4.1. Plastic LQFP64 package

The BST7606 plastic package shape and pin arrangement are shown in the figure below.

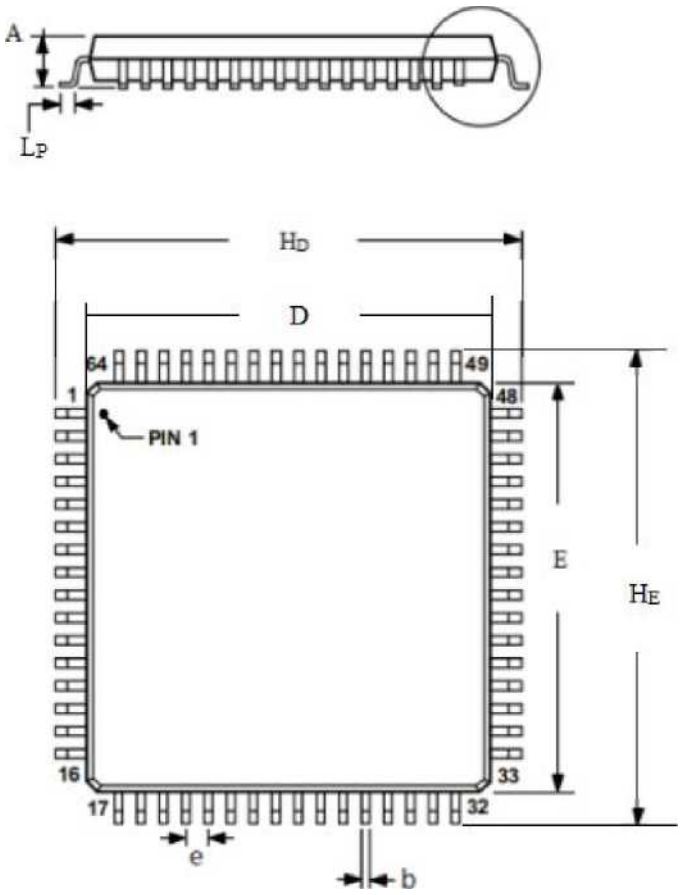


Figure 2. Plastic P64 package outline

Unit is mm

DIMENSION SYMBOLS	NUMERIC		
	MINIMUM	NOMINAL	MAXIMUM
D	,80	—	0.20
E	,80	—	0.20

HD	,80	—	2.20
H E	,80	—	2.20
A	—	—	,60
b	0. 7	—	0.27
L P	0.45	—	0.75
e	—	0.50	—

4.2 Ceramic CQFP64 package

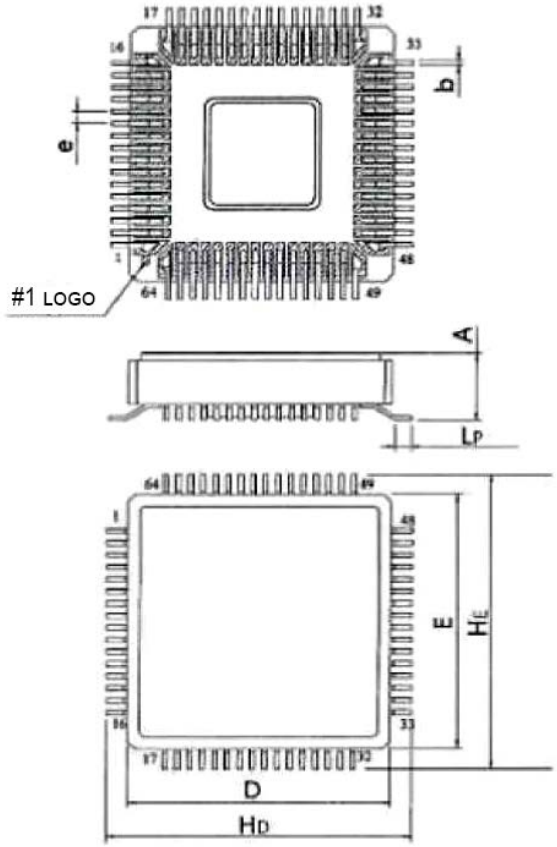


Figure 3 Ceramic CQFP64 Package Dimensions

Unit is mm

DIMENSION SYMBOLS	NUMERIC		
	MINIMUM	NOMINAL	MAXIMUM
D	,85	—	0.55
E	,85	—	0.55
HD	,60	—	2.40
HE	,60	—	2.40
e	—	0.50	—
b	0. 0	—	0.30
LP	0.40	—	-
A	—	—	3.60

4.3. Pin Description

Table 1. Pin Description

PINS	PIN NAME	FUNCTIONAL DESCRIPTION
,37,38,48	AV CC	Analog Supply Voltage, 4.75V to 5.25V, Supply voltage for the internal front-end amplifier and ADC core.
2,26,35,40,4,47	AGND	Analog ground, the ground reference point for all analog circuits.
Page65,4,3	OS[2:0]	Oversampling mode control port. OS2 is the MSB control bit and OS0 is the LSB control bit.
6	P A R /SER/BYTE SEL	Parallel, serial, byte data output mode control port.
7	STBY	Standby mode control port, low level is valid.
8	RANGE	Analog input range control port.
, 0	CONVSTA CONVSTB	Signal conversion control port. CONVSTA CONVSTB controls and starts channels VI to V4, and CONVSTB controls and starts channels V5 to V8,
	RESET	Reset control port. RESET rising edge reset, the device should receive a RESET pulse

		after power-on. The typical value of RESET high pulse width is 50ns,
2	RD /SCLK	Data read signal port. In parallel mode, if both CS and RD are at logic low level, the output bus is started. In serial mode, this pin is used as the serial clock input for data transmission. The falling edge of CS makes the data output lines D out A and D out B out of three-state and outputs the conversion results one by one.
3	CS	Chip select signal port, low level is effective. Enable data frame transmission.
4	BUSY	Conversion identification signal port. After both CONVSTA and CONVST B reach a rising edge, this pin becomes a logic high level, indicating that the conversion process has started. The BUSY output remains high until the conversion process of all channels is completed. The BUSY falling edge indicates that the conversion data is being latched into the output data register and can be read after time t4,
5	FRSTDATA	The first set of channels VI data output identifies the signal ports.
22- 6	DB [6:0]	Parallel output data bits DB6 to DB0.
23	VDRIVE	Logic power input, operating voltage of the logic interface.
24	DB7/DOUTA	Parallel output data bit DB7/ serial interface data output pin DOUTA.
25	DB8/DOUTB	The parallel output data bits are on the DB8 / serial interface data output pin DOUTB.
3 -27	DB[3:]	Parallel output data bits DB 3 to DB.
32	DB 4/HBEN	Parallel output data bit DB 4/ high byte enable (HBEN).
33	DB 5/ BYTE SEL	Parallel Output Data Bit DB 5 / Parallel Byte Mode Select (BYTESEL).
34	REF SELECT	Internal / external reference voltage selection control port. Logic high/ A logic low internal reference voltage is enabled.
		voltage is disabled, an external reference must be applied to REFIN/REFOUT pin.

36,3	REGCAP	Internal regulator output voltage decoupling capacitor pins. These output pins should be decoupled to ground through a luF capacitor. Pin output voltage range,8V ~ 2.0V, These two pins are not allowed to be shorted.
42	REFIN REFOUT	Reference voltage input (REFIN) reference voltage output (REFOUT), a 0uF capacitor should be connected between this pin and the ground near the REFGND pin,
43,46	REFGND	Reference Voltage Ground Pin.
44,45	REFCAPA REFCAPB	Reference voltage buffer output port. These pins must be connected together and decoupled to AGND through low ESR 0uF ceramic capacitors, the pin voltage is about 4.5V.
4, 5, 53, 55, 57, 5, 6,63	V ～ V8	Analog input V ~ V8 ports.
50, 52, 54, 56, 58, 60, 62, 64	V GND ～ V8GND	Analog input ground port. These pins are the AGND pins.

V. Absolute Maximum Ratings and Recommended Operating Ranges

5.1. Absolute Maximum Ratings

SERIAL NUMBER	PARAMETER NAME	PARAMETER VALUE
1	Analog supply voltage *(AV CC)*	-0.3V～+6V
2	Digital port supply voltage (*V* DRIVE)	-0.3V ～ *AVCC* + 0.3V
3	Analog input voltage	±l6.5V
4	Digital input voltage	-0.3V ~ *V* DRIVE +0.3V
5	Digital output voltage	-0.3V ~ *V* DRIVE +0.3V
6	Reference input voltage (*V* REFIN)	-0.3V ~ *AVCC* + 0.3V
7	Input current of ports other than power supply (*I* IN)	± 0mA
8	Storage ambient temperature *T*	-65° C ~ + 50° C

9	Lead wire soldering temperature resistance (*Th*)	300
10	Junction temperature (*T* J)	75C

Note:

- Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

5.2. Recommended working range

SERIAL NUMBER	PARAMETER NAME	PARAMETER VALUE
	Digital port supply voltage (V DRIVE)	2.3V ~ 5.25V
2	Analog supply voltage (AV cc)	4.75V ~ 5.25V
3	Reference voltage (V ref, internal reference or external reference)	2.5V
4	Working environment temperature (TA)	-55 ° Γ ～ 25° C

VI. Electrical characteristic parameters

The electrical characteristic indicators are the best indicators that this series of products can achieve. Different quality levels and packaging forms are slightly different. Please refer to the corresponding detailed specifications for details.

Table 2. Electrical characteristics

PARAMETER	SYMBOL	CONDITION (UNLESS OTHERWISE SPECIFIED, 4.75V ≤ AVCC ≤ 5.25V, 2.3V ≤ VDRIVE ≤ 5.25V,ANALOG INPUT RANGE: ± 5V-55 ℃ ≤TA≤ 25 ℃ ）	MINIMUM	AXIMUM	UNIT
Resolution	RE S	No missing codes, AV CC = V DRIVE = 5V	6	—	Bits

Differential nonlinearity error	DN L	AV CC =V DRIVE = 5V	-0.	2	LSB
Integral nonlinearity error	INL	AV CC =V DRIVE = 5V	- 0	0	LSB
Positive full-scale error	E FP	External reference, AV CC = V DRIVE = 5V	- 5	5	mV
		Internal reference, AV CC = V DRIVE = 5V			
Negative full scale error	E F	External reference, AV CC = V DRIVE = 5V	- 5	5	mv
		Internal reference, AV CC = V DRIVE = 5V			
Bipolar Zero Error	E Z	AV CC = V DRIVE = 5V, analog input Range: ± 0V	-20	20	LSB
		AV CC = V DRIVE = 5V, analog input Range: ±5V	-30	30	LSB
Digital input high level voltage	V IN H	—	0. × V DRIVE	—	V
Digital input low level voltage	V IN L	—	—	0. × V DRIVE	V
Digital input current	I IN	Excluding RANGE Pinout	-2	2	μA
Digital output high level voltage	V	—	V DRIVE - 0.8	—	V
Digital output low level voltage	V OL	—	—	0.8	V
Power consumption	P D	Normal working status	—	75	mW
Signal-to-Noise Ratio	SN R	AV CC =V DRIVE = 5V , V IN = -0.5dBFS, no oversampling	82	—	dBc
		AV CC =V DRIVE = 5V , V IN =-0.5dBFS, 4 Oversampling	86	—	dBc
Serial read clock frequency	K	AV CC =V DRIVE = 5V	—	20	MHz
Sampling rate	fs	AV CC =V DRIVE = 5V		80	KSPS

VII. Functional Description

7.1. Analog Input

7.1.1. Analog input range

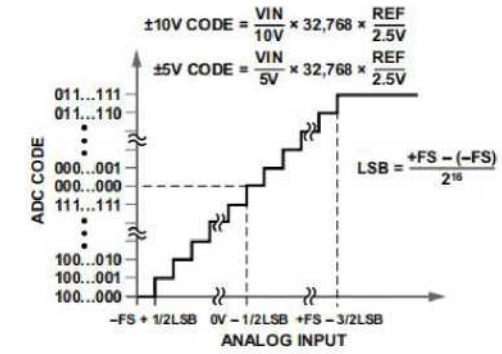
BST7606 can handle true bipolar, single-ended input voltage. The logic level of the RANGE pin determines the analog input range of all analog input channels. If this pin is connected to a logic high level, the analog input range of all channels is ± 0V, If this pin is connected to a logic low level, the analog input range of all channels is 5V, Changes in the logic state of this pin will immediately affect the analog input range, but in addition to the normal acquisition time requirements, there is a typical settling time requirement of about 0 u S. It is recommended to set the RANGE pin by hard wiring according to the input range required by the system signal.

7.1.2. Analog input impedance

The analog input impedance of BST7606 is MΩ, This is a fixed input impedance that does not change with the sampling frequency. The high input impedance can avoid the need for the driver amplifier on the end allows it to be connected directly to the signal source or sensor. Since no driver amplifier is required, the bipolar linear power supplies (usually a source of noise in the system).

7.2. ADC Transfer Function

BST7606 is two's complement. The code transition is designed to be in the middle of consecutive LSB integer values (i.e. /2LSB and 3/2LSB), The LSB size of BST7606 is FSR/65,536, Its ideal transfer characteristic is shown in the figure below.



	+FS	MIDSCALE	–FS	LSB
±10V RANGE	+10V	0V	–10V	305μV
±5V RANGE	+5V	0V	–5V	152μV

Figure 4 Ideal transfer characteristics of BST7606

7.3. Internal / External Reference Voltage

The BST7606 has a built- in 2.5V bandgap reference voltage source. The REFIN/REFOUT pin can use this 2.5V **reference** voltage for 4.5V on-chip reference voltage is generated internally, and a 2.5V external reference voltage is also allowed to be applied. The applied 2.5V external reference voltage is also amplified to 4.5V by the internal buffer, this 4.5V buffered reference voltage is the reference voltage used by the SARADC, REF SELECT pin is a logic input that allows the user to select either an internal reference or an external reference. If this pin is set to a logic high, the internal reference mode is selected and enabled. If this pin is set to a logic low, the internal reference is disabled and an external reference must be applied to the REFIN/REFOUT pin. The internal reference buffer is always enabled. After reset, the device operates in the reference mode selected by the REF SELECT pin. Whether using an internal or external reference, decoupling the REFIN/REFOUT pin is required. A 0 PF ceramic decoupling capacitor is required for the REFIN/REFOUT pin.

7.3.1. External Reference Voltage Mode

BST7606 can use an external reference voltage source ADR42 to drive the REFIN/REFOUT pins of all BST7606 devices, 00nF decoupling capacitor should be used on the REFIN/REFOUT pin of each device in this configuration.

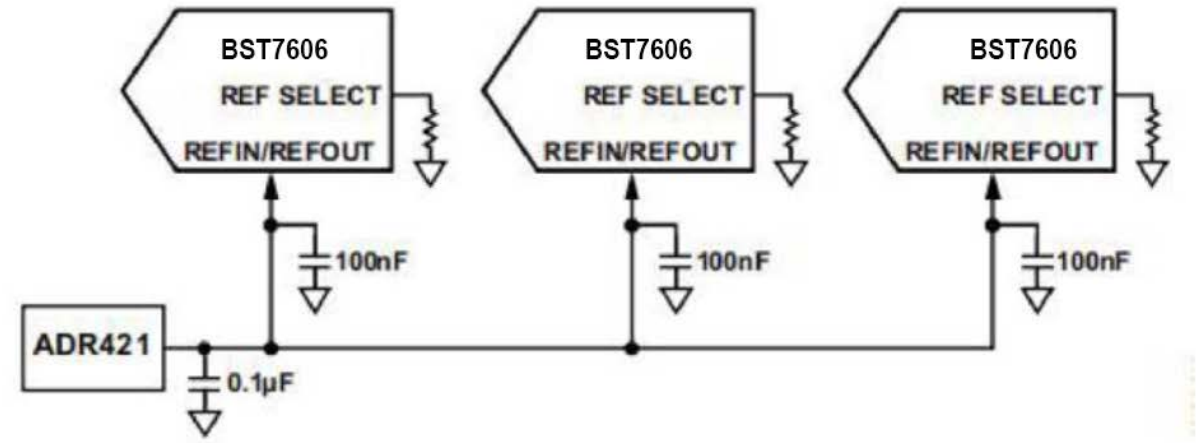


Figure 5: External reference voltage source driving multiple REFIN pins.

7.3.2. Internal Reference Voltage Mode

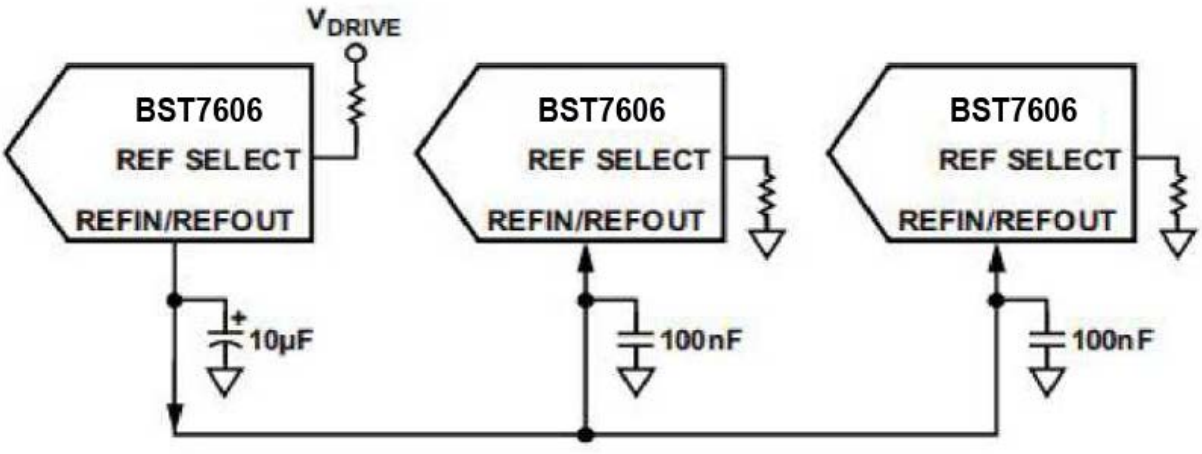


Figure 6. Internal reference driving multiple REFIN pins

BST7606 device configured in internal reference voltage operation mode can be used to drive the remaining BST7606 devices configured in external reference voltage operation mode, as shown in the figure below. It should use a 0 -tetra ceramic decoupling capacitor

to decouple its REFIN/REFOUT pins. The other 7606 devices configured in external reference voltage mode should each use at least one 00nF decoupling capacitor to decouple their REFIN/REFOUT pins.

VIII. Conversion Control

8.1. All analog input channels are sampled simultaneously

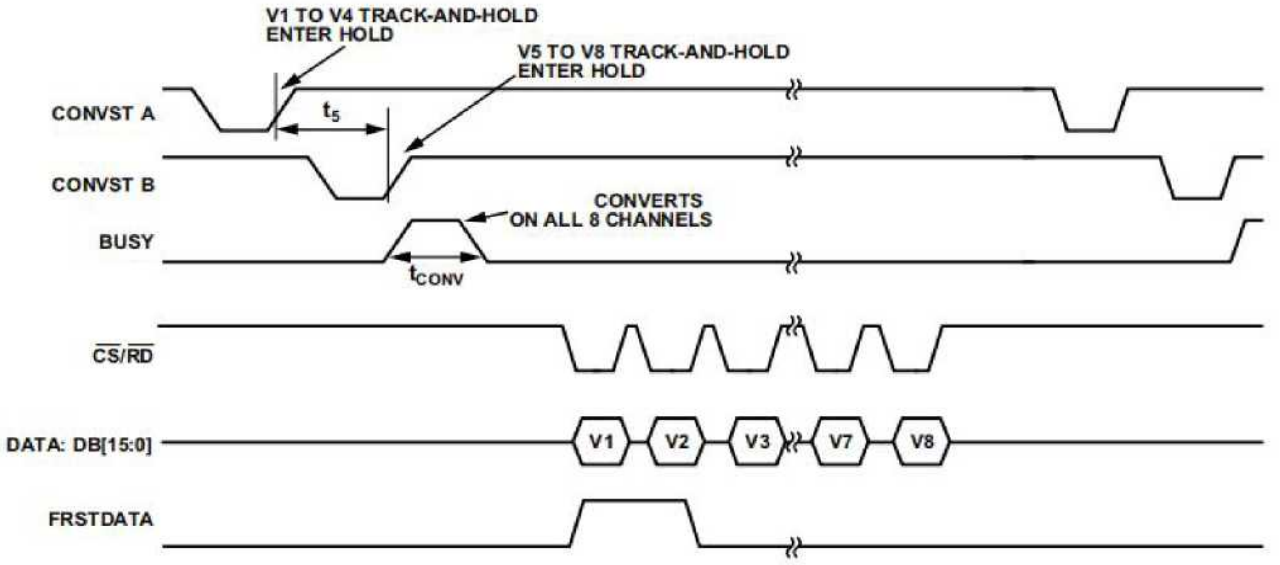
The BST7606 can perform synchronous sampling of all analog input channels. When the two CONVST pins (CONVSTA and CONVST B) are connected together, all channels are sampled synchronously. One CONVST signal can control the X inputs of both CONVSTs, The rising edge of this common CONVST signal starts synchronous sampling of all analog input channels (V -V8),

The BST7606 has an on-chip oscillator for conversion. The conversion time for all ADC channels is 00ms. The BUSY signal informs the user that a conversion is in progress, so when the rising edge of CONVST is applied, BUSY becomes a logic high and becomes a low at the end of the entire conversion process. The falling edge of the BUSY signal is used to return all eight sample-and-hold amplifiers to tracking mode. The BUSY falling edge also indicates that new data can be read from the parallel bus DB[5:0], the DOUTA/DOUTB serial data lines, or the parallel byte bus DB[7:0].

8.2. Two groups of channels are sampled synchronously

BST7606 also allows the analog input channels to be sampled synchronously in two groups. This can be used in power line protection and measurement systems to compensate for the phase difference introduced by PT and CT transformers. This sampling method can be achieved by activating the two CONVST pins independently through pulses, and only when oversampling is not used. CONVSTA is used to start synchronous sampling for the first group of channels (V -V4); CONVST B is used to start synchronous sampling for the second group of analog input channels (V5-V8), As shown in the figure below.

at the rising edge of CONVSTA, The track-and-hold amplifiers for the second set of channels enter hold mode at the rising edge of CONVST B. The conversion process begins when both CONVST X signals have reached rising edges, so BUSY goes high at the rising edge of the next CONVST X signal, using two independent CONVST X signals.



Connect all unused analog input channels to AGND, the results for unused channels are still included in the data read because all channels are always converted.

8.3. Digital Interface

The BST7606 provides three interface options: parallel interface, high-speed serial interface and parallel byte interface. The required interface mode can be selected by PAR/SER/BYTE SEL and DB 5/BYTE SEL pins to select.

Table 3 Interface mode selection

PAR/SER/BYTE SEL	DB 5	INTERFACE MODE
0	0	Parallel interface mode
	0	Serial interface mode
		Parallel Byte Interface Mode

8.4. Parallel interface

from the BST7606 through the parallel data bus using standard CS and RD signals, When reading data through the parallel bus, the PAR/SER/BYTESEL pin needs to be connected to a low level. By internally selecting the CS and RD input signals, the conversion result can be output to the data bus. When CS and RD are both at a logic low level, the data line DB 5 to DBO is no longer in a high impedance state. The interface is shown in the figure below.

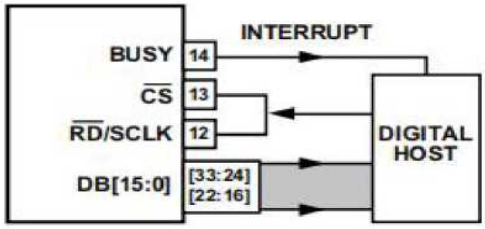


Figure 8. BST7606 interface diagram

8.5. Parallel Bytes

The parallel byte interface mode works very similarly to the parallel interface mode, but each channel conversion result is read out in two 8- bit transfers. Therefore, 6 RD pulses are required to read all eight conversion results of the BST7606, When it is configured in parallel byte mode, the PAR/SER/BYTE SEL and BYTE SEL/DB 5 pins should be connected to a logic high level, as shown in Table 3. In parallel byte mode, DB[7:0] is used to transfer data to the digital host. DB0 is the LSB of the data transfer, and DB7 is the MSB of the data transfer, DB 4 acts as the HBEN pin. When DB 4/HBEN is connected to a logic high level, the high byte (MSB) of the conversion result is output first, followed by the low byte (LSB). When DB 4 is connected to a logic low level, the LSB of the conversion result is output first, followed by the MSB, The FRSTDATA pin will remain high until all 6- bit conversion results of the VI are read from the 7606.

8.6. Serial Interface

to read back data from the BST7606 through the serial interface, the PAR/SER/BYTE SEL pin must be connected high. The CS and SCLK signals are used to transmit data from the BST7606, The BST7606 has two serial data output pins: DOUTA and DOUTB, Data can be read back from the BST7606 through a single or dual DOUT line, For the BST7606, the

conversion results of channels V -V4 first appear on D_{OUT} A On the, the conversion results of channels V5-V8 appear first on D_{OUT} B.

8.7. Read during conversion

Can also be read from the BST7606 while BUSY is high and a conversion is in progress, which has little impact on the performance of the converter and allows for faster throughput rates. Parallel, parallel byte or serial reads can be performed during conversion, with or without oversampling.

BUSY high in parallel or serial mode is shown below. Performing the read during conversion allows the highest throughput rate to be achieved when using the serial interface and VDRIVE is above 4.75V.

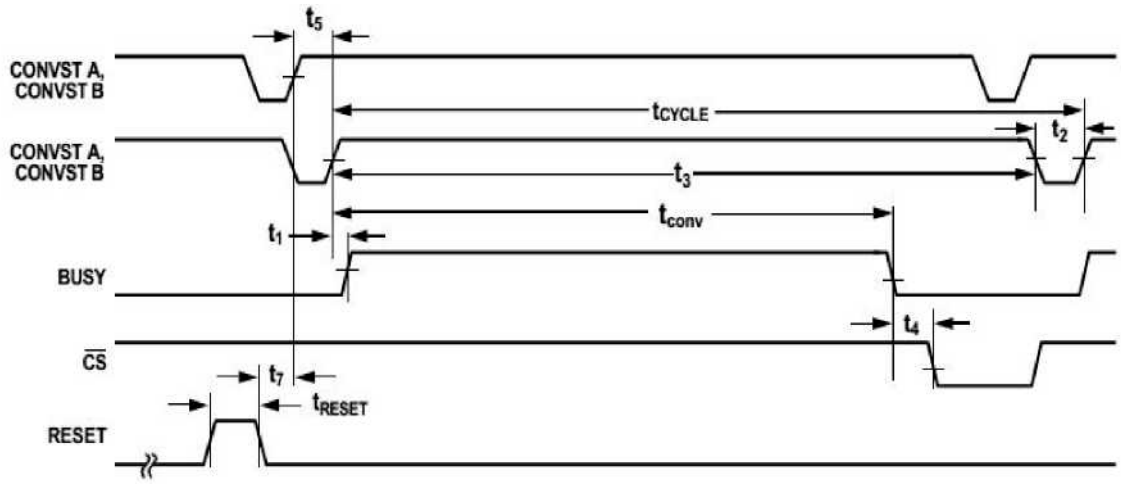


Figure 9. CONVST timing - read after conversion

8.8. Digital Filter

The BST7606 has an optional digital first-order sinc filter built in. It can be used when using lower throughput rates or when a higher signal-to-noise ratio or wider dynamic range is required.

This filter should be used in applications with high oversampling range. The oversampling ratio of the digital filter is controlled by the oversampling pin O S[2:0], as shown in the following table.

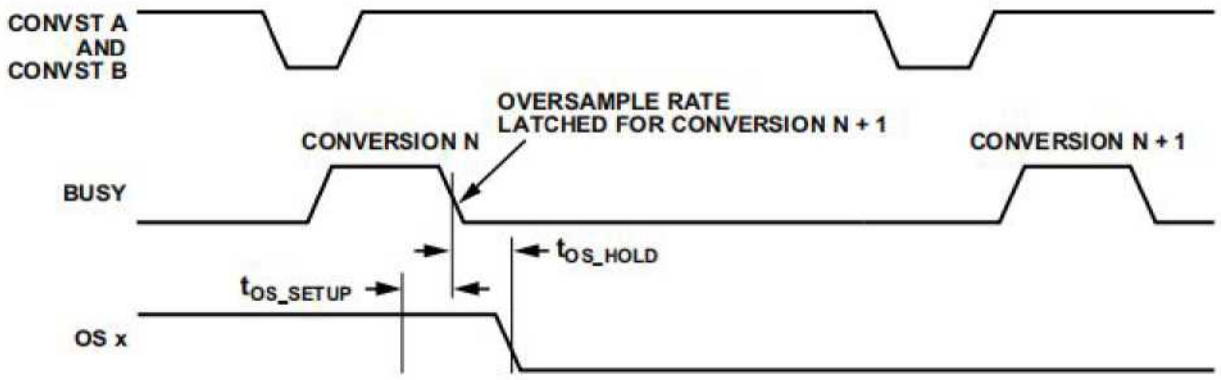
Table 4. Oversampling bit decoding

OS[2:0]	OVERSAMPLING RATIO	OS[2:0]	OVERSAMPLING RATIO
000	NO OS	00	6
00	2	0	32
0 0	4	0	64
0	8		invalid

OS2 is the MSB control bit, and OS0 is the LSB control bit. The table above provides the oversampling bit decoding used to select different oversampling ratios.

The OS pin is latched on the falling edge of BUSY, thereby setting the oversampling ratio for the next conversion, as shown in the following figure. In addition to the oversampling function, the output

The result is decimated to 6-bit resolution.



IX. Power saving mode

BST7606 provides one power saving mode: standby mode. When the SENSE pin is low, the device is in standby mode, some modules are still powered on, and the overall power consumption is 50mW.

X. Timing diagram

Table 5 Timing parameters

PARAMETER	TYPICAL VALUE	DESCRIB
Parallel / Serial / Byte Mode		
t CYCLE	5.56μs	/ throughput rate. Parallel mode, read during or after conversion, or serial mode: V DRIVE =4.75V~5.25V, Using D OUT A and D OUT B Line read during conversion
	5.56μs	/ throughput rate. Serial mode, read during conversion, V DRIVE = 3.3V
	,7μs	/ throughput rate. Serial mode, read after conversion, V DRIVE =2.3V, D OUT A and D OUT B Line switching time
t CONV	4.40μs	Conversion time, oversampling off
	,6μs	2 Oversampling
	,6μs	4 Oversampling
	40μs	8 Oversampling
	80μs	6 Oversampling
	62μs	32 Oversampling
	324μs	64 Oversampling
t WAKE-UP STANDBY	00μs	STBY rising edge to CONVST x rising edge, power-on time from standby mode
t WAKE-UP SHUTDOWN	30ms	Internal reference voltage, STBY rising edge to CONVST x rising edge, power-on time from shutdown mode
	3ms	External reference voltage, STBY rising edge to CONVST x rising edge, power-on time from shutdown mode
t RESET	50ns	RESET High level pulse width
t OS_SETUP	20ns	BUSY ToOS x Pin setup time
t OS_HOLD	20ns	BUSY ToOS x Pin hold time
t1	40ns	CONVST x High level to BUSY High level
t2	25ns	Shortest CONVST x Low level pulse

t3	25ns	Shortest CONVST x High level pulse
t4	0ns	BUSY Falling edge to CS falling edge setup time
t5	0.5ms	CONVST A/CONVST B Maximum allowable delay time between rising edges
t6	25ns	The last CS rising edge and BUSY Maximum time between falling edges
t7	25ns	RESET Low level to CONVST The shortest delay time between x high level; t7 Only applicable to reading data after conversion ш‌n normal use, it is recommended to reset Signal earlier than CONVST Signal 5us Above, and only reset once.
Parallel / Byte Read Operation		
t8	0ns	CS to RD setup time
t9	0ns	CS to RD hold time
t10	22ns	RD low level pulse width; V DRIVE Above 4.75V
	24ns	RD low level pulse width; V DRIVE Above 3.3V
	25ns	RD low level pulse width; V DRIVE Above 2.7V
	32ns	RD low level pulse width; V DRIVE Above 2.3V
t11	5ns	RD high level pulse width
t12	22ns	cs high level pulse width, cs is connected to RD
t13	7.6ns	from CS until DB [5:0] tri-state disable; VDRIVE is above 4.75V
	20n	from CS until DB [5:0] tri-state disable; V drive is higher than 3.3V
	25n	from CS until DB [5:0] tri-state disable; V drive is higher than 2.7V
	30n	from CS until DB [5:0] tri-state disable; V drive is higher than 2.3V
t14	7.6ns	Data access time after RD falling edge; V drive is higher than 4.75V
	2ns	Data access time after RD falling edge; V drive is higher than 3.3V
	25ns	Data access time after RD falling edge; V drive is higher than 2.7V
	32ns	Data access time after RD falling edge; V drive is higher than 2.3V
t15	0.4ns	Data hold time after RD falling edge
t16	2.0ns	From CS to DB [5:0] hold time
t17	22ns	from CS rising edge to DB [5:0] tri-state enable

Serial Read Operation		
f SCLK	22.0MHz	Serial read clock frequency; V drive is higher than 4.75V;
	7MHz	Serial read clock frequency; V DRIVE is higher than 3.3V
	4.5MHz	Serial read clock frequency; V DRIVE is higher than 2.7V
	5 MHz	Serial read clock frequency; V drive higher than 2.3V
t18	5ns	from CS until D out A/D out B tri-state disabled / Delay time from CS until MSB valid, V drive Above 4.75V
	20ns	from CS until D out A/D out B tri-state disabled / Delay time from CS until MSB valid, V DRiVE above 3.3V
	30ns	from CS until D out A/D out B tri-state disabled / Delay time from CS until MSB valid, V DRiVE =2.3V~2.7V
t19	7ns	Data access time after SCLK rising edge; V drive is above 4.75V
	23ns	Data access time after SCLK rising edge; V drive is higher than 3.3V
	27ns	Data access time after SCLK rising edge; V drive is higher than 2.7V
	34ns	Data access time after SCLK rising edge; V drive is higher than 2.3V
t20	0.4 t SCLK ns	SCLK low level pulse width
t21	0.4 t SCLK ns	SCLK high level pulse width
t22	7ns	SCLK rising edge to D ouT A/D ouT B valid hold time
t23	22ns	CS rising edge to D out A/D out B tri-state enable
FRSTDATA Operation		
t24	5ns	from CS falling edge until FRSTDATA tri-state is disabled; V drive is above 4.75V
	20ns	from CS falling edge until FRSTDATA tri-state is disabled; V drive is above 3.3V
	25ns	from CS falling edge until FRSTDATA tri-state is disabled; V drive is above 2.7V
	30ns	from CS falling edge until FRSTDATA tri-state is disabled; V drive is above 2.3V
t25	5ns	from CS falling edge until FRSTDATA high, serial mode, V drive above 4.75V
	20ns	from CS falling edge until FRSTDATA high, serial mode, V drive above 3.3V
	25ns	from CS falling edge until FRSTDATA high, serial mode, V drive above 2.7V

	30ns	from CS falling edge until FRSTDATA high, serial mode, V drive above 2.3V
t26	6ns	from RD falling edge until FRSTDATA high, V drive above 4.75V
	20ns	from RD falling edge until FRSTDATA high, V drive above 4.75V
	25 ns	from RD falling edge until FRSTDATA high, V drive above 4.75V
	30 ns	from RD falling edge until FRSTDATA high, V drive above 4.75V
t27	ns	from RD falling edge to FRSTDATA low level, V drive = 3.3V ~ 5.25V
	20.8 ns	from RD falling edge to FRSTDATA low level, V drive =2.3V~2.7V
t28	7 ns	from the 6th SCLK falling edge to FRSTDATA low level, V drive = 3.3V ~ 5.25V
	22 ns	from the 6th SCLK falling edge to FRSTDATA low level, V drive = 2.3V ~ 2.7V
t2	24 ns	from CS rising edge until FRSTDATA tri-state is enabled

Note:

- t7 is only applicable to reading data after conversion. In normal use, it is recommended that the reset signal is more than 50us earlier than the CONVST signal and reset only once;

Note 3:

- Actual parallel / byte read operation, it is recommended that the sum of rd low level pulse width and rd high level pulse width be greater than 00ns, and the minimum values of ti0 and ti cannot be used at the same time;

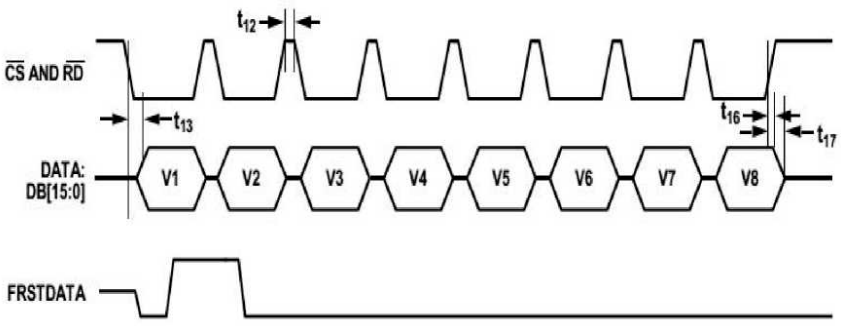


Figure 10. CONVST timing - reading during conversion

In actual use, it is recommended to use less than 11.5MHz, which is compatible with different digital circuits.

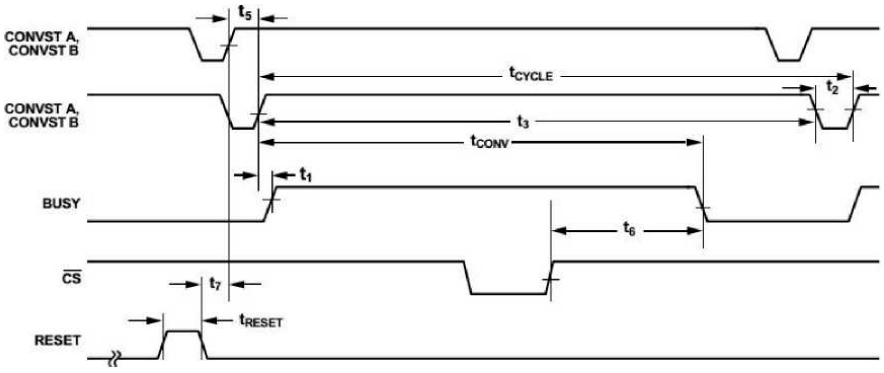


Figure 11. Parallel mode, independent CS and RD pulses

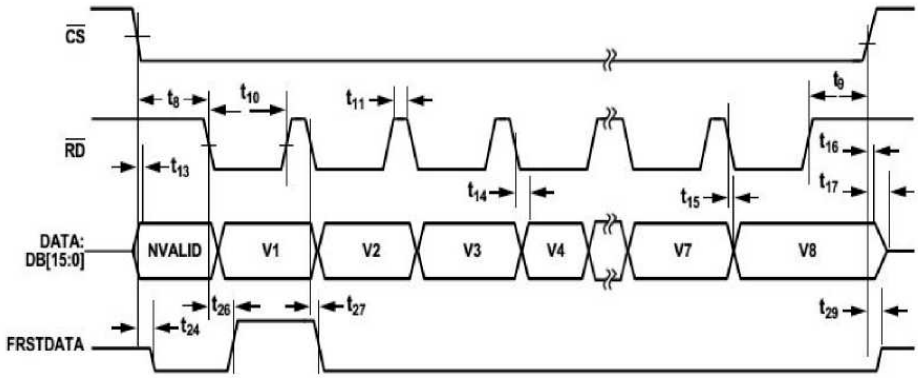


Figure 12. Byte Mode Read Operation

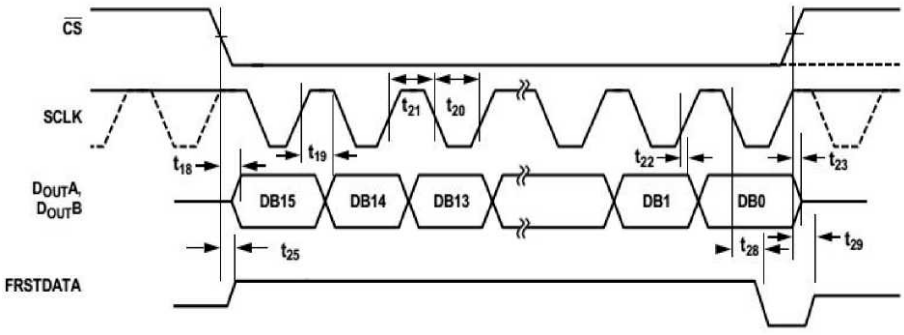
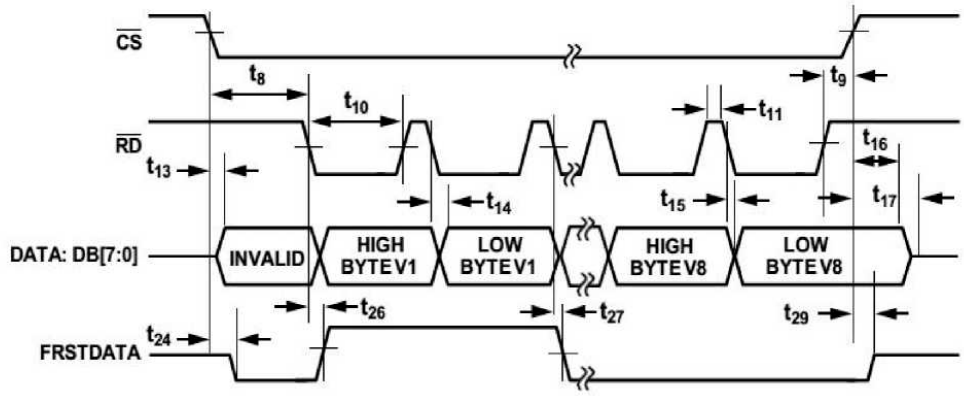


Figure 13. Serial read operation (channel)



XI. Typical Connections

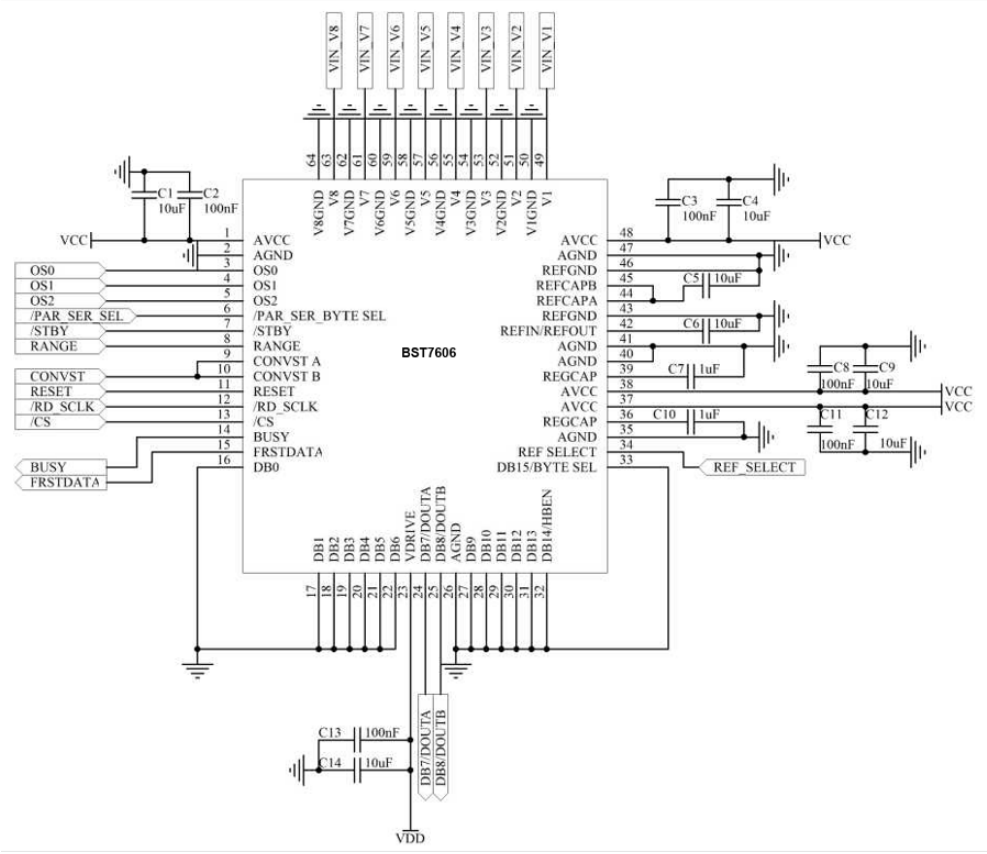


Figure 14. Typical application circuit of serial mode

Note:

- Two gears;
- VxGND is grounded. The 8 analog input signal terminals VIN_V to VIN_V8 are bipolar inputs with a maximum swing of ±5V.
- All unused analog input channels are grounded;
- Analog power supply VCC = 4.75V ~ 5.25V, digital power supply VDD = 2.3V ~ 5.25V and ± 0V

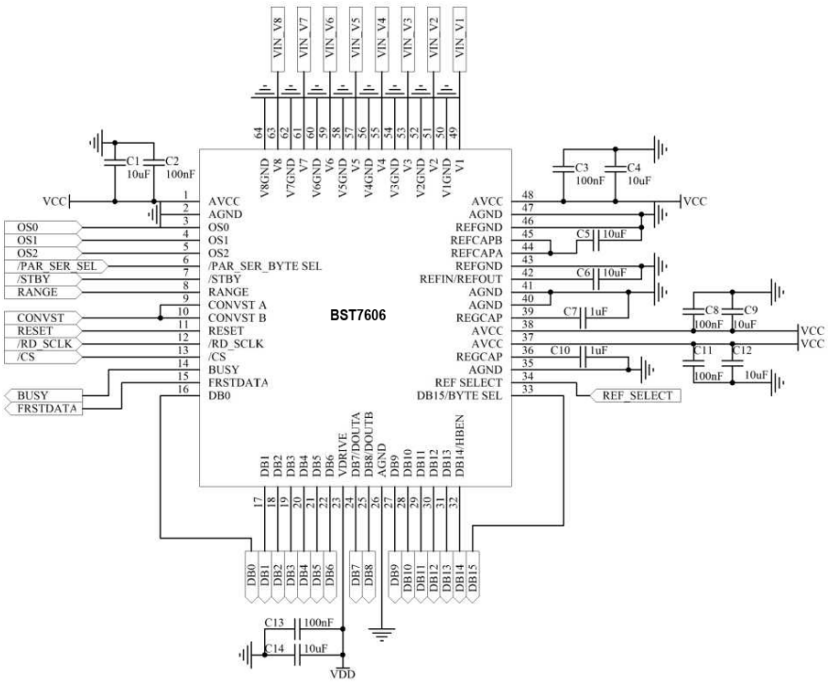


Figure 15. Parallel mode typical application circuit

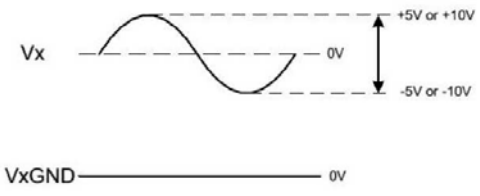


Figure 8. Single-ended mode signal input format

- Configuration ports Pin3~5 (OS0~OS2), Pin6 (/PAR_SER_BYTE SEL), Pin7 (/STBY), Pin8 (RANGE),Pin34 (REF_SELEC) up to VDD and down to GND directly through hardware circuits, If the configuration port is configured through a digital microcontroller, it is necessary to note that the configuration port signal should be reset after 500ms, to give the reset signal RESET 50us before giving the conversion signal CONVST;

- Pin24 (DB7/DOUTA) and Pin25 (DB8/DOUTB) are serial mode data output ports;
- Pin 6~Pin22, Pin24, Pin25, Pin27~Pin33 are parallel mode data output ports DB0~DB 5;
- Pinl2 (/RD_SCLK) and Pin 3 (/CS) are digital output port reading control signals;
- Pinl4 (BUSY) and Pin 5 (FRSTDATA) are conversion output identification signals;
- Results that do not use channels are still included in the data read.

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XII. Precautions for use

The device must be handled with anti-static measures.

The device operation precautions are as follows:

- The device should be operated on an anti-static workbench;
- Test equipment and apparatus should be grounded;
- Do not touch the device leads;
- Devices should be stored in containers made of conductive materials;
- Avoid using plastic, rubber or silk fabrics that can cause static electricity in the MOS area;
- If feasible, maintain relative humidity above 50%,

XIII. Ordering Information

Table 6. Product ordering information

SERIAL NUMBER	PRODUCT MODEL	PACKAGE	PACKAGING MATERIALS	QUALITY GRADE	LEAD MATERIAL	WEIGHT (G)	TYPICAL DIMENSIONS (MM) (L X W X H)	DETAILED SPECIFICATIONS
	BST7606LQFP64M3	LQFP64	plastic	N	Tinning	0.34	2.20 x 2.20 x,60	Q/BST 5024 -2022
2	BST7606CQFP64M	CQFP64	ceramics	B	Nickel plating Gold plating	,	2.40 x 2.40 x 3.60	Q/BST 5030 -2023

Note :

- Class B devices meet the Class B screening requirements of GJB 5 7B-20 2 “General Specification for Semiconductor Integrated Circuits”;
- N -level devices meet the N - level screening requirements of GJB 7400 "General Specification for Semiconductor Integrated Circuits for Qualified Manufacturer Certification".