BST7512AE CPLD
Product Brochure

Product Overview

BST7512AE is a high-density, high-performance complex programmable logic device (CPLD) based on the "product term" principle, with an integration of up to 2 million gates and 10,000 available gates; the core power supply voltage is 3V~3.6V, and the I/O voltage is 3.3V/2.5V; the number of logic arrays (LAB) is 32, with 512 trigger resources; the operating temperature range is -55℃~+125℃, and the maximum Pin-to-Pin delay time is: 10 ns (-40℃~+105℃), 15 ns (-55℃~+125℃); the packaging form is ceramic BGA256 and ceramic QFP144, and the available I/Os are 212 (CBGA256) and 120 (CQFP144); the quality assurance level is B level; ESD protection is not less than 2000V. This type of chip is widely used in computer bus systems, industrial control, communications, office automation and other fields.

Model Option Information:

Product Model	**BST7512AE**	**BST 7512AEMCQFP144**
Corresponding	EPM7512AE F256I10	EPM7512AE T144I10
Package	CBGA256	C QFP144
Quality	GJB597 B - 2012 Class B	GJB597 B - 2012 Class B
Standard No.	Q/BST 20162-2014	Q/BST 20228-2016
Available IO	212	120
Macrocell	512	512
Available doors	10000	10000
register	512	512
T_{PD} (ns)	10	10
F_{SYSTEM} (MHz)	150	150

Product features

The BST7512AE device is mainly composed of logic array modules (LAB , including logic and array, macro cells and extended product terms), programmable interconnect matrix (PIA) and I / O control and other functional modules (as shown in Figure 2) . BST7512AE can provide up to 512 macro cells, each of which includes a programmable "AND"/fixed "OR" array and a programmable trigger. Every 16 macro

cells form a logic array module. To build complex logic functions, each macro cell can provide up to 32 extended product terms.

LAB module

The BST7512AE device structure is mainly composed of 32 high-performance LAB arrays, each LAB includes 16 macro cell arrays , and the I/O and LAB and LAB communicate through PIA . Each LAB is driven by the following signals:

- 36 general-purpose logic inputs from the PIA;
- Global control over additional functions for triggers;
- Fast input channels between I/O and triggers to reduce setup time ;
- Macrocell:

The BST7512AE device includes 512 macrocells, each of which can be configured to implement combinational logic functions or sequential logic functions. The macrocell mainly includes three functional modules: product terms, product term selection matrix , and programmable triggers. The macrocell structure diagram is as follows:

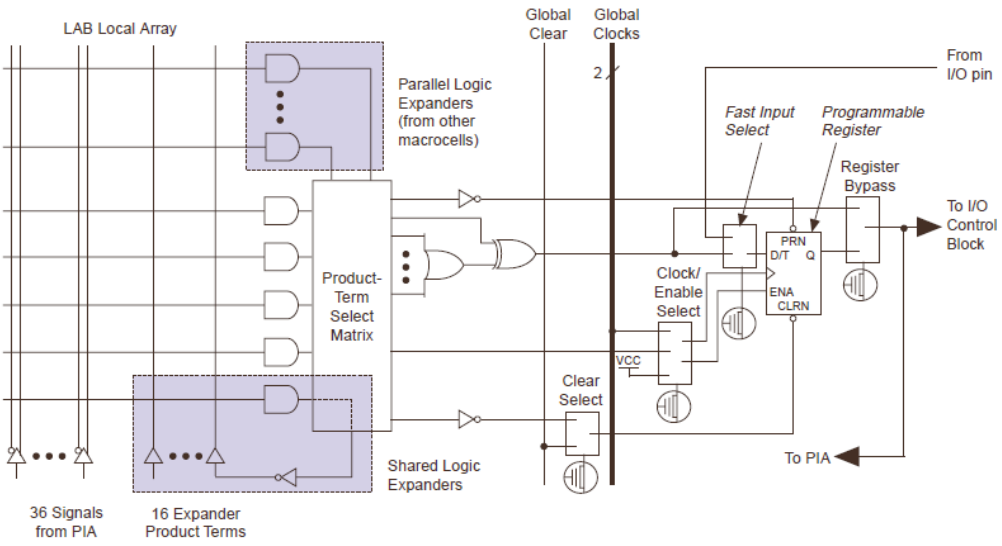


Figure 1 Macro unit structure diagram

Each macrocell can provide 5 product terms to implement combinational logic. The product term selection matrix assigns these product terms to be used as primary logic inputs or as inputs for control signals such as set, reset , clock, and clock enable of flip-flops in the macrocell .

Programmable Interconnect Array (PIA)

Between I/O and LAB and between LAB is realized through PIA . This global bus can be programmed to make any I/O input or macro unit output of the chip reach any LAB, that is, all dedicated inputs, I/O pins and macro unit outputs of BST7512AE device can drive PIA. The signal of each LAB comes from PIA, as shown in the following figure :

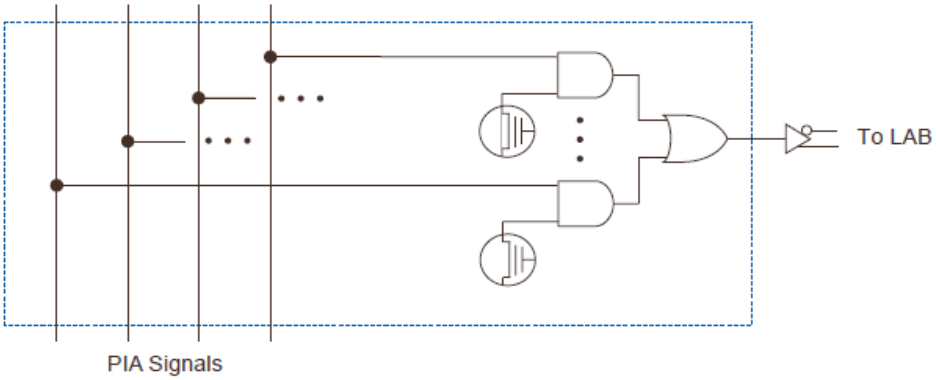


Figure 2 PIA wiring diagram

Compared with FPGA routing delay, which is cumulative and variable and depends on the path selection, the PIA delay of BST7512AE is predictable , so that the device timing is easier to estimate in application development .

I/O control module

The I/O control module can configure each I/O pin independently as input, output or bidirectional. All I/O pins include a tri-state buffer, which can be independently controlled by the global output enable, ground or power supply. The following figure is the functional block diagram of the I/O control module:

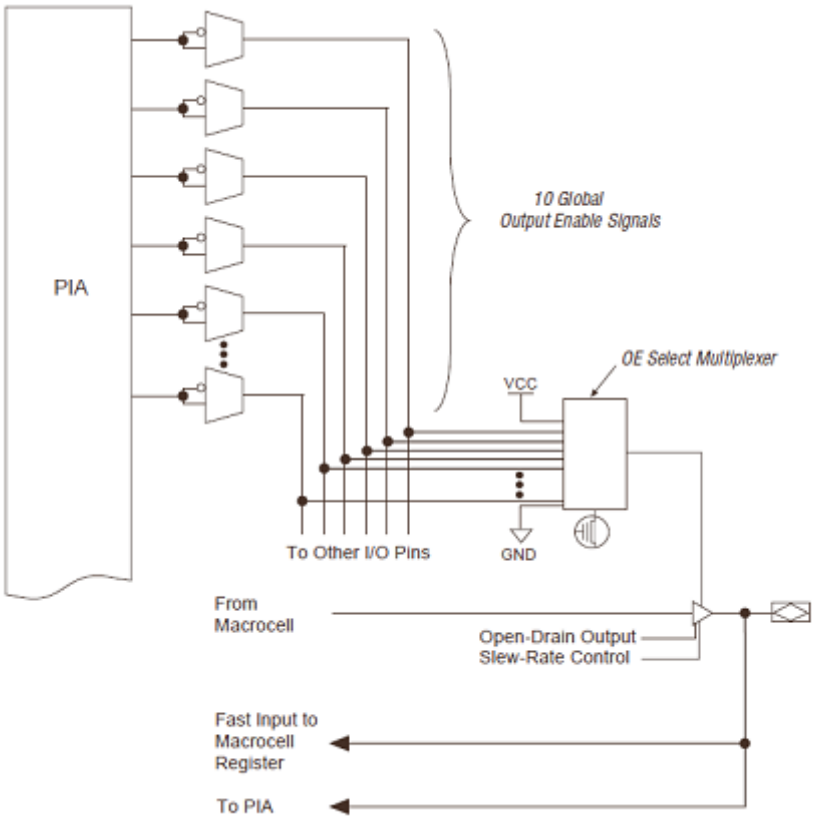


Figure 3 I/O control module functional block diagram

As shown in the figure above, the I/O control module includes 10 global output enable signals, which come from : two global output enable signals, some I/O pins and some macro cells.

When the control terminal of the tri-state buffer is connected to a low level, the buffer outputs a high impedance state, and the I/O can be used as a dedicated input. When the control terminal of the tri-state buffer is connected to a high level, the output enable is valid.

The BST7512AE device provides dual I/O feedback, that is, the macrocell and pin feedback are independent of each other. When the I/O pin is configured as an input, the macrocell associated with it can implement logic for use.

Expanding product terms

Although most logic functions can be implemented by 5-input product terms in each macrocell, additional product terms are required for complex logic functions. Therefore, another macrocell can be used to implement the necessary logic

expansion resources. The BST7512AE device provides shared and parallel expanded product terms, so that any macrocell in the same LAB can obtain such expanded product terms. These expanded product terms ensure that the fastest speed is achieved with the least logic resources after logic synthesis.

Shared Expansion Product Term

Each LAB has 16 shared extended product terms, which can be regarded as many unused product terms that are inverted and fed back to the logic array. Each shared extended product term can be used by other macrocells or all macrocells in the same LAB to form a complex logic function. When using shared extended product terms, a certain transmission delay will be generated. As shown in the following figure :

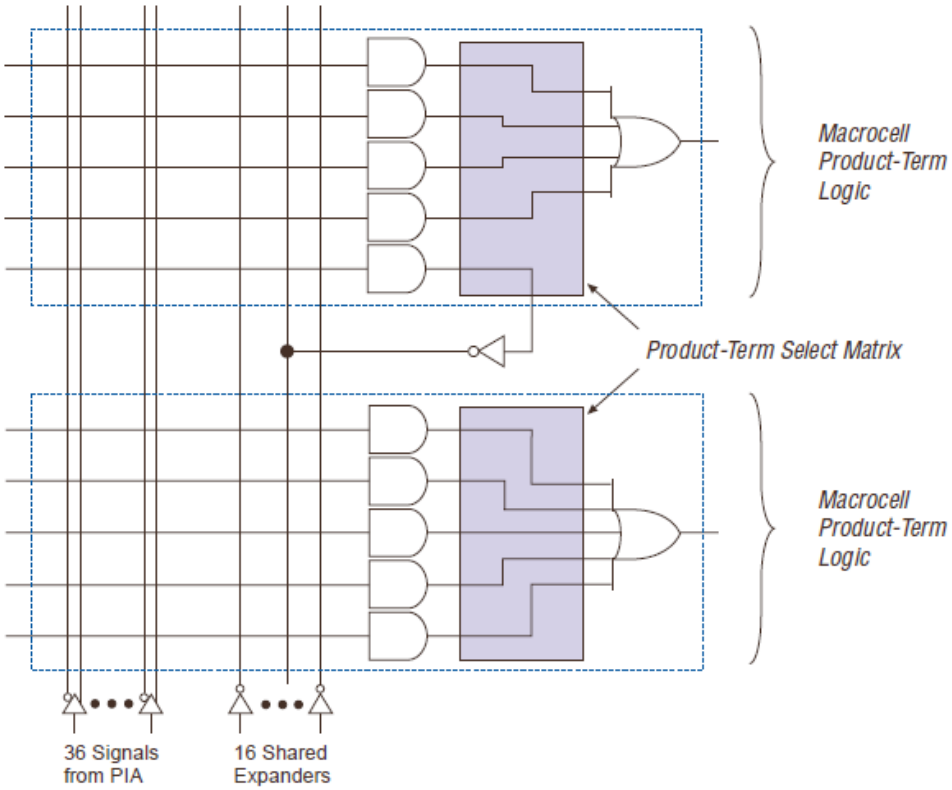
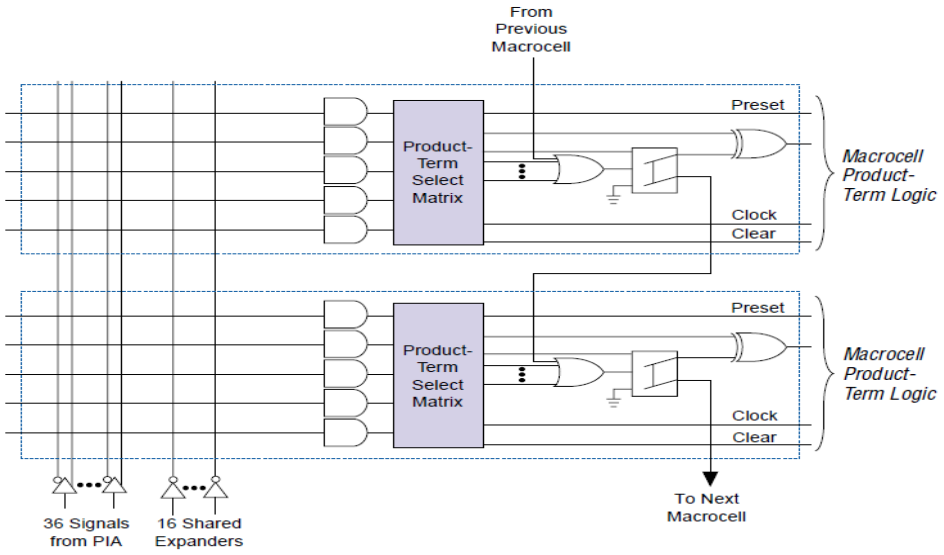


Figure 4 Functional diagram of shared expansion product term implementation

Parallel Expansion of Product Terms

Parallel extended product terms utilize unused product terms from adjacent acrocells to implement fast and complex logic functions. Parallel extended product terms allow up to 20 product terms to be directly output to the " OR " logic of the macrocell. These 20 product terms mainly come from: 5 parallel extended product

terms provided by this macrocell and 15 parallel extended product terms provided by adjacent macrocells in the same LAB.



Functional Block Diagram

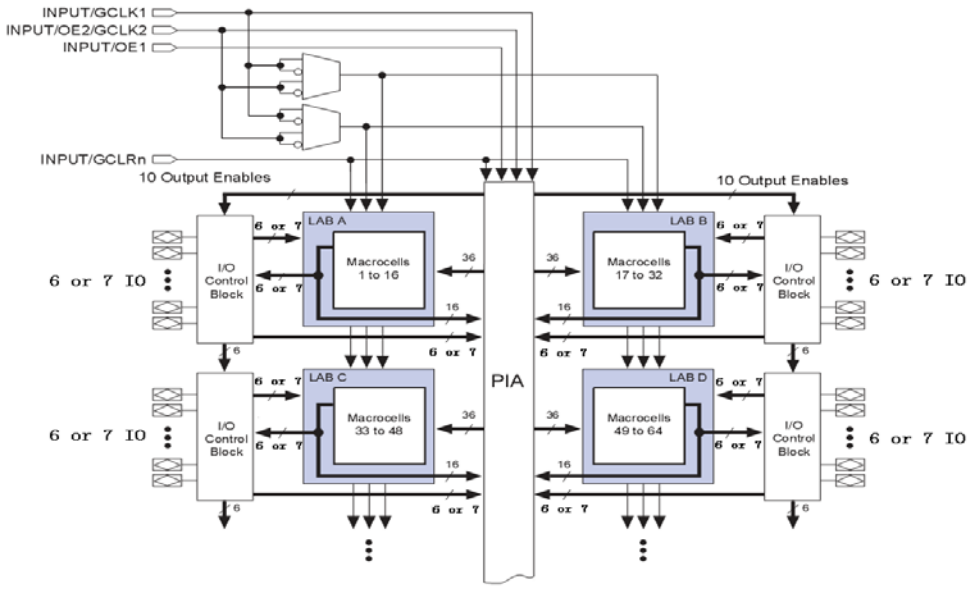


Figure 5 BST7512AE functional block diagram