BST74801

1. Product Overview

The BST74801 low dropout linear regulator provides an easy-to-control, robust power solution for a wide range of applications. The user-programmable soft-start function effectively reduces the pressure on the input power supply by reducing the inrush current during startup. The monotonic soft start is well adapted to powering a variety of different types of processors and ASICs. The enable input and PG output can easily arrange the sequence of external regulators. Complete adaptability provides users with solutions that can solve FPGAs, DSPs and other devices with special startup requirements with sequential requirements.
The precise reference and error amplifier enable the chip to have a 2.5% tolerance under full load, linearity, temperature and process conditions. Each LDO can be stabilized with low-cost ceramic output capacitors, and the chip operates accurately over the -55°C to +125°C temperature range.

1. Quality Grade

Country, company and product model of alternative products

Our product model	Replacement product models	Alternative Products Company	Alternative product country
BST 74801	TPS74801	TI	USA

2. Product Features

BST74801 is a 1.5A LDO voltage regulator with programmable soft-start function, output voltage 0.8V~3.6V, adopts NMOS output power tube structure, with enable control, temperature protection, over-current protection, under-voltage protection, soft-start function, PG function, mainly used to provide stable power supply for FPGA, DSP, ASIC and microprocessor.

- Adjustable output (0.8V to 3.6V).
- The soft start (SS) terminal provides a linear start time by setting an external capacitor.
- 2% accuracy over full load, temperature, linear conditions.
- Voltage drop to 300mV (max) at 1.5A.
- Fast transient response.
- Open drain PG terminal.
- Enable high level is effective.
- With undervoltage lockout, overcurrent protection, temperature protection function.
- 20-pin QFN20 package.

3. Functional Block Diagram

The overall architecture of BST74801 is shown in the figure below:

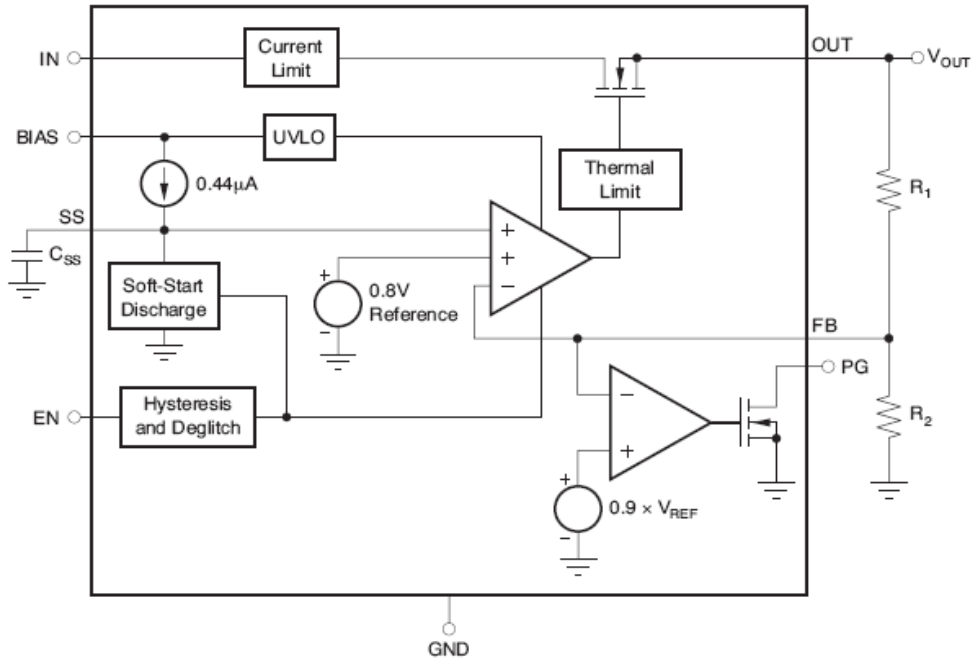

Figure 1Functional module diagram

4. Product appearance

The device adopts leadless ceramic sealed QFN20 package, and its dimensions refer to the provisions of GB/T 7092-1993. The appearance is shown below.

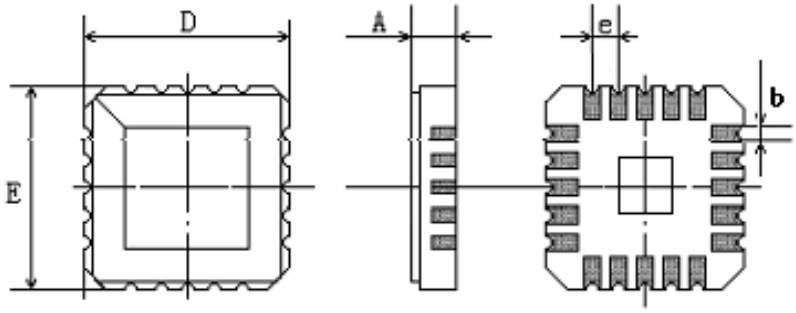

Figure 2Dimensions

Table 1Dimensions

Unit is mm

Dimension symbols	Numeric		
	Minimum	Nominal	maximum
D	6.90	-	7.10
E	6.90	-	7.10
A	-	-	2.5
b	-	0.35	-
e	-	0.65	-

5. Electrical properties

Unless otherwise specified, the electrical characteristics shall be as specified in Table 5 and shall apply over the full operating temperature range.

Table 2Electrical characteristics parameters

parameter	symbol	Test conditions (V_{EN} = V_{BIAS} =5V, V_{IN} = V_{OUT} +1V, I_{OUT} =10mA, -55°C≤ T_J ≤1 25°C)	Group A Grouping	Standard value		unit
				Minimum	maximum	
V_{IN} Voltage Range	V_{IN}		A1 A2 A3	VOUT + 0.3	5.5	V
V_{BIAS} Voltage Range	V_{BIAS}			2.7	5.5	V
Internal reference voltage	V_{REF}			0.7 84	0.8 16	V
Output voltage range	*VOUT*			V_{REF}	3.6	V
Output voltage accuracy	*VOUT*	3.6V≤V_{BIAS} ≤ 5.5V 1 0mA≤I_{OUT} ≤ 1.5A		-2	+2	%
Line Regulation	$V_{OUT(\triangle IOUT)}$	VOUT + 1V ≤VIN ≤ 5.5V		—	0.3	% /V
Load Regulation	*VOUTLR*				1	% /A
Low dropout voltage	V_{DO}	IOUT = 1.5A, VFB = 0V		—	0.3	V
V_{BIAS} voltage drop	V_{DOBIAS}			—	1.62	V
Output Current	I_{OUT}			1.5	—	A
Feedback pin current	I_{FB}			-1	1	μA
B IAS current	I_{BIAS}			—	3	mA
Shutdown current	I_{SHDN}	V_{EN} ≤0.4V, test V_{IN} terminal leakage current V_{BIAS} = 5.5 V, V_{IN} = 5.5 V		—	100	μA
Soft start charging current	I_{SS}	V_{SS} =0.4V		0.4	1.1	μA
Enable input high level	V_{EN} (high)			1.8	5	V
Enable input low level	V_{EN} (low)			0	0.4	V
Enable terminal hysteresis level	V_{EN} (hys)				100	mV
Enable terminal current	I_{EN}			-1	1	μA
PG trigger threshold	V_I	VOUT drops		80	9 4	% V_{OUT}
PG trigger hysteresis	V_Y			—	10	% V_{OUT}
PG output low voltage	V_{PG} (low)	IPG =1mA, V_{OUT} < VIT		—	0.5	V
PG terminal leakage current	I_{PG}	VPG =5V, V_{OUT} > VIT		—	5.0	μA
Startup time	t_{STR}	No capacitor is connected to the SS terminal.	A 9 A 10 A 11	—	200	μs
Functional testing	V_{EN} = V_{BIAS} = 5.0V, perform functional test according to the test program compiled according to the logical relationship of the device.		A7 A8A A8B			