

## BST74401

### 1. Product Overview

The BST74401 low dropout linear regulator provides an easy-to-control, robust power solution for a wide range of applications. The user-programmable soft-start function effectively reduces the pressure on the input power supply by reducing the inrush current during startup. The monotonic soft start is well adapted to powering various types of processors and ASICs. The enable input and PG output can easily arrange the sequence of external regulators. Complete adaptability provides users with solutions that can solve FPGAs, DSPs and other devices with special startup requirements with sequential requirements. The precise reference and error amplifier enable the chip to have a 2.5% tolerance under full load, linear, temperature and process conditions. Each LDO can be stabilized with low-cost ceramic output capacitors, and the chip works accurately over the temperature range of -55 °C to +125 °C.

### 2. Product Features

- soft-start ( SS ) terminal provides a linear start-up time by setting an external capacitor.
- At full load, temperature, linear conditions 2.5 % accuracy.
- Adjustable output ( 0.8V arrive 3.6V ).
- 3A When the pressure drops to 700mV (max).
- Fast transient response.
- Open Drain PG end.
- The high level of the enable terminal is valid.

### 3. Functional Block Diagram

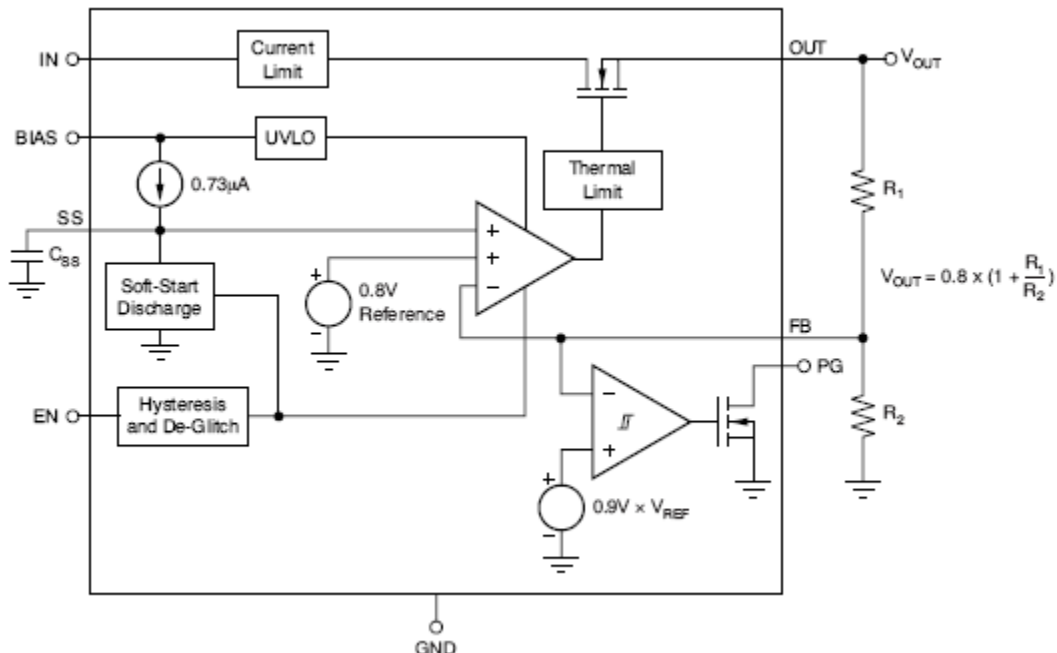


Figure 1. Functional Block Diagram

## Pin Information

### Pin Assignment Diagram

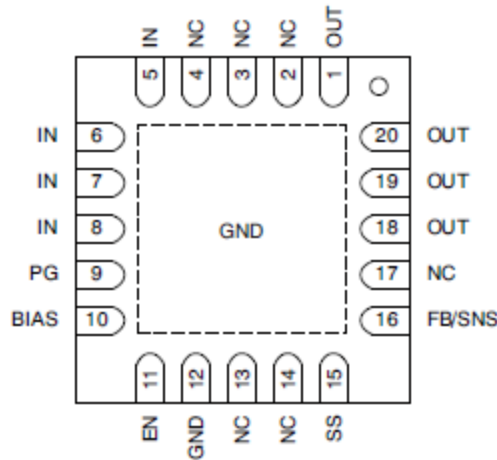


Figure 2. BST74401 pinout diagram

## Pin Description

Table 1. Pin Description

| Pin number          | symbol | Pin Description                                                                                                      |
|---------------------|--------|----------------------------------------------------------------------------------------------------------------------|
| 1, 18, 19, 20       | OUT    | Regulator output, no need to connect capacitors to stabilize the chip                                                |
| 2, 3, 4, 13, 14, 17 | NC     | No connection                                                                                                        |
| 5, 6, 7, 8          | IN     | Chip input                                                                                                           |
| 9                   | PG     | Open-drain output to indicate output voltage status                                                                  |
| 10                  | BIAS   | Error amplifier, reference, and internal control circuit bias input voltage                                          |
| 11                  | EN     | Enable terminal, when it is high level, the chip starts to work, when it is low level, the chip enters shutdown mode |
| 12                  | GND    | land                                                                                                                 |
| 15                  | SS     | Soft start terminal, this terminal is connected to a capacitor to set the start time                                 |
| 16                  | FB/SNS | This port is connected to an external voltage divider network to set the output voltage and cannot be left floating. |

## 4. Product appearance

### Ceramic CLCC20 package

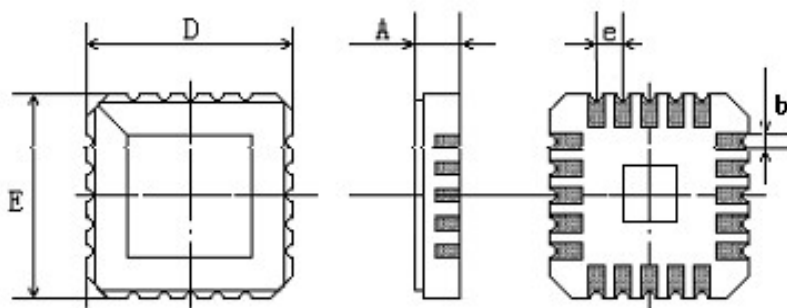


Figure 3. Ceramic CLCC20 package dimensions

Table 2 for dimensions

Table 2. Dimensions in millimeters

| Dimension symbols | Numeric |         |         |
|-------------------|---------|---------|---------|
|                   | Minimum | Nominal | maximum |
| D                 | 6.85    | -       | 7.20    |
| E                 | 6.85    | -       | 7.20    |
| A                 | 1.60    | -       | 2.0     |
| b                 | -       | 0.35    | -       |
| e                 | -       | 0.65    | -       |

The lead-out arrangement is shown in the figure below (top view):

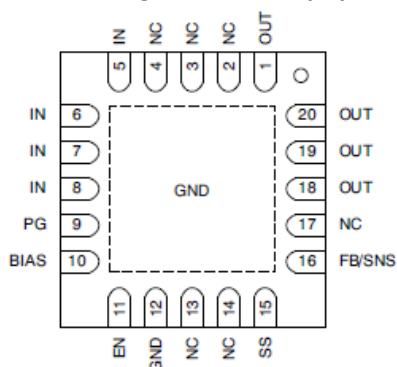


Figure 4. Ceramic CLCC20 package outline pin diagram

## Plastic QFN20 Package

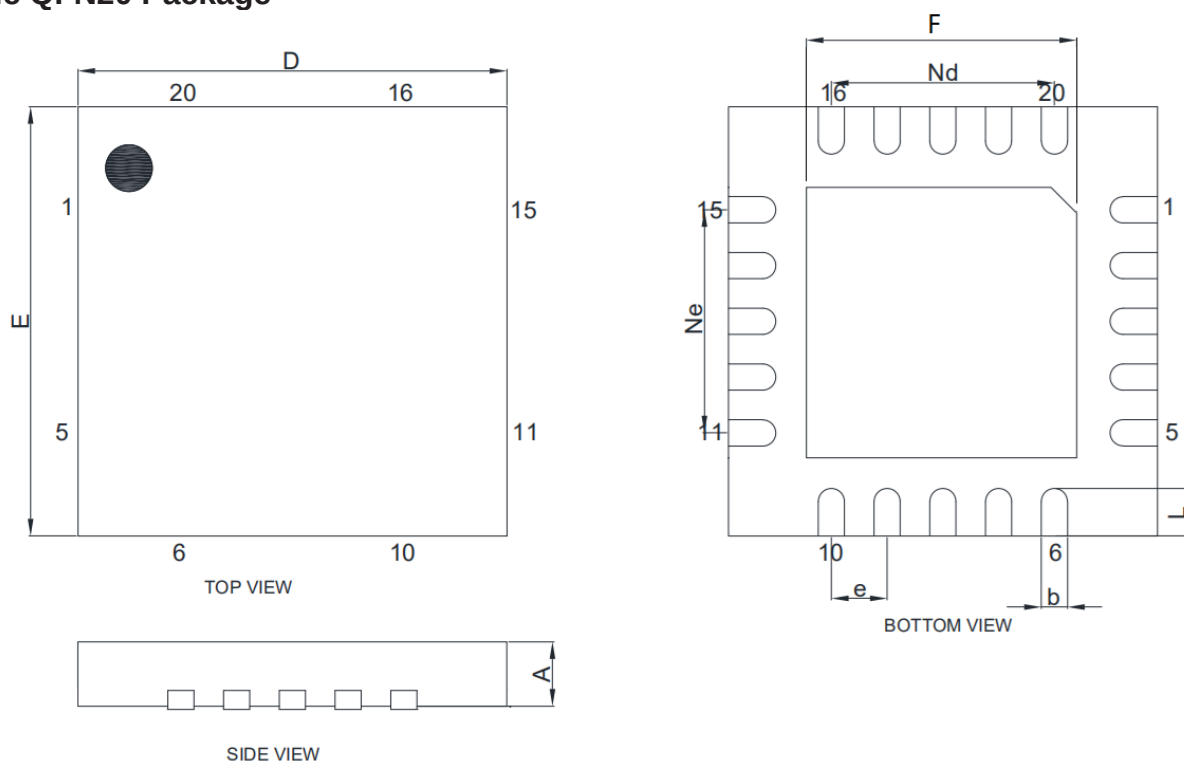


Figure 5. Plastic QFN20 package dimensions

Table 3. Dimensions in millimeters

| Dimension symbols | Numeric |         |         |
|-------------------|---------|---------|---------|
|                   | Minimum | Nominal | maximum |
| D                 | 4.90    | -       | 5.10    |
| E                 | 4.90    | -       | 5.10    |
| A                 | -       | 0.85    | -       |
| b                 | -       | 0.3     | -       |
| e                 | -       | 0.65    | -       |
| L                 | 0.45    | 0.55    | 0.65    |
| u                 | 0.1     | 0.2     | 0.3     |
| F                 | 3.05    | 3.15    | 3.25    |
| Ne                |         | 2.60    |         |
| Nd                |         | 2.60    |         |

The lead-out arrangement is shown in the figure below (top view):

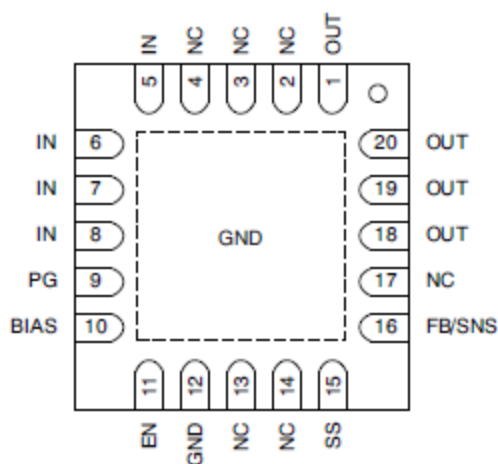


Figure 6 Plastic QFN20 package outline pin diagram

## 5. Electrical characteristics parameters

Table 4. Electrical properties

| parameter                     | symbol                                                                                                                                | condition                                                    | Minimum         | Maximum | unit        |
|-------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------|-----------------|---------|-------------|
| Input voltage range           | $V_{IN}$                                                                                                                              |                                                              | $V_{OUT} + 0.8$ | 5       | V           |
| BIAS Voltage range            | $V_{BIAS}$                                                                                                                            |                                                              | 2.75            | 5       | V           |
| Internal reference voltage    | $V_{REF}$                                                                                                                             |                                                              | 0.78            | 0.82    | V           |
| Accuracy ( 1 )                |                                                                                                                                       | $3.6V \leq V_{BIAS} \leq 5V$ , $50mA \leq I_{OUT} \leq 2.0A$ | -2.5            | +2.5    | %           |
| Line Regulation               | $V_{OUT} / V_{IN}$                                                                                                                    | $V_{OUT} (NOM) + 0.3 \leq V_{IN} \leq 5V$                    | —               | 1       | %           |
| Vin Pressure drop ( 2 )       | $V_{DO}$                                                                                                                              | $I_{OUT} = 2.0A$ , $V_{BIAS} = 5V$                           | —               | 700     | mV          |
| $V_{BIAS}$ voltage drop ( 2 ) |                                                                                                                                       | $I_{OUT} = 50mA$ , $V_{IN} = 5V$                             | —               | 1.62    | V           |
| BIAS Terminal current         | $I_{BIAS}$                                                                                                                            | $I_{OUT} = 50mA$                                             | —               | 6       | mA          |
| Shutdown Current ( $V_{IN}$ ) | $I_{SHDN}$                                                                                                                            | $V_{EN} \leq 0.4V$                                           | —               | 100     | uA          |
| Soft start charging current   | $I_{SS}$                                                                                                                              | $V_{SS} = 0.4V$                                              | 0.5             | 1.1     | uA          |
| Enable input high level       | $V_{EN}(high)$                                                                                                                        |                                                              | 1.8             | 5       | V           |
| Enable low level              | $V_{EN}(low)$                                                                                                                         |                                                              | 0               | 0.4     | V           |
| PG trigger threshold          | $V_I$                                                                                                                                 | $V_{OUT}$ decline                                            | 80              | 93.5    | % $V_{OUT}$ |
| parameter                     | symbol                                                                                                                                | condition                                                    | Minimum         | Maximum | unit        |
| PG output low voltage         | $V_{PG}(low)$                                                                                                                         | $I_{PG} = 1mA$ , $V_{OUT} < V_{IT}$                          | —               | 0.5     | V           |
| PG terminal leakage current   | $I_{PG}(1kg)$                                                                                                                         | $V_{PG} = 5V$ , $V_{OUT} > V_{IT}$                           | —               | 5       | uA          |
| Functional testing            | $V_{CC} = 5.0V$ , perform functional test according to the test program compiled according to the logical relationship of the device. |                                                              | —               |         |             |

Note 1: The adjustable chip is tested at 1.6V output, ignoring the tolerance of the external voltage divider resistor.

Note 2: Input-output voltage drop is defined as the input-output voltage difference when the output voltage is 2% lower than the normal voltage.