BST7185

1. Product Overview

The BST7185 series is a linear regulator with negative input, negative output, output current -500mA, ultra-noise, and high power supply rejection ratio. The input voltage is -2.3V to -5.5V, the maximum output current is -500mA, and it has good low noise performance while having high PSRR and linear and load adjustment characteristics. The chip has a fixed output version and an adjustable version, which can be applied to noise-sensitive analog circuits and RF circuits. This product uses a QFN8 package with an outer size of 2mm×2mm.

2. Product Features

- Output current - 500 mA.
- Low dropout voltage 190mV (25 °C).
- Low noise 10 μV RMS (100 Hz —100KHz).
- Low PSRR 73 dB (800 Hz).
- Quiescent current 0.9mA.
- Fixed output voltage : -1.8V, -2.5V, -3.3V, -5V ; adjustable output voltage range: -1.5V to -5V.
- Thermal protection function.

3. Functional Block Diagram

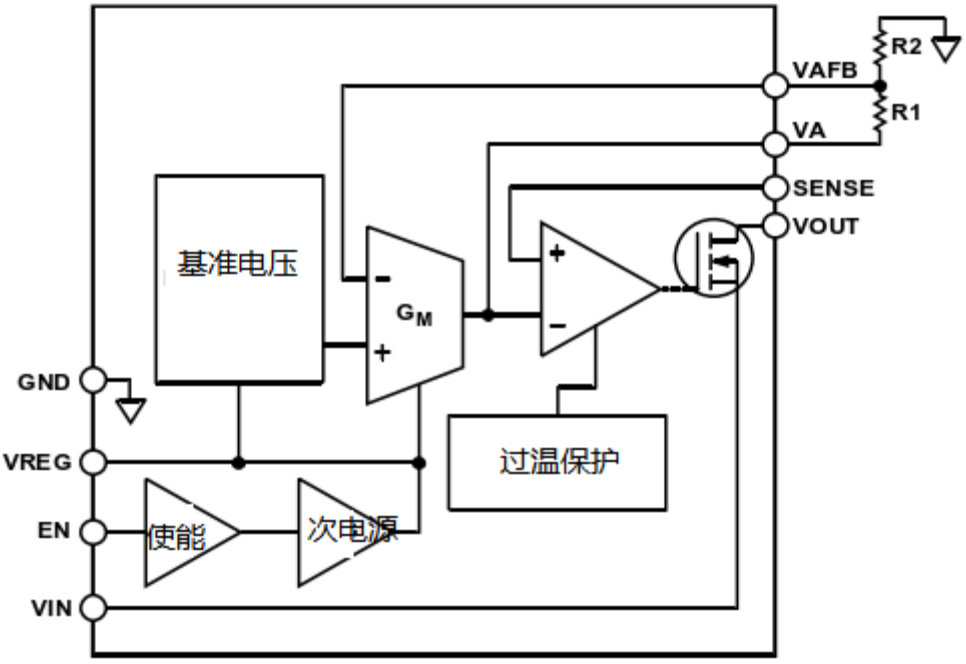

Figure 1. Functional Block Diagram

Pin Information

Pin Assignment Diagram

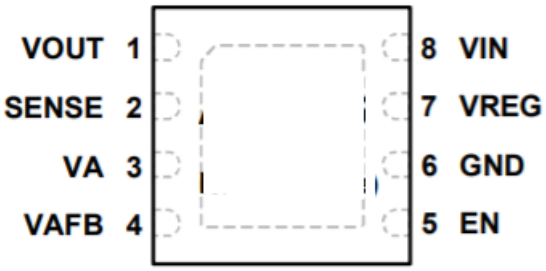

Figure 2. BST7185 series pinout diagram

Pin Description

Table 1. Pin Description

Pins	Pin Name	Functional Description
1	VOUT	output of the linear regulator
2	SENSE	Vout port detection terminal
3	VA	The output of the error amplifier
4	VAFB	The feedback terminal of the error amplifier
5	EN	Enable Port
6	GND	High level, ground
7	VREG	Secondary power supply - 1.8V power supply
8	VIN	Negative phase input

4. Product appearance

Plastic QFN 8 package

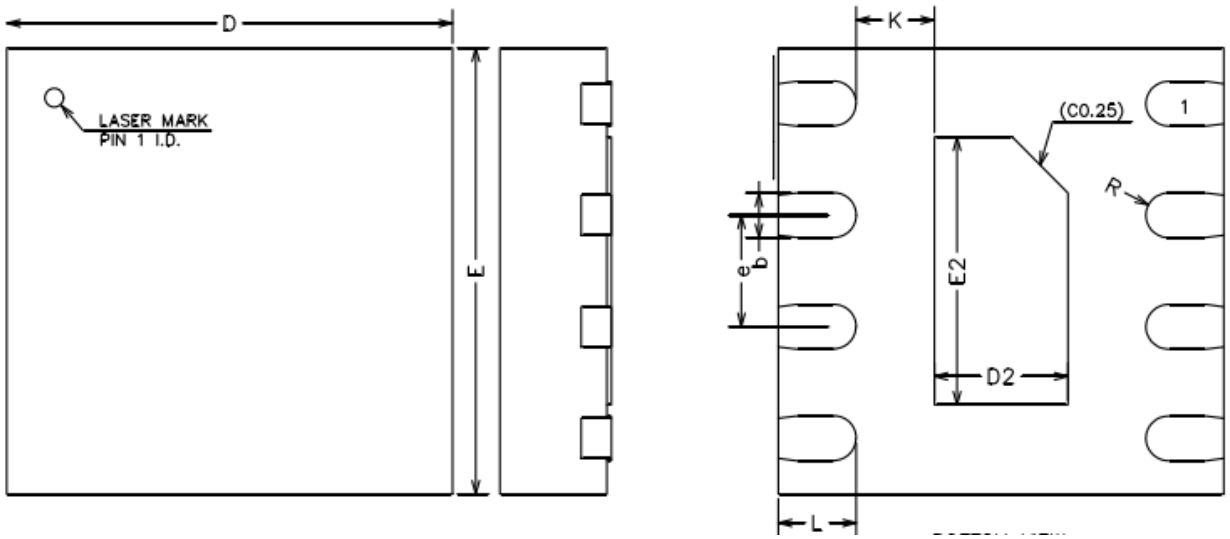

Figure 3. Plastic QFN 8 package dimensions

Unit is mm

Dimension symbols	Numeric		
	Minimum	Nominal	maximum
D	1.8	2	2.2
E	1.8	2	2.2
D2	0.4	0.6	0.8
E2	1	1.2	1.4
L	0.2	0.35	0.5
K	0.2	—	—
e	—	0.5	—
b	0.1	0.2	0.3

5. Electrical characteristics parameters

Table 2. Electrical properties

special sex	symbol	strip Item -2.3 V ≤ V_{IN} ≤ -5.5 *V*, V_{IN} = V_{OUT} - 0.5V, *CIN* = COUT = 4.7 μF, CAFB = 10 nF, CREG = CA = *1* uF Unless otherwise specified, -55 °C ≤ TA ≤ 125 °C	Limit value		unit
			Minimum	maximum	
Input voltage	V_{VIN}		-2 .3 -5.5		V
Load current	I_{LOAD}			-500	mA
Supply Current	I_{GND}	IOUT = 0		-0.9	mA
		IOUT = -500 mA		- 2. 8	mA
Shutdown current	I_{GND-SD}	EN = GND V_{IN} = -5.5V		-7	uA
Output Noise	$V_{outnoise}$	100Hz —100KHz, CAFB = 10nF	10 (Typical)		uVrms
Noise spectral density	VOUTNSD	10 Hz—1MHz, CAFB = 10nF	200 (typical)		nV/√Hz
Power Supply Rejection Ratio	PSRR	I_{OUT} = -500 mA, V_{OUT} =-3.3V, V_{IN} =-3.8V			
		800Hz	73 (Typical)		dB
		10 KHz	6 0 (Typical)		dB
		100KHz		45 (Typical)	dB
Output voltage accuracy	*VOUT*	-1 mA< I_{OUT} < -500 mA, V_{IN} = V_{OUT} -0.5 V or -5.5 V	-3	+3	%
Feedback voltage accuracy	V_{AFB}		-0.48 -0.5 -0.5 2		V
Line Regulation	ΔV_{OUT} / ΔV_{IN}	V_{IN} = V_{OUT} -0.5 V or -5.5 V		+0.3	% /V
Load Regulation	ΔV_{OUT} / ΔI_{OUT}	IOUT = -10mA - -500mA	1.8		% /A
Input bias current	$I_{SENSE IBIAS}$	-1 mA< I_{OUT} < -500 mA, V_{IN} = V_{OUT} -0.5 V or -5.5 V		-10	nA
Dropout voltage	$V_{dropout}$	IOUT = -500 mA	19 0 (typical) 360		mV
Current Limitation	I_{limit}		-2		A
Thermal Shutdown	T_S		1 6 0 (typical)		℃
Opening time	T_{start}	*CAFB* = 10 nF, *CA* = 1 uF	45 (typical)		ms
Undervoltage lockout threshold	$V_{UVLOrise}$	When VIN drops from 0V to -5.5V, the device starts working.	-1. 85		V
Undervoltage lockout threshold	$V_{UVLOfall}$	When VIN rises from -5.5V to 0V, the device does not work	-1.4		V
EN input (negative phase) Logic High	$V_{EN-NEG-HIGH}$	From off to on	-1.3		V
EN input (negative phase) Logic Low	$V_{EN-NEG-LOW}$	From on to off	-0.4		V
EN input (negative phase) Leakage Current	I_{EN-LKG}	EN =VIN		1.6	uA
EN input (positive phase) Logic High	$V_{EN-POS-HIGH}$	From off to on	1.25		V
EN input (positive phase) Logic Low	$V_{EN-POS-LOW}$	From on to off	0.5		V
EN input (positive phase) Leakage Current	I_{EN-LKG}	VEN =5V, Vin = -5.5V	12		uA

6. Functional Description

Overview

The typical application of BST7185 is shown below.

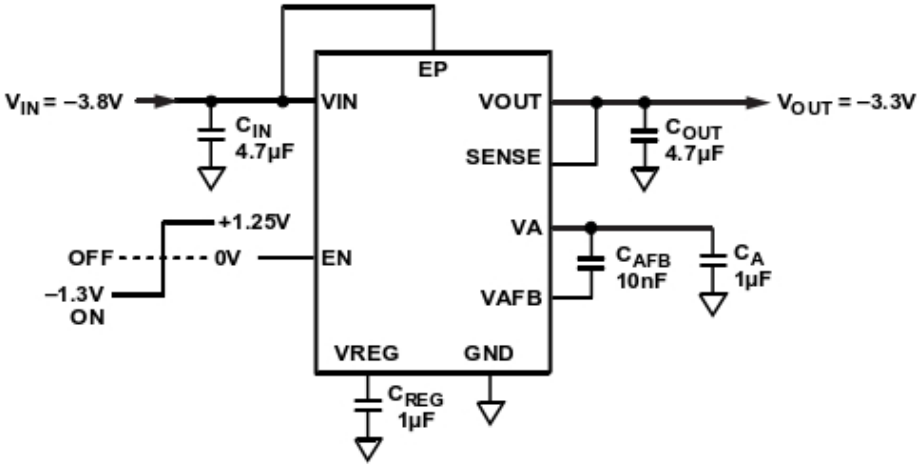

Figure 3 Typical application diagram of fixed output version

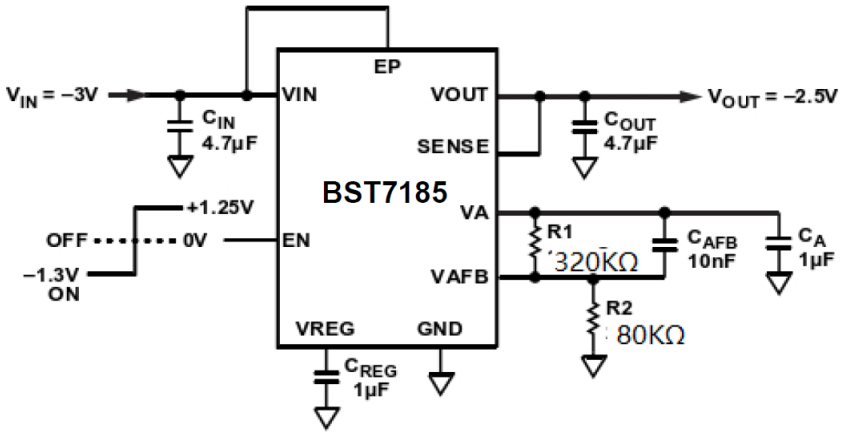

Figure 4. Typical application diagram of adjustable output version

Functional Description

The BST7185 series is a linear regulator with an output current of -500mA, ultra-noise, and high power supply rejection ratio. The input voltage is -2.3V to -5.5V, and the maximum output current is -500mA . It has good low noise performance and high PSRR and linear and load adjustment characteristics. This chip is used in analog circuits and RF circuits that are sensitive to noise.

The enable circuit of BST7185 allows the chip's internal secondary power supply VREG to generate a -1.8V voltage, and then generates an internal reference voltage of -0.5V, which is used as the input of the error amplifier. The error amplifier uses an external series resistor, the output terminal VA, and the feedback port VAFB to adjust the error amplifier's output voltage VA. The VA voltage passes through a buffer circuit in the form of unit gain negative feedback to generate the LDO's output voltage VOUT.

Adjustable version

of BST7185 is -2.3V to -5.5V, the adjustable output voltage range is -1.5V to -5V, and the input voltage and output voltage have a voltage difference of at least 0.5V, $V_{IN} = V_{OUT} - 0.5V$. By adjusting the series feedback resistors R_1 and R_2, the output voltage value can be achieved, as shown in the following formula.

$$Vout = -0.5 \times \left(1 + \frac{R_1}{R_2}\right)$$

Enable Port

The enable port EN controls the device's working and shutdown states. When the EN port voltage is at (+1.25V, +5V) or the EN port voltage is at (-1.3V, -5.5V), the device is in the working state. When the EN port voltage is in the range of -0.4V to 0.5V, the device is in the shutdown state.

Power supply recommendations

The device is designed to operate over an input voltage supply range of -2.3 V to -5.5 V. The input voltage range provides enough headroom for the device to obtain a regulated output.

Output Capacitor

In order to ensure the stability of the loop, the output port Vout is connected to a 4.7uF capacitor, and the ESR resistance of the capacitor must be greater than or equal to 10mΩ.

CA and C_{AFB} capacitors

To ensure the stability of the error amplifier loop, the error amplifier output terminal VA is connected to capacitor CA = 1uF. To reduce noise, capacitor CAFB = 10nF is added . The larger the capacitance of the capacitor, the smaller the noise and the longer the startup time.

Undervoltage lockout function

In order to ensure the stability of the device, an undervoltage lockout circuit is designed. When the power supply voltage VIN drops to -1.85V, the undervoltage lockout function does not work and the device works normally. When the power supply voltage VIN rises to -1.4V, the undervoltage lockout function takes effect and the device cannot work normally.

Over temperature protection function

In order to protect the device from overheating and burning when the output is overloaded, an over-temperature protection function is designed. When the junction temperature rises to 160°C, the over-temperature protection function shuts down the device; when the junction temperature drops to 150°C, the device returns to normal operation.

Dropout voltage

The voltage difference between the V IN and V OUT pins when operating at a specific output current . The dropout voltage can also be expressed as the voltage drop of the power tube at a specific output current, and the power tube resistance $R_{DS(ON)}$ when the power tube operates in the linear region . Therefore, the dropout voltage can be defined as ($V_{DO} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{OUT}$). For normal operation, the recommended LDO operating range is: the input voltage and output voltage have a voltage difference of at least 0.5V $V_{IN} = V_{OUT} - 0.5V$ to obtain good transient response and PSRR performance.

Heat dissipation considerations

Thermal protection limits the power dissipation of the device . When the power dissipation on the power switch is too large ($P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$) and causes the operating junction temperature to exceed 1 60 °C, the overtemperature protection circuit starts to operate and turns off the power switch. After the junction temperature cools by 10 °C, the power tube turns on again. The junction temperature should not exceed the absolute maximum junction temperature $T_{J(MAX)}$ listed under Absolute Maximum Ratings to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the surrounding airflow rate, and the difference between the junction and ambient temperature. The maximum power dissipation can be calculated using the following formula .

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA)}$$

where $T_{J(MAX)}$ is the maximum junction temperature, TA is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

7. Application suggestions

The input and output voltage selection of the chip is defined in the chip's instruction manual. This section mainly focuses on the precautions during welding and debugging.

Anti-static packaging is used during the transportation process, but if you are not careful during the entire process from before and after welding to the completion of debugging and assembling the board into the chassis, static damage will occur, reducing the reliability of the integrated circuit.

8. Precautions for use

The device must be handled with anti-static measures.

The device operation precautions are as follows:

- The device should be operated on an anti-static workbench;
- Test equipment and apparatus should be grounded;
- Do not touch the device leads;
- Devices should be stored in containers made of conductive materials;
- Avoid using plastic, rubber or silk fabrics that can cause static electricity in the MOS area;
- If feasible, maintain relative humidity above 50%.

9. Ordering Information

Table 2. Product Ordering Information

model	Package	Packaging materials	Quality Grade	Detailed specifications	Product Status
BST7185	QFN8	Plastic packaging	Military temperature level	Q/BST XXX	First Sample