BST7150

1. Product Overview

BST7150 is an ultra-noise high PSRR linear voltage regulator circuit . Input voltage 6.2 V to 16 V, maximum quiescent current 7 mA at zero load , maximum drive 800mA load current, suitable for wide input voltage, high performance applications. BST7150 has excellent noise performance and high PSRR, and can be used to power noise-sensitive analog circuits and RF circuits. Input/output capacitors ceramic 10 uF ensure system stability. Undervoltage, overcurrent and overheating protection functions are integrated on the chip. It uses 8 -pin ceramic C SOP8 package and plastic PDFN8 package .

2. Product Features

- Input voltage range: 6.2 V to 16 V
- Fixed output voltage: 5.0V
- Output integrated RMS noise: 2μVrms @10-100KHZ
- Input/output 10 uF ceramic capacitors to ensure stability
- Operating current without load current: 7mA
- Maximum drivable load current : 800mA
- Minimum input - output voltage difference: 1V
- ± 3 % Total Output Voltage Regulation Accuracy
- Power supply rejection PSRR : 90dB@10KHZ
- Overvoltage, overcurrent and overtemperature protection
- 8 -pin CSOP8 and PDFN 8 packages

3. Functional Block Diagram

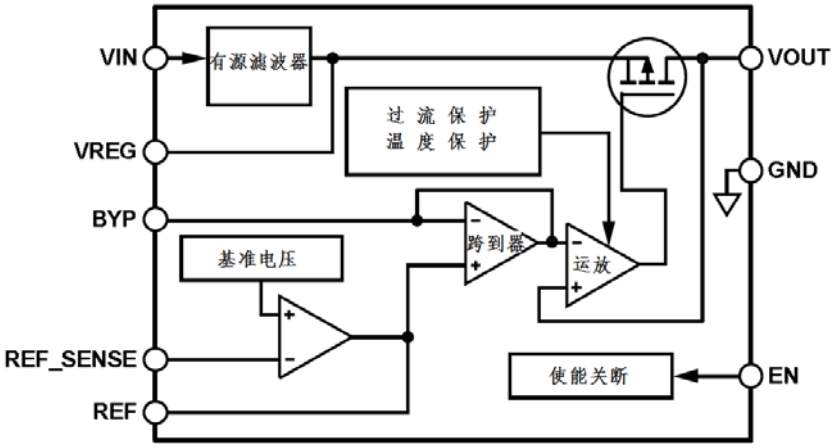

Figure 1 Functional block diagram

4. Product appearance

CSOP8 Package Information

Figure 2. CSOP8 package outline

Dimension symbols	Numeric		
	Minimum	Nominal	maximum
A	—	—	3.00
b	0.35	—	0.45
e	—	1.27	—
D	5.85	—	6.15
E	4.85	—	5.15
H_E	6.50	—	7.10

P DFN 8 Package Information

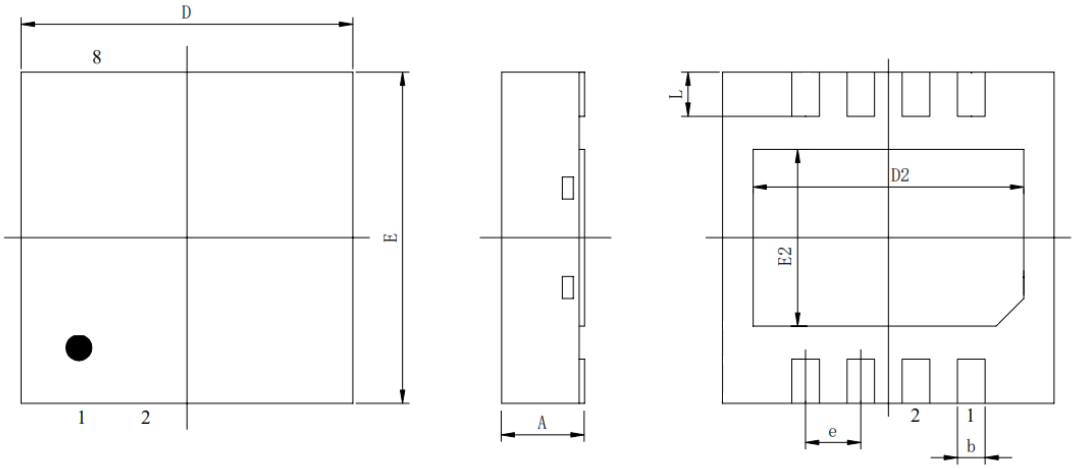

Figure 3. PDFN8 package outline

Unit is mm

Dimension symbols	Numeric		
	Minimum	Nominal	maximum
A	0.7	0.75	0.8
b	0.20	—	0.3
e	—	0.50	—
D	2.90	—	3.10
E	2.90	—	3.10
D2	2.30	2.45	2.60
E2	1.50	1.60	1.70
L	0.35	0.4	0.45

Pin Definition

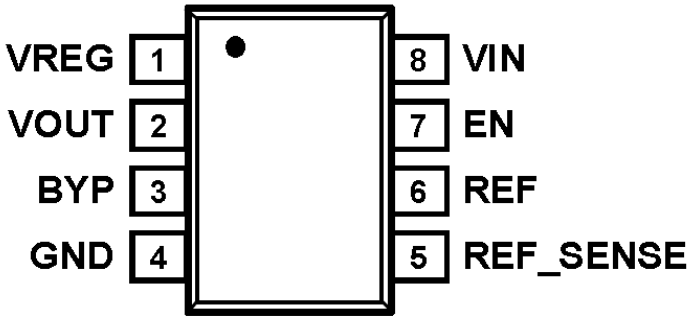

Figure 4. BST7150 pin definition

Pin Description

Table 1. Pin Description

Pin number	Pin Symbols	Functional Description
1	VREG	Active filter output voltage, connect 10uF or larger capacitor to ground
2	VOUT	Regulator output voltage, connect 10uF or larger capacitor to ground
3	BYP	Low noise bypass capacitor, 1uF capacitor connected to ground to reduce output noise
4	GND	land
5	REF_SENSE	Low noise reference voltage output detection terminal, must be connected to REF, cannot be connected to VOUT and ground
6	REF	Low noise reference voltage output terminal, connected to ground with 1uF capacitor, connected to REF_SENSE
7	EN	Enable terminal, high level is valid, EN=VIN at self-startup
8	VIN	Input power, connect a 10uF or larger capacitor to ground

5. Electrical parameters

Table 2. Electrical properties

characteristic	symbol	condition (Unless otherwise specified, V_{IN} = 6.2V, I_{OUT} =10mA, C_{IN} = C_{OUT} = C_{REG} =10μF, C_{REF} = C_{BYP} = 1 μF, -55°C ≤ T_A ≤125°C)	Limit value		unit
			Minimum	maximum	
Input voltage range	V_{IN}		6.2	16	V
Output Current	I_{OUT}		800	—	mA
Quiescent Current	I_{GND}	I_{OUT} = 0mA	—	7	mA
		I_{OUT} = 800mA	—	12	mA
Shutdown current	I_{GND-SD}	VEN = GND	—	10	μA
Output voltage	V_{OUT}		4.85	5.15	V
Voltage Regulation	$\triangle V_{OUT} / \triangle V_{IN}$	6.2V≤ V_{IN} ≤16V	—	0.05	%/V
Current Regulation	$\triangle V_{OUT} / \triangle I_{OUT}$	1mA≤ I_{OUT}≤800mA	—	2	%/A
Limiting threshold current	I_{LIMIT}		1	1.8	A
Minimum input-output pressure difference	$V_{DROPOUT}$	I_{OUT} = 800mA		1	V
VIN undervoltage protection threshold	V_{VIN_UVLO}	VIN_{rises}	—	4.49	V
		VIN_{drops}	3.85	—	V
EN enable input high level voltage	V_I	6.2V≤ V_{IN} ≤16V	3.2	—	V
EN enable input low level voltage	V_{IL}	6.2V≤ V_{IN} ≤16V	—	0.8	V
EN Enable Input Leakage Current	VI_{-LKG}	VEN = V_{IN} or VEN = GND	-1	1	μA
Output noise	V_{OUT_NOISE}	T_A = 25°C ,10 Hz to 100 kHz	—	2	μV rms
Power Supply Rejection Ratio	PSRR	T_A= 25°C, f=100Hz, I_{OUT} =100 mA	90	—	dB
Startup time	T_{START_UP}		—	5	ms
a. Sampling is performed only for initial qualification or design changes5 (0).					