BST7104

1. Product Overview

The BST7104 developed in this project is a CMOS low dropout linear regulator with an operating range of 3.3V to 20V and an output current of up to 500mA. This high output voltage LDO is ideal for high performance analog and mixed signal circuit regulation working on 19V to 1.22V rails. Using an advanced internal structure, it provides high power supply rejection, low noise, and excellent linearity and load transient response can be obtained through a small 1 microfarad ceramic output capacitor.

2. Product Features

- Input voltage: 3.3V～20V.
- Output adjustable range: 1.22V~V_{IN}-V_{DO}.
- Maximum output current: 500mA.
- Package type: DFN8.
- Working environment temperature: −55 °C～ 125 °C.
- Storage temperature range: −65 °C～ 150 °C.
- Functionally compatible with foreign models: BST7104.

3. Functional Block Diagram

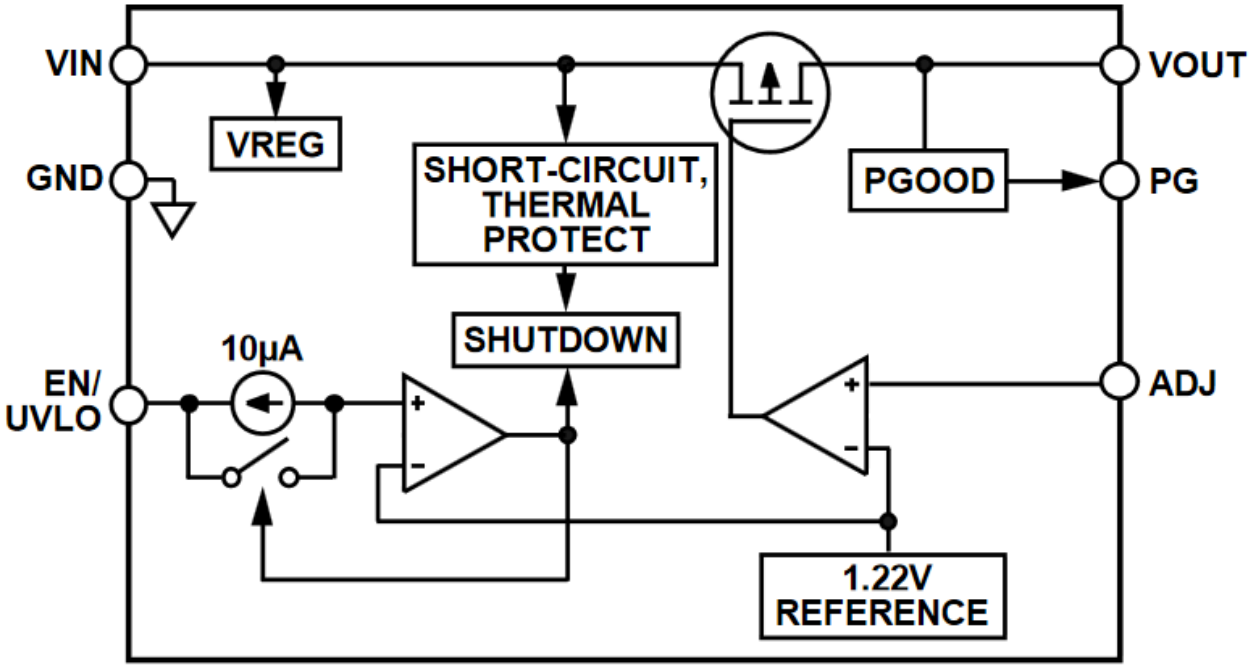
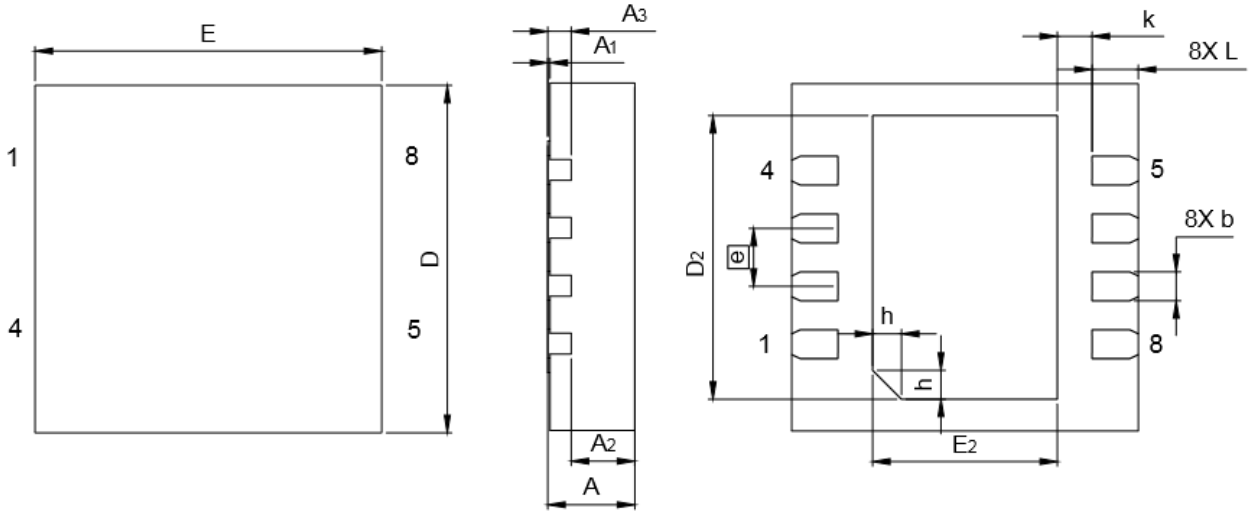


Figure 1. Functional Block Diagram

Packaging information

BST7104 packaging information

The BST7104 package outline and pin arrangement are shown in the figure below.



尺寸符号	数值，单位：mm		
	最 小	公 称	最 大
A	0.70	—	0.80
A_1	0.00	—	0.05
A_2	0.50	—	0.60
A_3	—	0.20	—
b	0.20	—	0.30
D(E)	2.90	—	3.10
D_2	2.35	—	2.55
E_2	1.50	—	1.70
e	—	0.50	—
h	0.20	—	0.30
L	0.35	—	0.45
k	0.20	—	—

The lead-out arrangement is shown in the figure below (top view):

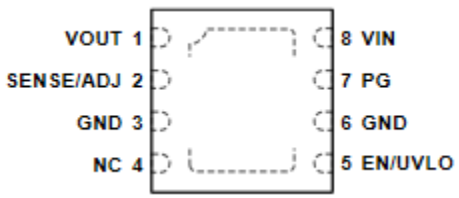


Figure 2. BST7104 package outline and pin arrangement

The BST7104 pin description is shown in the following table.

Table 1. BST7104 pin description

PIN number	symbol	describe
1	VOUT	Regulated output voltage. Connect a 1 microfarad or larger capacitor from VOUT to ground.
2	SENSE/ADJ	Sense. Measures the actual output voltage at the load and feeds back to the error amplifier. Connect sense as close as possible to the load to minimize the effect of IR drop between the regulator output and the load. This feature is only used for fixed voltages. Adjust input ADJ. An external resistor divider sets the output voltage. This function applies only to adjustable voltages.
3	GND	land
4	NC	Do not connect this PIN
5	EN/UVLO	Enable Input EN. Drive EN high to enable the regulator. Drive EN low to disable the regulator. For automatic startup, connect EN to VIN. Programmable Undervoltage Lockout UVLO When the programmable undervoltage lockout UVLO function is used, the upper and lower thresholds are determined by the programming resistors.
6	GND	land
7	PG	Power Good. This open-drain output requires an external pull-up resistor to VIN or VOUT. If the part is shut down, in current limit, thermal shutdown, or drops below 90% of the nominal output voltage, the PG pin immediately transitions to a low voltage. If the power good feature is not used, the pin can be left open or tied to ground.
8	VIN	Regulator input power supply. Pass VIN to GND through a 1 microfarad or larger capacitor.
	EPAD	Exposed Pad. Exposed pad on the bottom of the package. EPAD improves thermal performance and is electrically connected to GND inside the package. It is strongly recommended to connect EPAD to ground on the board.

4. Electrical parameters

The electrical characteristics are the best indicators that this series of products can achieve. Different quality levels and packaging forms are slightly different. Please refer to the corresponding detailed specifications for details.

Table 2. Electrical properties

parameter	Logo	condition	Minimum	Typical Value	Maximum	unit
Input voltage range	V IN		3.3		20	V
Working power supply current	I GND	I_{OUT} = 500 mA, V_{IN} = 10 V, T_J = −55°C to +125°C			2600	μA
Shutdown current	I GND-SD	EN = GND, V_{IN} = 12 V, T_J = −55°C to +125°C			175	μA
Input flip current	I REV-INPUT	EN = GND, V_{IN} = 0 V, V_{OUT} = 20 V, T_J = −55°C to +125°C			50	μA
Input voltage accuracy						
Fixed output voltage accuracy	VOUT	1 mA < I_{OUT} < 500 mA, V IN = (V_{OUT} + 1 V) to 20 V, T_J = -55°C to 125°C	-2.25		+2	%
Adjustable output voltage accuracy	V ADJ	1 mA < I_{OUT} < 500 mA, V_{IN} = (V_{OUT} + 1 V) to 20 V,T_J = -55°C to 125°C	-3.25		+3	V
Linear Regulation	ΔV OUT /ΔV IN	V_{IN} = (V_{OUT} + 1 V) to 20 V, T_J = −55°C to +125°C	-0.1		+0.1	%/V
Load Regulation 1	Δ V OUT/ Δ I OUT	I_{OUT} = 1 mA to 500 mA, T_J = −55°C to +125°C			1.75	%/A
Adjustable input bias current	ADJ I-BIAS	1 mA < I_{OUT} < 500 mA, V_{IN} = (V_{OUT} + 1 V) to 20 V, ADJ connected to V_{OUT}		100		nA
Sensing Input Bias Current	SENSE I-BIAS	1 mA < I_{OUT} < 500 mA, V_{IN} = (V_{OUT} + 1 V) to 20 V, SENSE connected to V_{OUT} , V_{OUT} = 1.5 V		10		μA
Output voltage difference 2	V DROPOUT	I_{OUT} = 500 mA, T_J = −55°C to +125°C			850	mV
Opening time 3	t START-UP	V = 5 V		1000		μs
Current limit threshold 4	I LIMIT		625	775	1000	mA
PG output logic level						
PG output logic high	PG HIGH	IOH < 1 μA	1.0			V
PG output logic low	PG LOW	IOL < 2 mA			0.4	V