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BST3L4G16

DRAM DDR3 4G Product Overview

I. Functional Description

The BST3L4G 16-bit 4Gb synchronous dynamic random-access memory (SDRAM) is a double-data-rate DDR3 DRAM circuit fabricated using a high-speed CMOS process. It employs an 8-bank structure, with each bank consisting of 32M x 16 bits. The circuit's command and address signals are synchronized with an external clock, CLK, while the data signal is synchronized with the DQS signal. The logic state of each signal is determined by sampling on the rising edge of CLK.

BST3L4G16 circuit's various operation instruction sequences and packaging are compatible with Micron 's MT41K256M16HA-107.

II. Overview

• Operating voltage: Vcc = Vccq = 1.35V ± 0.067V, compatible 1.5V±0.075V

• Storage capacity: 4Gbit

Memory structure: 256Mbx16 (32Mbx16x8 banks)

Data rate:
1866Mbps

• Double rate: data signal is latched on both edges of the system clock

Programmable CAS Latency

Fixed burst length (BurstLengths):

Supports self-refresh and auto-refresh modes

- Auto refresh interval:
 - 64ms, T_C less than 85 °C
 - 32ms, TC =greater than 85 °C

Package type:
BGA96 (plastic package)

• Temperature range: -55°C to +125°

• Quality grade: Enhanced temperature grade, QB grade, Aerospace grade

- Radiation resistance:
 - Total dose of 100Krad (Si)
 - Single event lock-in LET > 75MeV-cm²/mg



III. Recommended operating conditions

• Power supply voltage (V_{DD}, V_{DDQ}): 1.35±0.067V

• Reference voltage (V=(DC), VREFDQ (DC)): 0.5VDD ± 0.01VDD

• Input high level voltage (V_{IH}): 0.85V

• Input low level voltage (V_{IL}): 0.65V

• Operating temperature range (T_A):- 55 °C ~ +125 °C

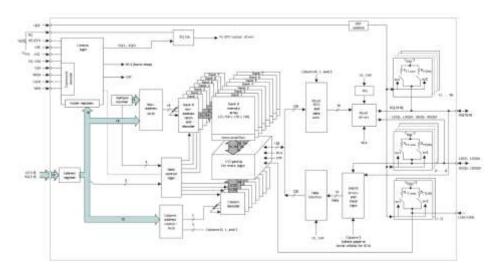
• Operating frequency (f): 933MHz

IV. Operational measures

• The device should be operated on an anti-static workbench or with finger cots;

- Test equipment and apparatus should be grounded;
- Do not touch the device leads:
- Devices should be stored in containers made of conductive materials (e.g)., special boxes for integrated circuits);
- Avoid using plastics, rubber or silk fabrics that may cause static electricity during production, testing, use and transportation;
- The relative humidity should be kept above 50%±30% as much as possible.

V. Principle Block Diagram



Picture 1.