

BST3L16G32

DRAM DDR3 16G Product Overview

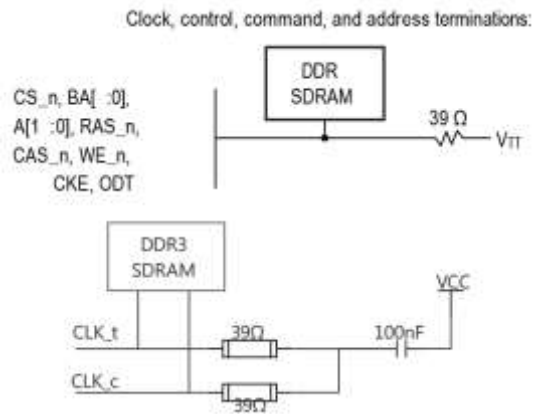
I. Functional Description

BST3L16G32 16Gb synchronous dynamic random-access memory (SDRAM) is a double-bit-rate DDR3 dynamic random-access memory (DRAM) circuit manufactured using a high-speed CMOS process. It is packaged from four 4Gb DDR3 SDRAM chips. Each chip utilizes an eight-bank structure, with each bank measuring 64M x 8 bits, ultimately achieving a 16Gb storage capacity. The circuit's command and address signals are synchronized with an external clock, CLK, while the circuit's data signal is synchronized with the DQS signal. The logic state of each signal is determined by sampling on the rising edge of CLK.

BST3L16G32 circuit's various operating instruction sequences and packaging are compatible with Mercury 's W3J512M 32.

I. Main indicators

- Working voltage: $V_{CC} = V_{CCQ} = 1.35V \pm 0.067V$, compatible 1.5V±0.075V
- Storage capacity: 16Gbit
- Storage structure: 512Mbx32 (64Mbx8x8banksx4chips)
- Data rate: 1866Mbps
- Double rate: data signal is latched on both edges of the system clock
- Programmable CAS Latency
- Fixed burst length (Burst Lengths): 8
- Supports self-refresh and auto-refresh modes
- Auto refresh interval:
 - 64ms, T_C less than 85°C
 - 32ms, T_C greater than 85°C
- Package type: BGA204 (plastic package)
- Quality grade: Enhanced temperature grade, QB grade, Aerospace grade
- Radiation resistance:
 - Total dose TID 100Krad (Si)
 - Single event lockup LET > 75MeV · cm²/mg



Picture 2.

Note:

- Address/control/clock termination resistors are included in the package.
- Calibration resistors (RZQs) are included in the package.
- The RESET_n pin is not internally pulled up.