BST32P FPGA supporting memory

Product Brochure

Ver3.2

Revision History

Edition	Change Description	Change order number	Change Person	Change Date	Re-mark
V1.00	Initial release	NA	Que Xiaoqian	2015/3/3	
V2.00	Add FBGA product information to modify order information	NA	Que Xiaoqian	2016/5/3	
V3.00	Complete package size information and power supply sequence requirements	NA	Que Xiaoqian	2019/3/25	
V3.1	The data retention period in the "BST32P Application" section was changed from 10 years to 20 years and the condition at room temperature was added; The company name was changed to “Stock Co., Ltd.”	NA	Que Xiaoqian	2021/12/21	
V3.2	Add application schematic	NA	Xia Ming-gang	2022/06/26	

I. Product Overview

The BST32P of Chengdu HuaWei Electronics Technology Co., Ltd. has a storage capacity of 32Mbits and supports master-serial, slave-serial, master-parallel and slave-parallel FPGA configuration modes. It is pin-to-pin compatible with the Xilinx XCF32PVO48C configuration chip.

II. Product Features

- In-circuit programmable PROM to configure Xilinx and compatible FPGAs
- The latest low-power CMOS NOR flash structure
- Supports more than 20,000 program/erase cycles
- Meets military temperature grades -55°C to +125°C
- Support IEEE 1149.1/1532 protocols
- JTAG commands can be used to initialize FPGA configuration
- Supports multi-chip cascading to store longer bit streams
- Dedicated I/O voltage (VCCJ) to support JTAG boundary scan
- The core voltage is 1.8V, and the I/O power supply voltage is 3.3V/2.5V/1.8V
- Design Versioning technology allows storage and access of up to four configuration versions
- Hardware data decompression supports Xilinx's latest compression technology

III. Block Diagram

The block diagram of the BST32P working platform is shown in Figure 1 below:

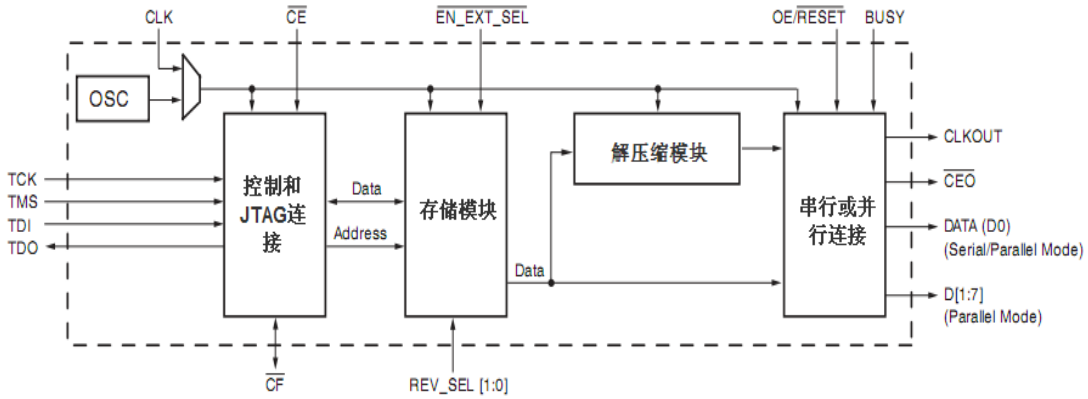


Figure 1. BST32P structure diagram

IV. Electrical properties

Please refer to the detailed specifications for product electrical characteristic parameters.

V. Functional Description

BST32P is an FPGA configuration memory with a storage capacity of 32Mbits, compatible with Xilinx's ISE software, and supports four FPGA configuration modes: master-serial, slave-serial, master-parallel, and slave-parallel.

5.1. JTAG

The BST32P Flash RPOMs platform supports the IEEE 1149.1 boundary scan standard and the IEEE 1532 online configuration standard. The test access interface (TAP) and registers are used to support boundary scan instructions and optional special IEEE 1149.1 standard instructions. In addition, the connection of the PROM TAP makes online programming (ISP), configuration, erase and verification operations more convenient. Table 3 lists the required and optional boundary scan instructions for the Flash PROM platform. The boundary scan structure and the required optional instructions can be completed according to the IEEE 1149.1 standard specification.

Table 3. BST32P boundary scan instructions

Boundary Scan Instructions	BST32P IR[15:0]	Instruction Description
Required instructions		
BYPASS	FFFF	Enabling BYPASS
SAMPLE/PRELOAD	0001	Enable boundary scan SAMPLE/PRELOAD operation
EXTEST	0000	Enable boundary scan EXTEST operation
Optional instructions		
CLAMP	00FA	Enable boundary scan CLAMP operation
HIGHZ	00FC	Set all outputs to high impedance at the same time

IDCODE	00FE	Enable shifting out 32-bit IDCODE
USERCODE	00FD	Enable shifting out 32-bit USERCODE
Flash RPOM special instructions		
CONFIG	00EE	pass$\overline{CF}$Initialize FPGA to low

When the BYPASS instruction is valid, the BYPASS register is a one-bit register connected directly from TDI to TDO. In the CAPTURE-DR state, the BYPASS register is downloaded to logic 0 on each TCK rising edge.

The boundary scan registers can be used to control and observe the state of the port during EXTEST, SAMPLE/PRELOAD, and CLAMP instructions. Each output port of the Flash PROM has two registers for boundary scan, while each input port has only one register. Bidirectional ports have three boundary scan registers. For each output port, the register closest to TDI controls and observes the output state, and the register next to TDO controls and observes the high-impedance enable state of the output port. For each input port, a separate register controls and observes the input state of the port. Bidirectional ports contain three bits, the first input bit, the second output bit, and the last output enable bit. The output enable bit is closest to TDO. The boundary scan bits and order of all connected device ports will be introduced later in the I/O. In the boundary scan register, boundary scan cell 0 is the least significant bit (LSB) of the boundary scan register and is the register closest to TDO.

5.2. TAP

The Flash PROM family can simultaneously perform in-circuit programming and IEEE1149.1 boundary scan testing (JTAG) with a single 4-wire test access interface (TAP). This simplified system allows standard automatic test equipment to perform both functions simultaneously. The AC features of the Flash PROM TAP platform are described below.

5.3. TAP Controller

The following figure shows the 16-bit state controller of BST32P. The four TAP ports control the data to be scanned and moved into various registers. At each rising edge of TCK, TMS determines the state transfer timing. There are two main timing relationships here: one is to move data into the data register, and the other is to move instructions into the instruction register.

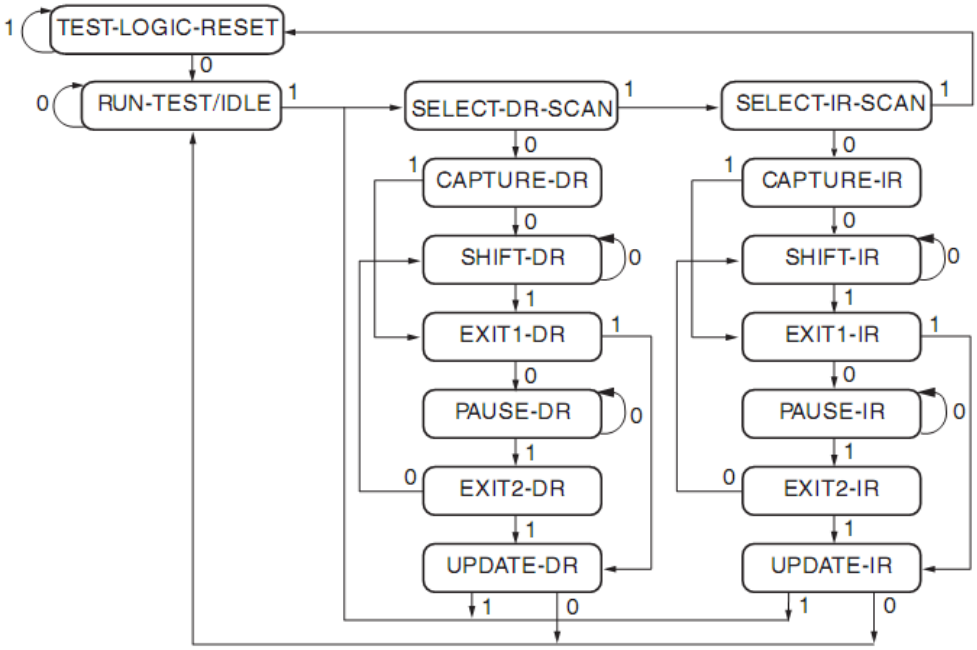


Figure 2. 16-bit state machine

5.4. IDCODE Register

IDCODE is fixed and used for manufacturer identification and address identification of special devices. The IDCODE register has a width of 32 bits. The IDCODE shift register can be shifted out and checked by using the IDCODE instruction.

Table 4. IDCODES of BST32P

Devices	IDCODE(hex)
BST32P	f5059093

5.5. Internal crystal

The BST32P has an internal selectable crystal that can be used to drive CLKOUT and the FPGA configuration connections. When programming the PROM, the internal crystal can be enabled and can be set to a default or lower operating frequency.

5.6. CLKOUT

The BST32P has a programmable option to enable the CLKOUT signal, which is a synchronous clock source that enables the data on the configuration connection to be sequenced. During PROM programming, the CLKOUT signal can come from the CLK input port or the internal oscillator. Data is valid on the rising edge of CLKOUT.

During programming, the CLKOUT signal is activated, CE_ goes low, and OE/RESET_ is high. If OE/RESET_ is high and the PROM's terminal count has not been reached when CE_ rises, CLKOUT remains active for eight clocks before it is invalid. When CLKOUT is invalid, the CLKOUT port is set to a high-impedance state or may be pulled up externally to a fixed state of "1".

When the CLKOUT of the cascaded Flash PROM platform is valid, after the first PROM data transmission is completed, the CLKOUT of the first-level PROM outputs high impedance, and drives CEO_ to enable the next-level PROM in the cascade. After the CE_ signal of the next-level PROM is valid, its CLKOUT signal is output normally.

5.7. Unzip

The 32Mbit BST32P Flash PROM platform has a built-in hardware data decompression module compatible with the latest Xilinx compression technology. Flash PROM compressed files are FPGA bitstreams compressed by iMPACT software. Only slave-serial and slave-parallel configuration modes support compressed bitstream configuration of FPGA.

During PROM programming, set whether the decompression item is valid. When the decompression item is valid, the PROM decompresses the data before driving the clock and

data to the configuration connection of the FPGA; the clock output port (CLKOUT) of the PROM must drive the configuration clock (CCLK) of the target FPGA device. The CLK input or internal oscillator of the PROM can be used as the CLKOUT clock source. In the

configuration chain, any FPGA connected to the PROM must be in slave serial or slave parallel configuration mode. Decompression does not support multi-chip cascading.

When the decompression item is valid, the CLKOUT signal clock is used as the configuration clock (CCLK) to drive the FPAG, and its output frequency is lower than the frequency when it is not decompressed. When the decompressed data is not ready, the CLKOUT signal will be in high impedance state or pulled up to the "1" state. When decompression is valid, the BUSY input will automatically be invalid.

5.8. Design version

Design version technology allows users to store up to four design versions in a single PROM or multiple PROM cascade designs. BST32P supports design version technology in both serial/parallel and decompression modes. When using iMPACT software, a programmable PROM file (.cfi) with version information is created. In iMPACT software programming, a .cfi file is required to make the design version valid.

A separate design version requires 1~n 8Mbit memory blocks. If a separate design version contains less than 8Mbit of data, the remaining space will be set to 1. A large design version uses multiple 8Mbit memory blocks, and the remaining space of the last 8Mbit memory block will be set to 1. Because at least 8Mbit of space is required for each version, a 32Mbit PROM has a maximum of four independent design versions:

- One version: 32Mb of data;
- Two versions: one with 8Mb and one with 24Mb of data, and two with 16Mb of data;
- Three versions: two 8Mb and one 16Mb of data;

- Four versions: four 8Mb data;

Larger design revisions can be achieved by using multiple cascaded PROMs. Figures 3 and 4 show basic examples of multiple memory revisions. The design revision is set when generating the mcs file using iMPACT.

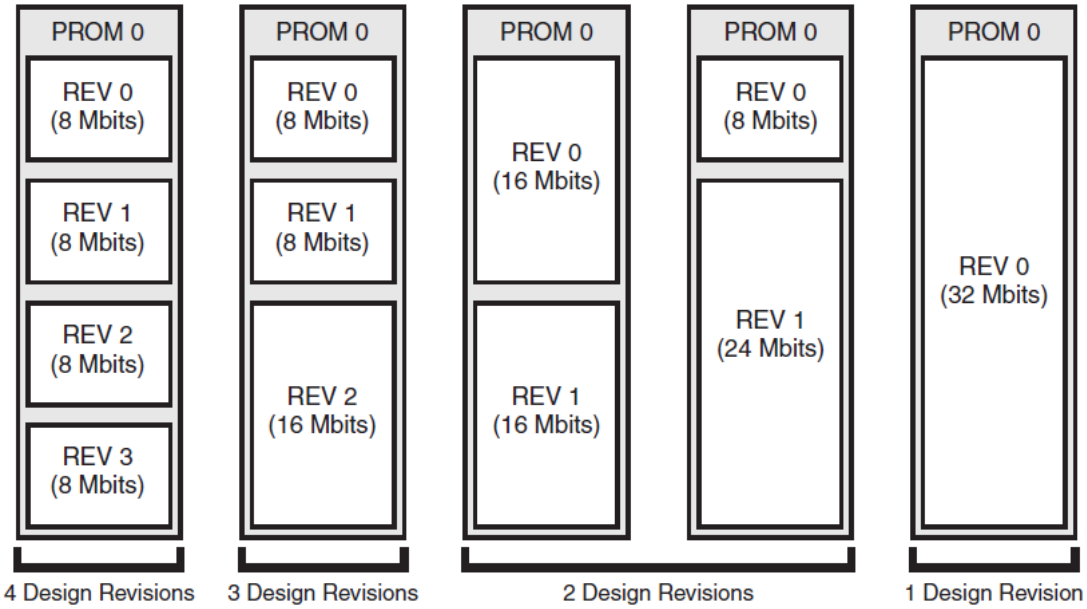


Figure 3: Example of single-chip BST32P version storage

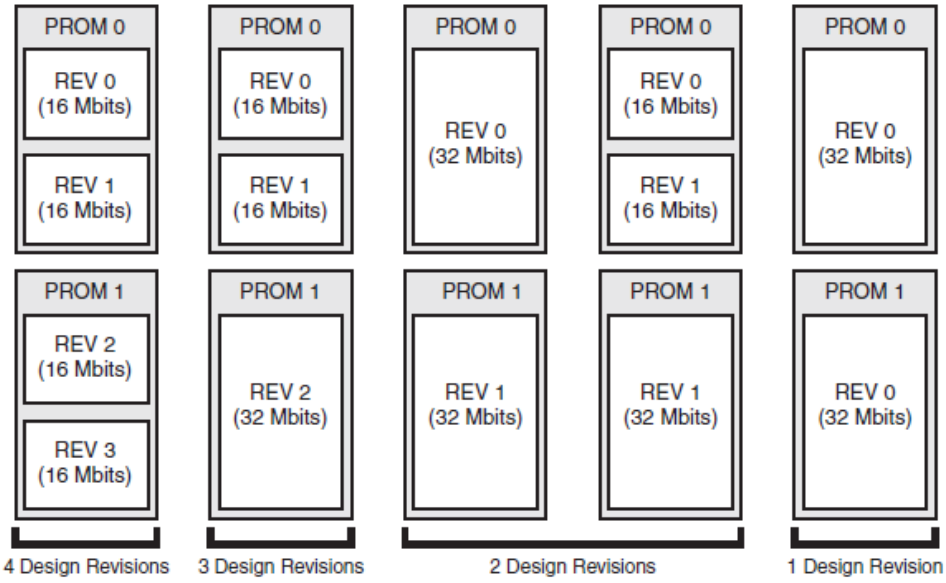


Figure 4. Two BST32P version storage example

During PROM file generation, each design revision is set to the following values:

- Revision 0 = '00'
- Revision 1 = '01'
- Revision 2 = '10'
- Revision 3 = '11'

After the Flash PROM platform containing the design version is programmed, an independent design version can be selected through the external REV_SEL[1:0] or the internal programmable design version control bit. The EN_EXT_SEL_ port determines whether the external port or the internal programmable control bit selects the design version. When EN_EXT_SEL_ is low, the design version is determined by the external port REV_SEL[1:0] selection, and when EN_EXT_SEL is high, the design version is determined by the internal programmable control bit selection. During power-on, the design version selection input (port or control bit) is sampled internally. After power-on, the design version selection input will be sampled again when the following conditions occur:

- CE_ generates rising edge
- OE/RESET_ generates a falling edge (when CE_ is low)
- When reconfiguring using the JTAG CONFIG instruction

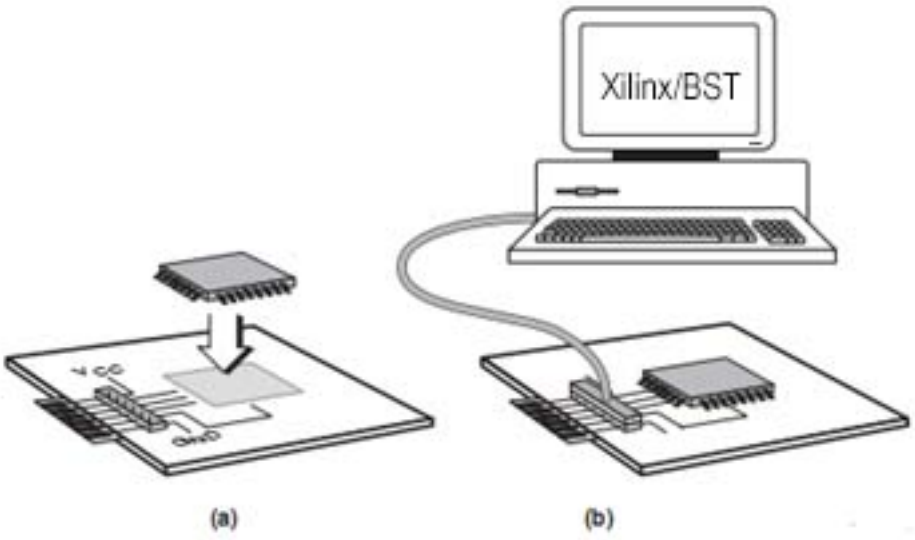
The configuration data of the selected design version will appear at the FPGA configuration connection.

VI. BST32P Applications

6.1. JTAG Programming Application

In-circuit programmable PROM can be programmed individually or in two or more cascaded rings through the standard JTAG protocol port (as shown below). In-circuit programming provides a fast and efficient design cycle, eliminating unnecessary packaging

operations and device sockets. Design data can be sequentially transferred to the device through Xilinx iMPACT software and Xilinx download cable, a third-party JTAG development system, a JTAG-compatible test board, or a microprocessor that emulates the JTAG instruction sequence. iMPACT software can also output any svf file format that supports serial vector (svf) tools, including automatic test equipment. During in-circuit programming, the CEO_ output is high, and all other outputs are fixed in a high impedance state or clamped at a certain level. In-circuit programming will fully support the recommended voltage and temperature changes.



(a) Soldering the device to the PCB (b) Using a programmable download cable

Figure 5. JTAG online programming operation

BST32P online programmable products guarantee more than 20,000 program/erase cycles and no less than 20 years of data retention (at room temperature). Within this effective limit, all functions, working conditions and data parameters of each device can be referred to in this parameter manual.

The BST32P In-Circuit Programmable Flash PROM device platform incorporates the latest

data security features to prevent FPGA data from being read by unauthorized JTAG or accidentally written by JTAG. Table 5 lists the effective security settings for the BST32P PROM.

Table 5. BST32P version data security settings

Read protection	Write protection	Anti-read/verification	Anti-programming	Anti-erasure
Reset (Default)	Reset (Default)	-	-	-
Reset (Default)	Setting effective	-	√	√
Setting effective	Reset (Default)	√	-	-
Setting effective	Setting effective	√	√	√

Note: √ means valid, - means invalid

The user can design a read protection security bit to prevent the internal programming template from being read or copied by JTAG. Read protection does not hinder write operations. The read protection security bit of BST32P PROM can be set for the design version separately. To reset the read protection bit, you need to erase part of the design version.

The BST32P PROM device also allows write protection for a special design version or as an optional setting of the PROM. Write protection can prevent an inadvertent JTAG instruction from modifying/erasing the protected area. The read and write protection bits must be cleared by an erase operation.

VII. Configuring Output Applications

7.1. Main String Mode

In master serial mode, the FPGA will automatically and synchronously download the bit stream from the outside in a bit-by-bit serial manner for configuration according to the

internally generated clock CCLK. When powering on or reconfiguring, the FPGA's mode selection port should select the master serial configuration mode. When configuring the FPGA, only serial data lines, clock lines, and two control lines (INIT and DONE) are required. As the PROM's internal address counter increases with each valid rising edge of CCLK, the configuration data is read out in order from a single data line (DIN). A short period of time before each rising edge of the FPGA's internal clock signal CCLK, the serial bit stream data must be established at the FPGA's DIN input port.

By default, the FPGA generates a low-frequency CCLK output clock. If you need to change the CCLK frequency, set it when the bit data stream is generated.

In master serial mode, the connection between FPGA and PROM is:

- The DATA output of the PROM is connected to the DIN terminal of the FPGA
- The PROM's CLK is connected to the main FPGA's CCLK terminal
- When PROMs are cascaded, CEO_ is connected to the CE_ terminal of the next PROM.
- The OE/RESET_ pin of the PROM must be connected to the INIT_B pin of the FPGA to ensure that the address count of the PROM is correct during reconfiguration
- The CE_ of the PROM is connected to the DONE of the FPGA. When cascading, only the CE_ of the first PROM is connected to the DONE of the target FPGA device. When the configuration is completed, the CE_ is driven high by the DONE of the FPGA, and the PROM enters the sleep mode to reduce the system power consumption.
- The CF_ terminal of PROM is connected to PROG_B of FPGA. When the CF_ terminal of BST32P is not connected to PROG_B of FPGA, it must be pulled up to high.

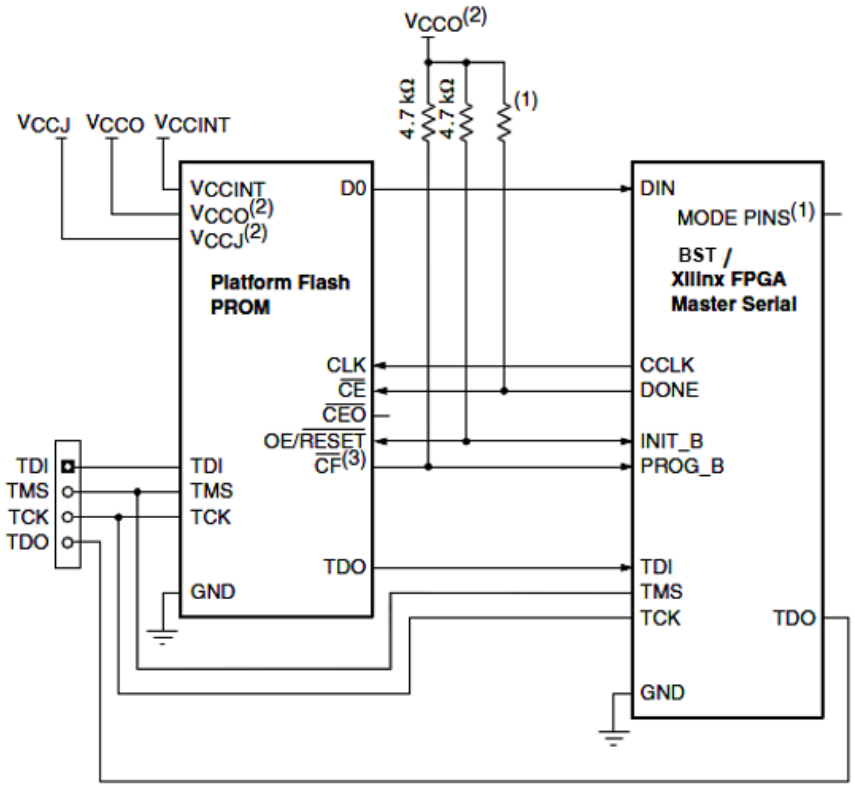


Figure 6. BST32P master string configuration mode application

Note:

- Data decompression is not supported.
- For the mode selection pin connection and the DONE pin pull-up resistor value, please refer to the relevant FPGA data sheet.
- For power supply voltage compatibility, please refer to the corresponding data sheet.
- The CF_ of BST32P is a bidirectional port. In BST32P, if CF_ is not connected to PROG_B, then CF_ must be connected to VCCO through a 4.7KΩ pull-up resistor.

7.2 Master-Merge Mode

In master-parallel mode, the FPGA will automatically and synchronously download the bit stream from the external bit-by-bit parallel (8-bit) for configuration according to the

internally generated clock CCLK, and use the BUSY signal to control the data flow. At power-on or reconfiguration, the FPGA's mode select port will select the master-parallel configuration mode. When configuring the FPGA, parallel data lines, clock lines, and two control lines (INIT and DONE) are required. In addition, the FPGA's chip select, WRITE, and BUSY ports must be connected correctly. As the PROM's internal address counter increases with each valid rising edge of CCLK, the configuration data is read out from D0-D7 in order. A short period of time before each rising edge of the FPGA's internal clock signal CCLK, the parallel bit stream data must be established at the FPGA's D0-D7 input ports. If BUSY is set high, the configuration data must be held until BUSY is set low. The FPGA's chip select (CS_ or CS_B) and write (WRITE_ or RDWR_B) signals must be enabled low.

By default, the FPGA generates a low-frequency CCLK output clock. If you need to change the CCLK frequency, set it when the bit data stream is generated.

In master-parallel mode, the connection between FPGA and PROM is:

- The DATA output of the PROM is connected to the DIN terminal of the FPGA
- The PROM's CLK is connected to the main FPGA's CCLK terminal
- When PROMs are cascaded, CEO_ is connected to the CE_ terminal of the next PROM.
- The OE/RESET_ pin of the PROM must be connected to the INIT_B pin of the FPGA to ensure that the address count of the PROM is correct during reconfiguration
- The CE_ of the PROM is connected to the DONE of the FPGA. When cascading, only the CE_ of the first PROM is connected to the DONE of the target FPGA device. When the configuration is completed, the CE_ is driven high by the DONE of the FPGA, and the PROM enters the STANBY mode to reduce system power consumption.
- For high-frequency parallel configuration, the BUSY of the PROM is connected to the BUSY of the FPGA, ensuring that the next byte of data output by the PROM

is delayed until the FPGA is ready to receive the next byte of configuration data.

- The CF_ terminal of PROM is connected to PROG_B of FPGA. When the CF_ terminal of BST32P is not connected to PROG_B of FPGA, it must be pulled up to high.

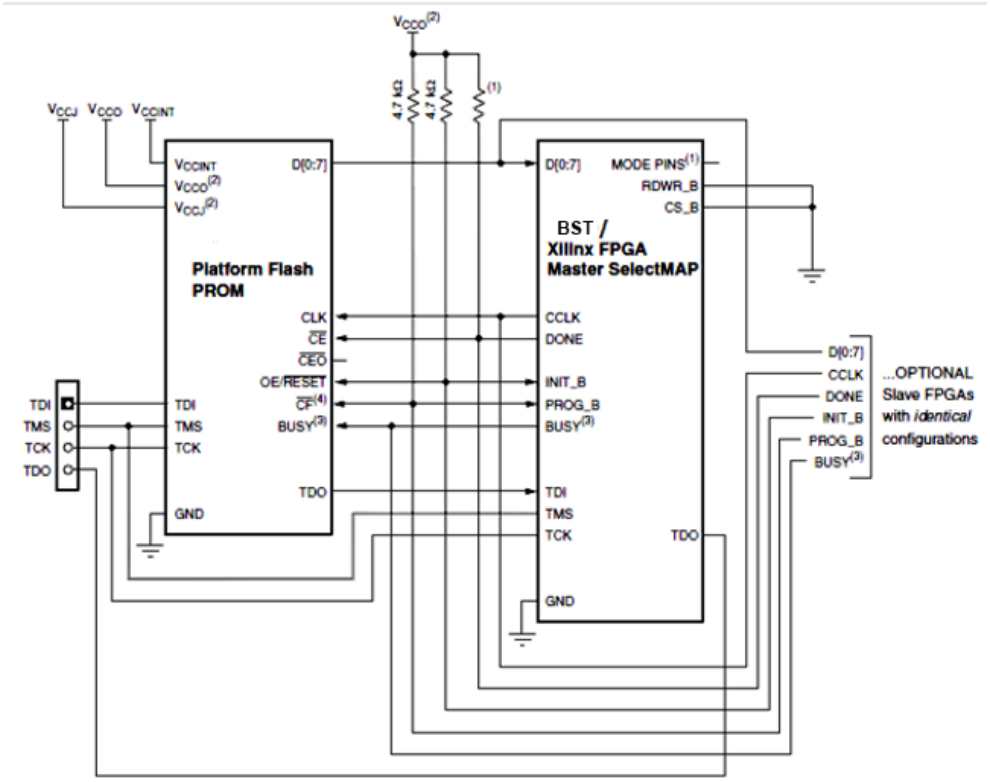


Figure 7. BST32P master and parallel configuration mode application

Note:.

- Data decompression is not supported.
- For the mode selection pin connection and the DONE pin pull-up resistor value, please refer to the relevant FPGA data sheet.
- For power supply voltage compatibility, please refer to the corresponding data sheet.
- CS_B (or CS_) and RDWR_B (or WRITE_) must be driven low or pulled down externally.
- The BUSY signal is connected only in parallel mode. For specific requirements,

please refer to the corresponding FPGA data manual.

- The CF_ of BST32P is a bidirectional port. In BST32P, if CF_ is not connected to PROG_B, then CF_ must be connected to VCCO through a 4.7KΩ pull-up resistor.

7.3. Slave Serial Mode

In slave serial mode, the FPGA will automatically and synchronously download the configuration bit stream from the external bit serially according to the external clock. When powered on or reconfigured, the FPGA's mode selection port will select the slave serial configuration mode. When configuring the FPGA, only a serial data line, a clock line, and two control lines (INIT and DONE) are required. With each valid rising edge of CCLK, the PROM's internal address counter increases, and the configuration data is read out in order from a single data line (DIN). A short period of time before each rising edge of the external clock signal CCLK, the serial bit stream data must be established at the DIN input port of the FPGA.

In slave mode, the connection between FPGA and PROM is:

- The DATA output of the PROM is connected to the DIN terminal of the FPGA
- The PROM's CLKOUT or external clock source drives the FPGA CCLK terminal
- When PROMs are cascaded, CEO_ is connected to the CE_ terminal of the next PROM.
- The OE/RESET_ pin of the PROM must be connected to the INIT_B pin of the FPGA to ensure that the address count of the PROM is correct during reconfiguration
- The CE_ of the PROM is connected to the DONE of the FPGA. When cascading, only the CE_ of the first PROM is connected to the DONE of the target FPGA device. When the configuration is completed, the CE_ is driven high by the DONE

- of the FPGA, and the PROM enters the STANBY mode to reduce system power consumption.
- The CF_ terminal of PROM is connected to PROG_B of FPGA. When the CF_ terminal of BST32P is not connected to PROG_B of FPGA, it must be pulled up to high.

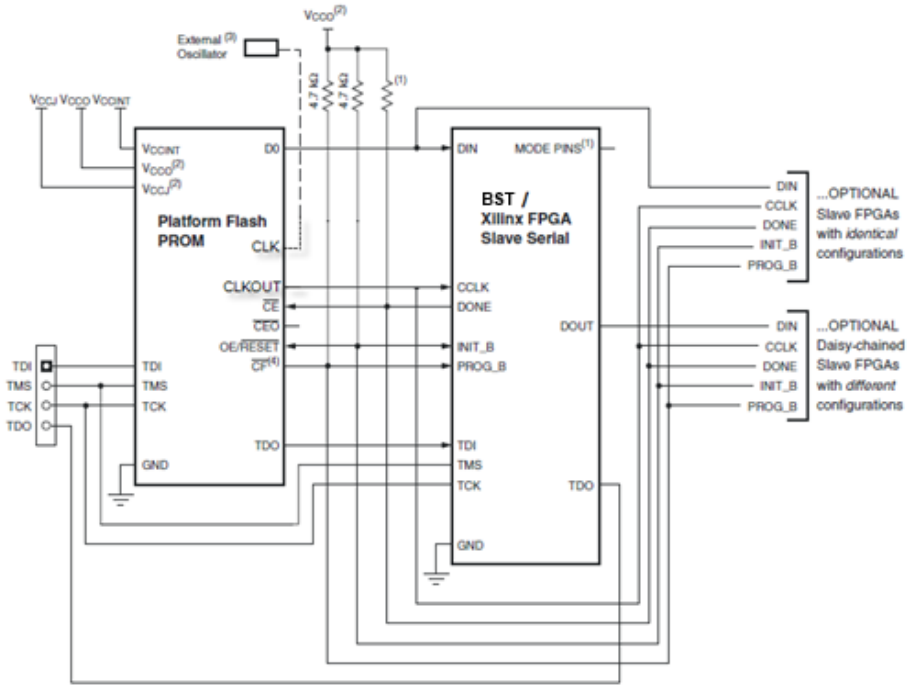


Figure 8. BST32P slave configuration mode application

Note:

- For the mode selection pin connection and the DONE pin pull-up resistor value, please refer to the relevant FPGA data sheet.
- For power supply voltage compatibility, please refer to the corresponding data sheet.
- In slave mode, the configuration clock is provided by an external clock crystal or the PROM internal oscillator. The CCLK terminal of the FPGA must be connected to the CLKOUT of the PROM, and CLKOUT is connected to VCCO through a

4.7KΩ pull-up resistor.

- The CF_ of BST32P is a bidirectional port. In BST32P, if CF_ is not connected to PROG_B, then CF_ must be connected to VCCO through a 4.7KΩ pull-up resistor.
- When data is decompressed, the CLKOUT output frequency is 1/2 of the clock source frequency.

7.4. Slave Mode

In slave-parallel mode, the FPGA will automatically and synchronously download the bit stream from the external bit-by-bit parallel (8-bit) for configuration according to the internally generated clock CCLK, and use the BUSY signal to control the data flow. At power-on or reconfiguration, the FPGA's mode select port will select the slave-parallel configuration mode. When configuring the FPGA, parallel data lines, clock lines, and two control lines (INIT and DONE) are required. In addition, the FPGA's chip select, WRITE, and BUSY ports must be connected correctly. As the PROM's internal address counter increases with each valid rising edge of CCLK, the configuration data is read out from D0-D7 in order. A short period of time before each rising edge of the FPGA's internal clock signal CCLK, the parallel bit stream data must be established at the FPGA's D0-D7 input ports. If BUSY is set high, the configuration data must be held until BUSY is set low. The FPGA's chip select (CS_ or CS_B) and write (WRITE_ or RDWR_B) signals must be enabled low.

Connection between FPGA and PROM in parallel mode:

- The DATA output of the PROM is connected to the DIN terminal of the FPGA
- The PROM's CLK is connected to the main FPGA's CCLK terminal
- When PROMs are cascaded, CEO_ is connected to the CE_ terminal of the next PROM.
- The OE/RESET_ pin of the PROM must be connected to the INIT_B pin of the FPGA to ensure that the address count of the PROM is correct during

reconfiguration

- The CE_ of the PROM is connected to the DONE of the FPGA. When cascading, only the CE_ of the first PROM is connected to the DONE of the target FPGA device. When the configuration is completed, the CE_ is driven high by the DONE of the FPGA, and the PROM enters the STANBY mode to reduce system power consumption.
- For high-frequency parallel configuration, the BUSY of the PROM is connected to the BUSY of the FPGA, ensuring that the next data output by the PROM is delayed until the FPGA is ready to receive the next byte of configuration data.
- The CF_ terminal of PROM is connected to PROG_B of FPGA. When the CF_ terminal of BST32P is not connected to PROG_B of FPGA, it must be pulled up to high.

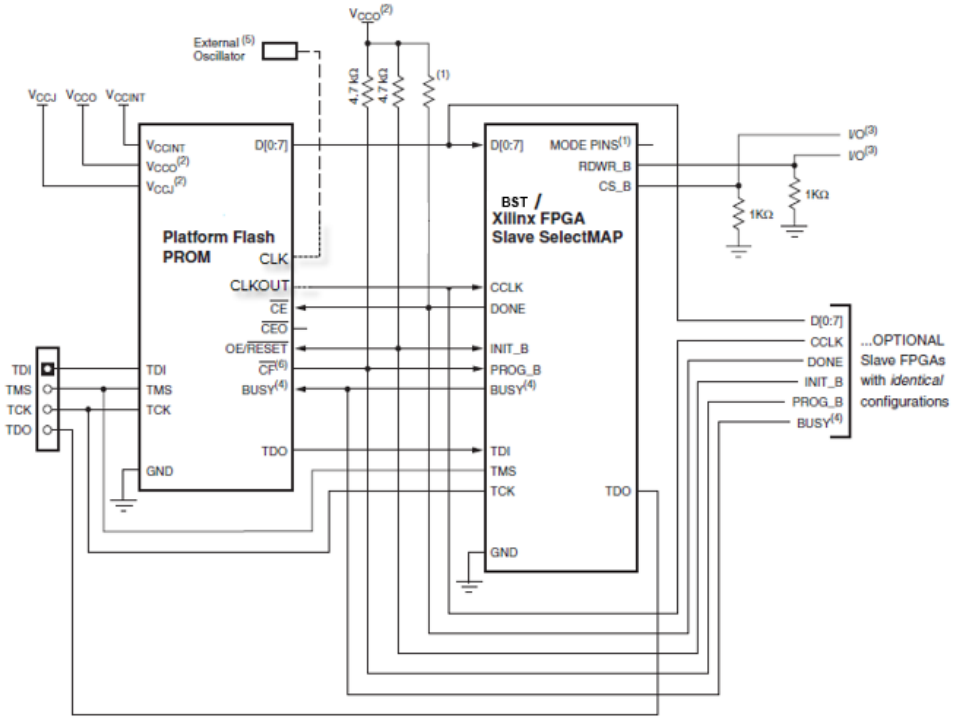


Figure 9. BST32P slave parallel configuration mode application

Note:

- For the mode selection pin connection and the DONE pin pull-up resistor value, please refer to the relevant FPGA data sheet.
- For power supply voltage compatibility, please refer to the corresponding data sheet.
- CS_B (or CS_) and RDWR_B (or WRITE_) must be driven low or pulled down externally.
- The BUSY signal is connected only in parallel mode. For specific requirements, please refer to the corresponding FPGA data manual.
- In slave mode, the configuration clock is provided by an external clock crystal or the PROM internal oscillator. The CCLK terminal of the FPGA must be connected to the CLKOUT of the PROM, and CLKOUT is connected to VCCO through a 4.7KΩ pull-up resistor.
- The CF_ of BST32P is a bidirectional port. In BST32P, if CF_ is not connected to PROG_B, then CF_ must be connected to VCCO through a 4.7KΩ pull-up resistor.
- When data is decompressed, the CLKOUT output frequency is 1/2 of the clock source frequency.

7.5. Cascade Mode

Cascading PROMs provides additional storage when configuring multiple FPGAs in a serial chain, configuring multiple FPGAs in a parallel chain, or configuring an FPGA that requires a larger bitstream. Multiple Flash PROM connections can be made by driving the CE_ input of the next device PROM through the CEO_ output of the previous PROM device. In the chain, the clock signals and data outputs of all Flash PROMs are interconnected. When the last data of the first PROM is read out, the CEO_ output of the first PROM is low and the other output ports are in a high impedance state. The second PROM recognizes that the CE_ input is low and immediately makes its output valid.

After configuration is complete, if the PROM's OE/RESET_ is low or CE_ is high, all cascaded PROM address counters are reset.

When the PROM is the master, the CLKOUT of the PROM must be connected to the CCLK port of the FPGA; BUSY needs to change on the falling edge of the clock.

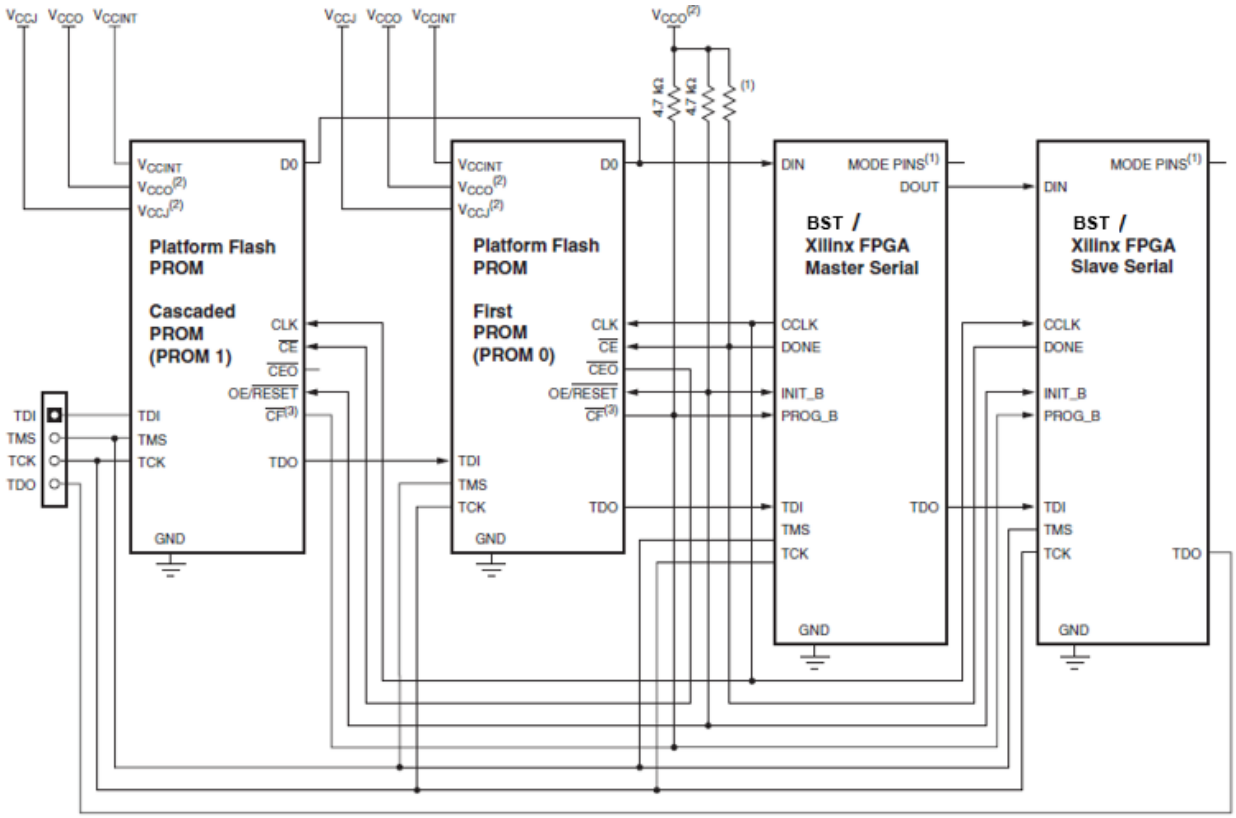


Figure 10. BST32P master/slave serial configuration mode cascade application

Note:

- For the mode selection pin connection and the DONE pin pull-up resistor value, please refer to the relevant FPGA data sheet.
- For power supply voltage compatibility, please refer to the corresponding data sheet.
- The CF_ of BST32P is a bidirectional port. In BST32P, if CF_ is not connected to PROG_B, then CF_ must be connected to VCCO through a 4.7KΩ pull-up resistor.

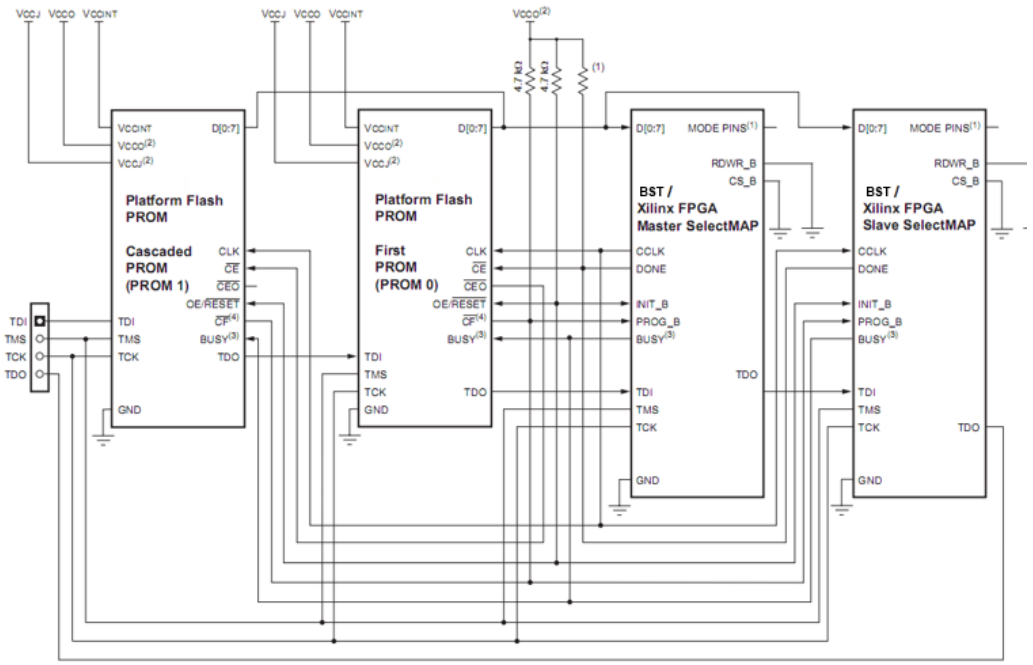


Figure 11. BST32P master/slave configuration mode cascade application

Note:

- For the connections of the mode port and the pull-up value of the DONE port, refer to the appropriate FPGA data sheet or the user configuration help documentation for the FPGA family.
- For compatible voltage values, please refer to the relevant data sheet.
- CS_B (or CS_) and RDWR_B (or WRITE_) must be driven low or pulled down externally.
- The BUSY port is only in the BST32P Flash PROM. (The BUSY port connection is required only when the FPGA series is configured in high-frequency parallel mode). If there is no BUSY port in the FPGA or the BUSY port is not required when configuring the device, the PROM BUSY port is not connected or grounded. For detailed information about the BUSY port, refer to the relevant FPGA data manual or FPGA configuration help document.

- The CF_ bidirectional port of BST32P. In BST32P, if CF_ is not connected to PROG_B, then CF_ must be connected to VCCO through a 4.7KΩ pull-up resistor.

7.6. Multiple design version application

When multiple FPGAs need to be configured, or different bit files need to be configured for one FPGA at different times, the BST32P version selection function can be used. The BST32P can store up to 4 different 8Mbit design files internally. When used, the BST32P can set the internal default output version by the programming software. If the output of the version data needs to be changed externally, the design provides the EN_EXT_SEL_version enable signal terminal and the REV_SEL[1:0] version selection signal terminal. These three version selection terminals are controlled by an external microcontroller or FPGA in conjunction with DONE and PROG_B to achieve version data changes and reconfiguration.

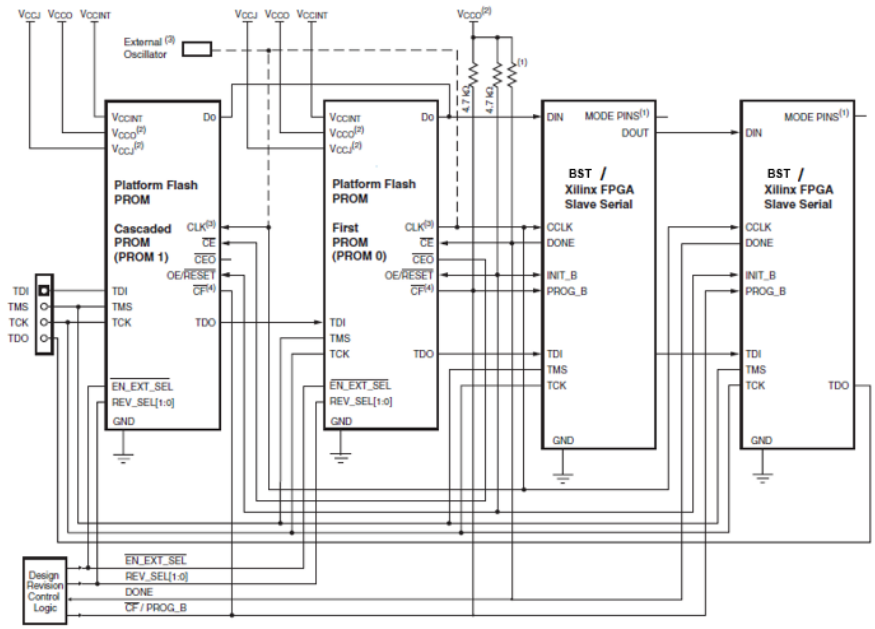


Figure 12. BST32P multi-version configuration in slave mode

Note:

- For the connections of the mode port and the pull-up value of the DONE port, refer to the appropriate FPGA data sheet or the user configuration help documentation for the FPGA family.
- For compatible voltage values, please refer to the relevant data sheet.
- In slave mode, the configuration clock is provided by an external clock crystal or the PROM internal oscillator. The CCLK terminal of the FPGA must be connected to the CLKOUT of the PROM, and CLKOUT is connected to VCCO through a 4.7KΩ pull-up resistor.
- The CF_ of BST32P is a bidirectional port. In BST32P, if CF_ is not connected to PROG_B, then CF_ must be connected to VCCO through a 4.7KΩ pull-up resistor.

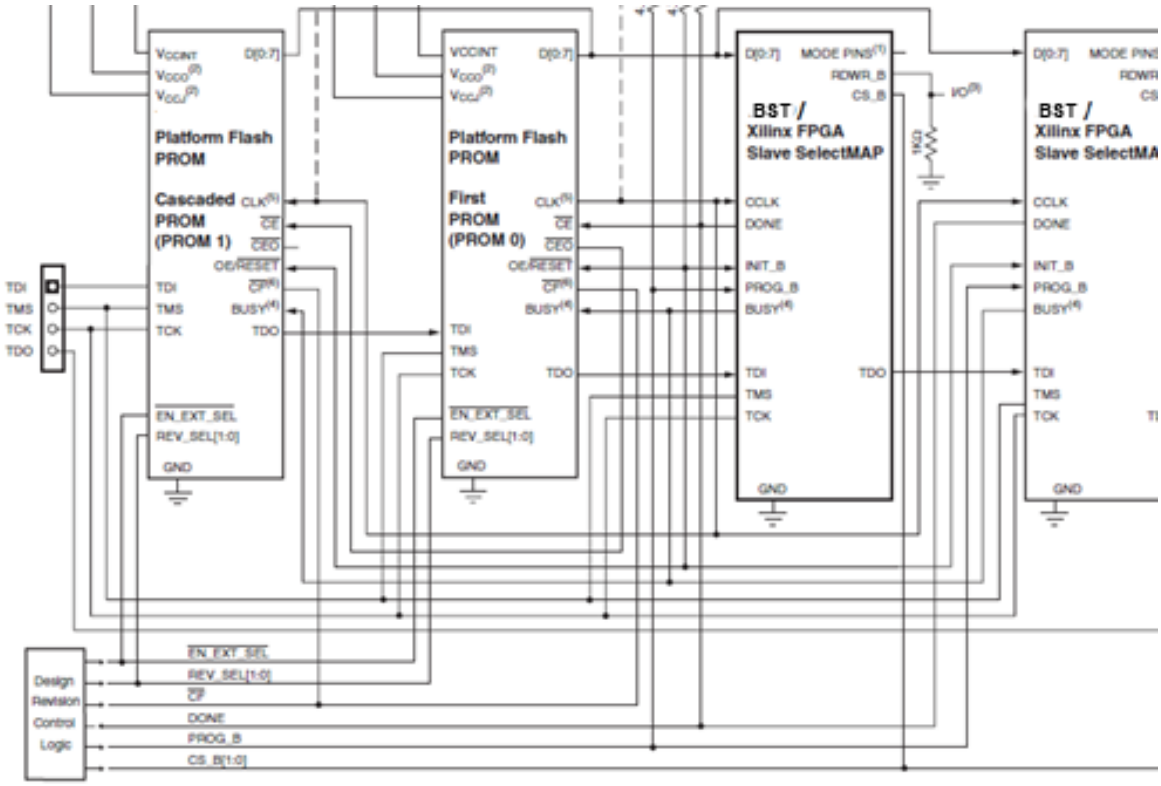


Figure 13. BST32P multi-version configuration in slave mode

Note:

- For the connections of the mode port and the pull-up value of the DONE port, refer to the appropriate FPGA data sheet or the user configuration help documentation for the FPGA family.
- For compatible voltage values, please refer to the relevant data sheet.
- CS_B (or CS_) and RDWR_B (or WRITE_) must be driven low or pulled down externally.
- The BUSY port is only in the BST32P Flash PROM. (The BUSY port connection is required only when the FPGA series is configured in high-frequency parallel mode). If there is no BUSY port in the FPGA or the BUSY port is not required when configuring the device, the PROM BUSY port is not connected or grounded. For detailed information about the BUSY port, refer to the relevant FPGA data manual or FPGA configuration help document.
- In slave-parallel mode, the configuration clock is provided by an external clock crystal or the PROM internal oscillator. The CCLK terminal of the FPGA must be connected to the CLKOUT of the PROM, and CLKOUT is connected to VCCO through a 4.7KΩ pull-up resistor.
- The CF_ of BST32P is a bidirectional port. In BST32P, if CF_ is not connected to PROG_B, then CF_ must be connected to VCCO through a 4.7KΩ pull-up resistor.

VIII. Application Schematic

The application schematic diagram of BST32P_CSOP48 configuring BST4VLX25_BGA668 is as follows. All configuration modes are taken into account, and users can simplify the design according to their own application.

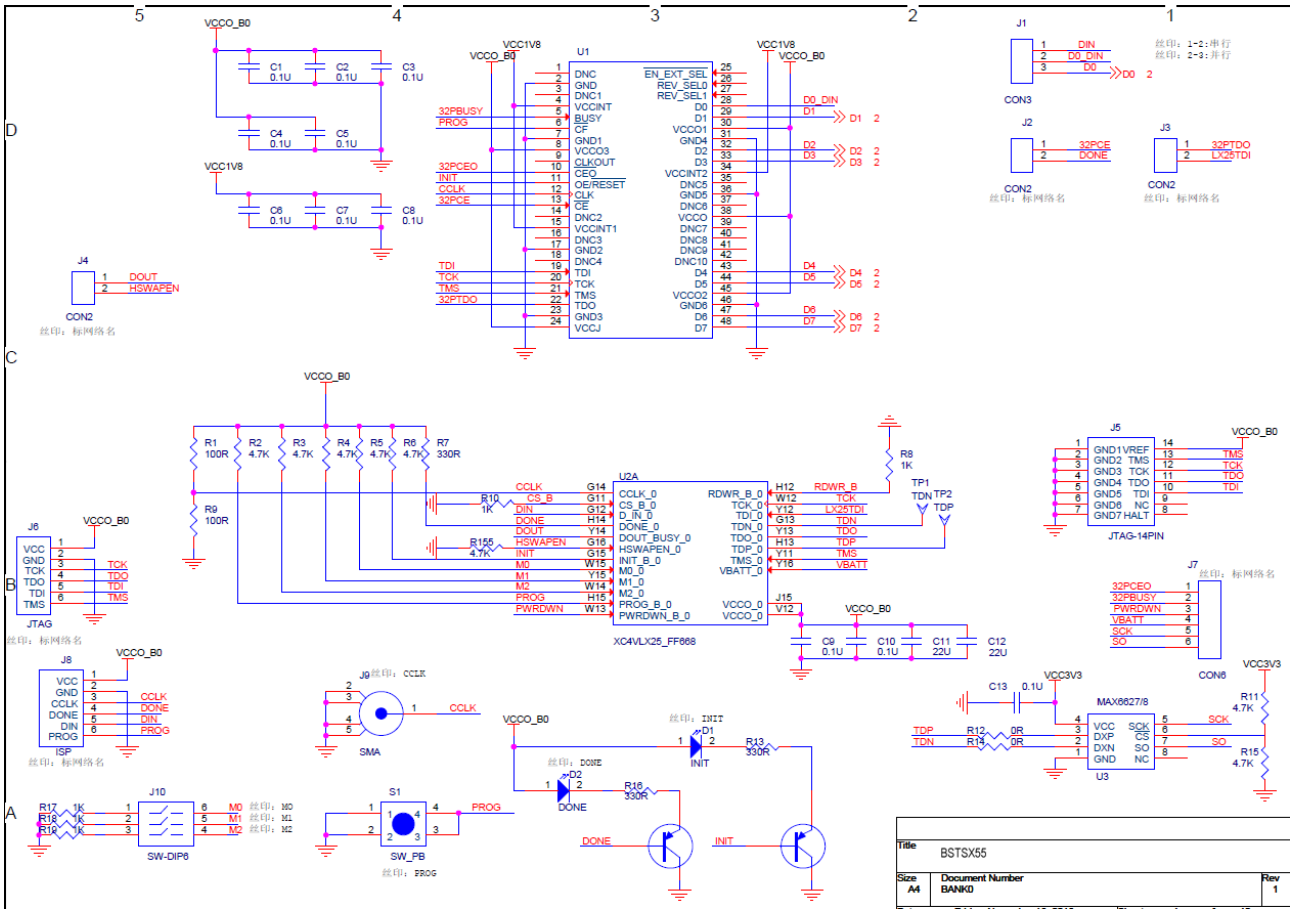


Figure 14. Application schematic diagram

IX. Switching Characteristics

9.1. Power-On Reset

When powered on, the device requires the voltage VCCINT to provide a monotonic and stable rising control voltage within the rising time. If the power supply cannot meet the requirements, the device may not be able to perform the power-on reset function. During the timing power-on period, OE/RESET_ is fixed at a low level by the PROM. Once the power supplies reach their respective POR (open reset) turn-on limit, the delay (minimum T_{OER}) releases OE/RESET_ to allow more margin for the power supply to stabilize before configuration. The OE/RESET_ port is connected to an external 4.7KΩ pull-up resistor and the FPGA's INIT port. When the power supply rises slowly, an additional voltage monitoring

circuit delays configuration by fixing OE/RESET_ low until the system power supply reaches the minimum operating voltage value. When OE/RESET_ is released, the FPGA's initialization port is pulled high and allows FPGA timing configuration. If the power supply drops to the shutdown limit (V_{CCPD}), the PROM is reset and OE/RESET_ is pulled low again until the POR voltage limit. The start-up conditions are shown in the figure.

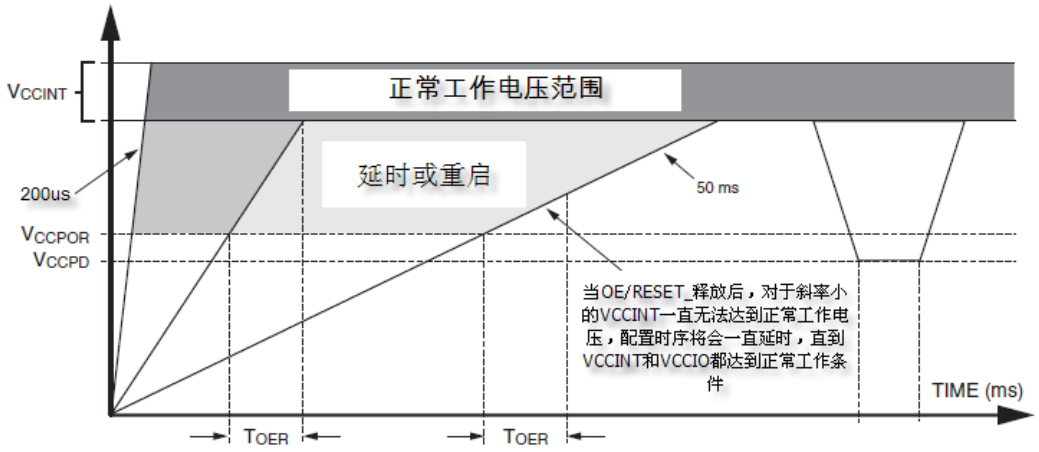


Figure 15. PROM power-on and power-off process

The voltage conditions for powering on and off are shown in the following table:

Table 6. Power-on and power-off requirements

Signal	Describe	BST32P		Unit
		Min	Max	
TVCC	The rise time of VCCINT from 0 to normal voltage	0.2	50	ms
VCCPOR	VCCINT POR start-up limit voltage	0.5	-	V
TOER	OE/RESET_ delay time after POR	0.5	30	ms
VCCPD	VCCINT shutdown limit voltage	-	0.5	V

Note:

- Power supply sequence: VCCINT must be powered on before VCCO.

- When powered on, the device requires the VCCINT power supply to automatically rise to the normal operating voltage range within the TVCC time.
- If VCCINT and VCCO have not reached their normal operating voltage range before OE/RESET_ is released, the configuration data from the PROM is not available. The configuration sequence must be delayed until both VCCINT and VCCO have reached their normal operating range.

9.2. Sleep Mode

When CE_ is high, the PROM will enter low-power sleep mode. In sleep mode, the address counter is reset, CEO_ is driven high, other outputs are set to high impedance, and the input state of OE/RESET_ is ignored. When the device remains in low-power standby mode, the JTAG port: TMS\TDI and TDO must be set low, and TCK must stop working (high or low).

After configuration is completed, the FPGA releases the DONE signal. Since the DONE (CE_) signal line is connected to an external pull-up resistor, the PROM CE_ is driven high to reduce power consumption. The pull-up resistor value of the DONE port (typically 330Ω pull-up resistor value) can be found in the relevant FPGA data document. If the DONE circuit is connected to an LED to show that the configuration is complete, the PROM CE_ must also be connected to enable the power sleep mode. However, an external buffer is required to drive the LED circuit to ensure that the signal is correctly transmitted to the PROM's CE_ port. If the PROM does not require a low-power sleep mode, CE_ should be grounded.

The following table is the input control truth table of PROM:

Table 7. BST32P input control truth table

Input control signal				Internal Address	Output			
OE/RESET_	CE_	CF_	BUSY(5)		DATA	CEO_	CLKOUT	ICC

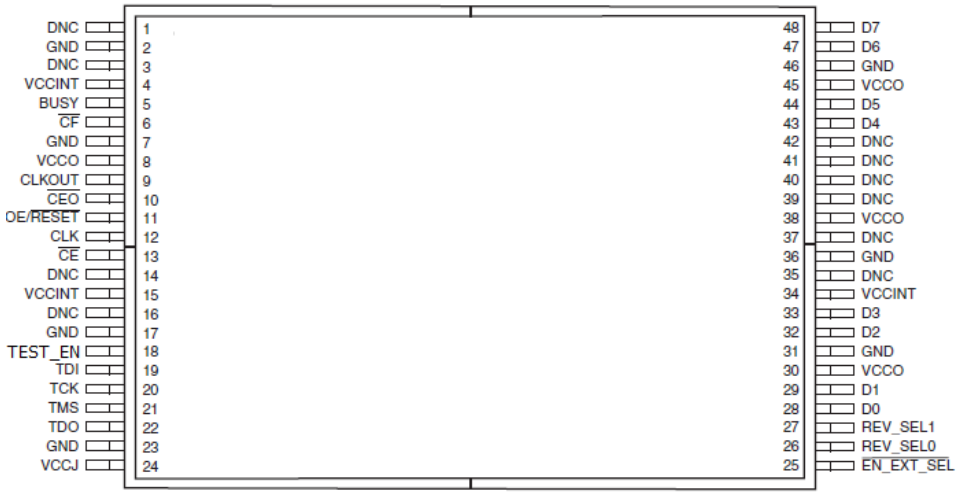
high	Low	high	Low	If address < TC(2) and < EA(3): increase	activa-tion	high	activation	acti-va-tion
				If address < TC and = EA: un-changed	High re-sistance	high	High re-sistance	re-duce
				If address = TC: unchanged	High re-sistance	Low	High re-sistance	re-duce
high	Low	high	high	constant	Activa-tion and invari-ance	high	activation	acti-va-tion
high	Low	↑	X(1)	Reset(4)	activa-tion	high	activation	acti-va-tion
Low	Low	X	X	Keep Reset	High re-sistance	high	High re-sistance	acti-va-tion
X	high	X	X	Keep Reset	High re-sistance	high	High re-sistance	Hi-ber-na-tion

Note:

- X=any value.
- TC: Final count, end address value.
- BST32P design version is valid, EA: the end address of the selected version.
- If the BST32P design version is valid, the reset address is reset to the initial address of the selected module. If the design version is invalid, the reset address is reset to 0.
- The BUSY input is only used when the BST32P is outputting data in parallel and decompression is disabled.

X. Terminal arrangement

The CSOP48 lead arrangement should be as shown in Figure 16 (top view).



Picture 16. CSOP48 pin arrangement

The FBGA48 lead arrangement should be as shown in Figure 17 (top view).

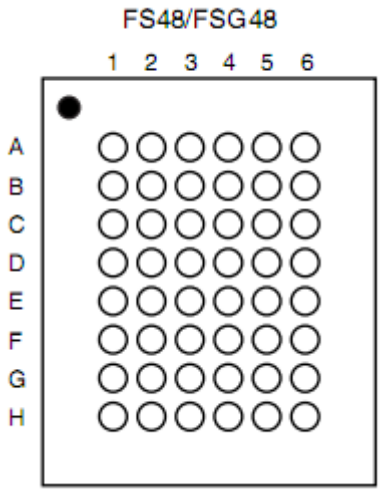


Figure 17. FBGA48 pin arrangement

Table 8. CSOP48 pin description

Pin Number	Pin Direction	Symbol	Function	Pin Number	Pin Direction	Symbol	Function
P1	-	DNC	Dangling	P25	I	EN_EXT_SEL_	Enable external selection input
P2	I	GND	land	P26	I	REV_SEL0	Version selection input
P3	-	DNC	Dangling	P27	I	REV_SEL1	Version selection input
P4	I	VCCINT	Core Power Supply	P28	O	D0	Serial/parallel data output D0 bit
P5	I	BUSY	BUSY signal input	P29	O	D1	Parallel data output D1 bit
P6	IO	CF_	Configuration Pulse	P30	I	VCCO	I/O Power
P7	I	GND	land	P31	I	GND	land
P8	I	VCCO	I/O Power	P32	O	D2	Parallel data output D2 bit
P9	O	CLKOUT	Configuring Clock Output	P33	O	D3	Parallel data output D3 bit
P10	O	CEO_	Chip Enable Output	P34	I	VCCINT	Core Power Supply
P11	IO	OE/RESET_	Output Enable/Reset	P35	-	DNC	Dangling
P12	I	CLK	Configuration Clock Input	P36	I	GND	land
P13	I	CE_	Chip Enable Input	P37	-	DNC	Dangling
P14	-	DNC	Dangling	P38	I	VCCO	I/O Power
P15	I	VCCINT	Core Power Supply	P39	-	DNC	Dangling
P16	-	DNC	Dangling	P40	-	DNC	Dangling
P17	I	GND	land	P41	-	DNC	Dangling
P18	I	TEST_EN	Test pin	P42	-	DNC	Dangling
P19	I	TDI	JTAG data input	P43	O	D4	Parallel data output D4 bit
P20	I	TCK	JTAG clock input	P44	O	D5	Parallel data output D5 bit
P21	I	TMS	JTAG Mode Selection	P45	I	VCCO	I/O Power

P22	O	TDO	JTAG data output	P46	I	GND	land
P23	I	GND	land	P47	O	D6	Parallel data output D6 bit
P24	I	VxJ	JTAG I/O Power Supply	P48	O	D7	Parallel data output D7 bit

Note:

P18 (TEST_EN)Used for production testing, not open to users, and requires to be grounded or left floating.

Table 9. CSOP48 pin description

Pin number	symbol	Function	Pin number	symbol	Function
A1	GND	land	E1	VCCINT	Internal logic power supply
A2	GND	land	E2	TMS	JTAG Test Mode
A3	OE/RERST_	Output enable signal/reset signal	E3	DNC	Floating pin
A4	DNC	Floating pin	E4	DNC	Floating pin
A5	D6	Parallel data output D6 bit	E5	D2	Parallel data output D2 bit
A6	D7	Parallel data output D7 bit	E6	TDO	JTAG test data output
B1	VCCINT	Internal logic power supply	F1	GND	land
B2	VCCO	IO Power	F2	DNC	Floating pin
B3	CLK	Clock signal	F3	DNC	Floating pin
B4	CE_	Chip enable signal	F4	DNC	Floating pin
B5	D5	Parallel data output D5 bit	F5	GND	land
B6	GND	land	F6	GND	land

C1	BUSY	BUSY input signal	G1	TDI	JTAG test data input
C2	CLKOUT	Configuring Clock Out-put	G2	DNC	Floating pin
C3	DNC	Floating pin	G3	REV_SEL0	Version selection input
C4	DNC	TEST_EN	G4	REV_SEL1	Version selection input
C5	D4	Parallel data output D4 bit	G5	VCCO	IO Power
C6	VCCO	IO Power	G6	VCCINT	Internal logic power supply
D1	CF_	Configuring Signals	H1	GND	land
D2	CEO_	Chip enable output sig-nal	H2	VxJ	JTAG Power Supply
D3	DNC	Floating pin	H3	TCK	JTAG Test Clock
D4	DNC	Floating pin	H4	EN_EST_SEL_	Enable external selec-tion input
D5	D3	Parallel data output D3 bit	H5	D1	Parallel data output D1 bit
D6	VCCO	IO Power	H6	D0	Serial data output (parallel data output D0 bit)

Note:

C4(TEST_EN)Used for production testing, not open to users, and requires to be grounded or left floating.

XI. Package Specifications

- The device adopts 48-lead ceramic sealed CSOP package, and its dimensions refer to the provisions of GB/T 7092-1993. The shell shape is shown in Figure 18.

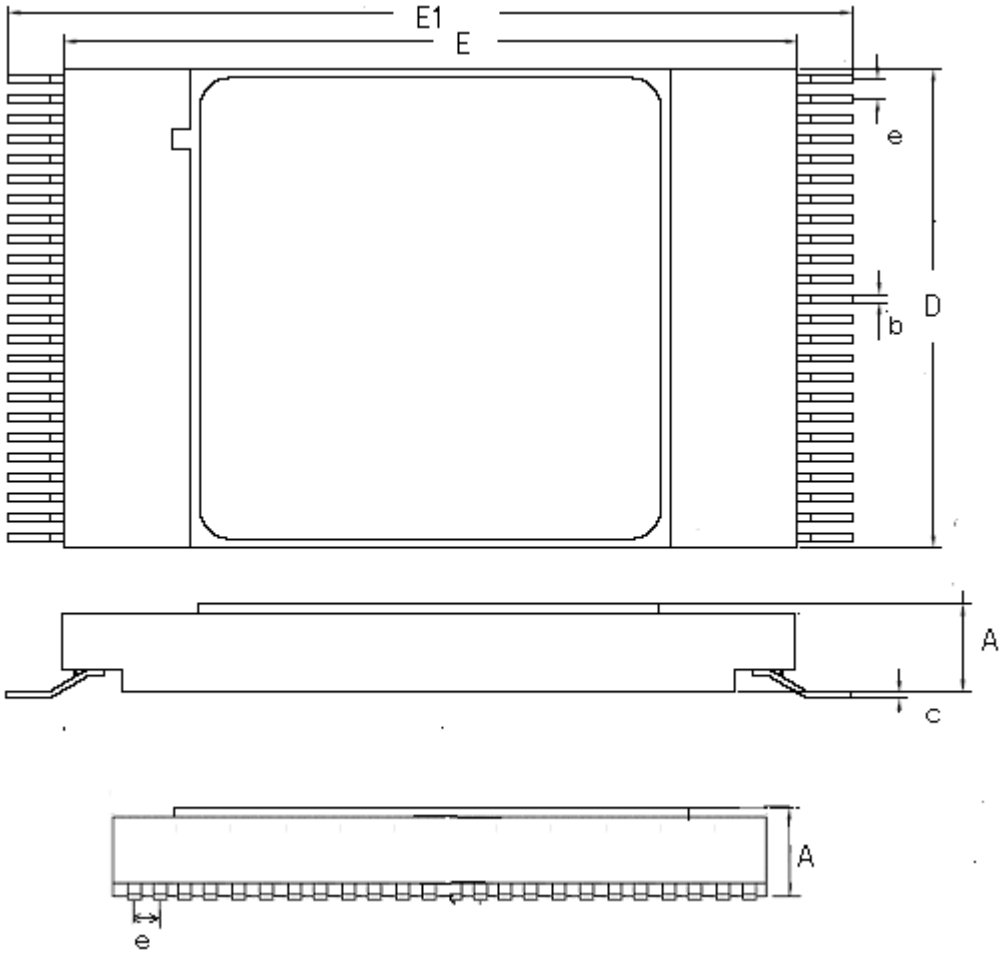


Figure 18. CSOP48 dimensions

Unit is mm

Dimension Symbols	Numeric		
	Minimum	Nominal	Maximum
D	11.80	—	12.20
E	18.20	—	18.60
E1	20.88	—	21.48
A	1.98	—	2.53
b	—	0.20	—
c	0.10	—	0.20

e	—	0.50	—
b	0.15	—	0.25

- The device adopts 48-lead FBGA package, and its dimensions refer to the provisions of GB/T 7092-1993. The shell shape is shown in Figure 19.

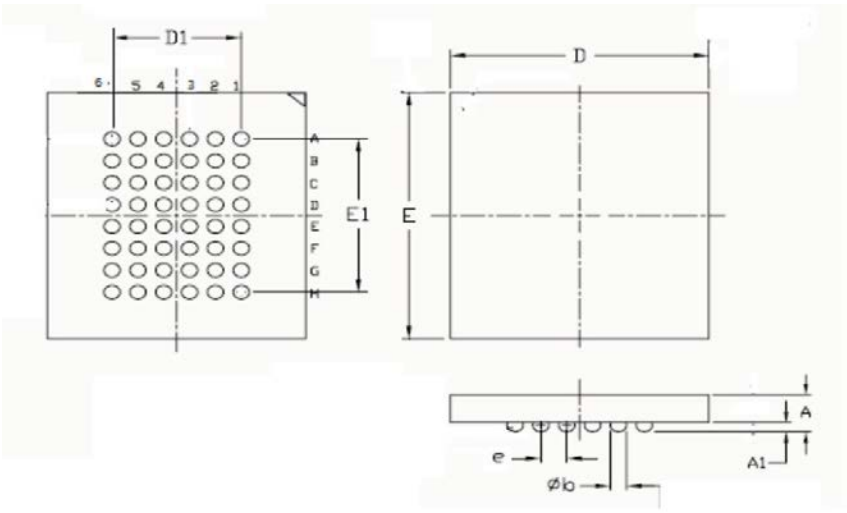


Figure 19. FBGA48 dimensions

Unit is mm

Dimension symbols	Numeric		
	Minimum	Nominal	maximum
A	—	—	1.2
A1	0.26	—	0.34
D	7.90	—	8.10
E	8.90	—	9.10
D1	—	4.00	—
E1	—	5.60	—
Φb	0.35	—	0.45

e	—	0.80	—

XII. Ordering Information

model	Package	Packaging materials	Quality Grade	General Specifications	Detailed specification number	Product Status
BST32PMCSOP48	CSOP8	ceramics	Class B	GJB597B-2012	Q/BST 20207-2015	Mass production
BST32PMFBGA48	BGA48	plastic	N1 Level	GJB7400-2011	Q/BST 20220-2015	Mass production
BST32PEFBGA48	BGA48	plastic	Military temperature grade	GJB7400-2011	Q/BST 20221-2015	Mass production