# BST32F7 Series
# Datasheet v2.0

32-bit RISC Kernel 216MHzFrequency,Supports single and double precision floating point operations, built-in instruction/data dual 16K cache, 2MB FLASH, 512KB SRAM, Support external memory (FMC), integrated USB OTG HS/FS(built-in PHY), 10/100 EMAC, 2-waySDMMC, 1 QSPI, 3 CAN, 4/4USART/UART, 6 SPI, 4 I2C, 3indivual 12bit ADC, 2 indivual 12-bit DAC, 4 comparators

## I. Product Features

- **Kernel:**

  32-bit RISC core, operating frequency 216MHz, built-in single and double precision floating point unit.

- **Sorage**
  - 2M FLASH, support read and write synchronization;
  - 512Kbyte SRAM + 16Kbyte ITCM + 4Kbyte backup SRAM.
- **Power Management and Reset**
  - VDD: 2.1v - 3.6v;
  - VBAT: 2.0v - 3.6v;
  - POR, PDR, PVD, BOR.
  - Support external pin reset, software reset, low power mode reset, watchdog timer reset.
- **Clock**
  - HSE(4-26MHz);
  - LSE(32.768K);
  - -HSI(16MHz);
  - LSI (32KHz).

- **Timer:**
  - 8 16-bit general-purpose timers, 2 32-bit general-purpose timers, 2 advanced timers (support motor PWM complementary output), 2 basic timers, 2 watchdog timers, 1 low-power timer;
  - 128-bit unique ID.
- **Communication interface**
- 4 USARTs and 4 UARTs;
- 6 SPI;
- 4 I2C, of which I2C 2\3\4 supports SMBUS protocol;
- 3 CAN 2.0A/B.
- **High-speed interface**
  - USB 2.0 FS, built-in PHY;
  - USB 2.0 HS with ULPI support.
- **Storage Interface**:
  - 2 SDMMCs;
  - 1 x QSPI.
- **High-performance simulation**
  - 3 12bit, 1.5M ADC, up to 15CH;
  - 2 12-bit DACs;
  - 4 comparators;
  - Built-in temperature sensor.
- **GPIO: Up to 168**

  GPIO, up to 108MHz.
- **Debug** :

  SWD/JTAG.

- **Power consumption:**

  Current in running mode <270mA.

- **ESD:**

  HBM2000V.

- **Package:**
  - -LQFP64, LQFP100, LQFP144, LQFP176, LQFP208;
  - CQFP64, CQFP144;
  - PBGA176.
- **Quality Grade:**
  - Industrial grade (operating temperature -40℃~85℃) ;
  - Military temperature grade (operating temperature -55℃~125℃);
  - -N1Level (Operating Temperature -55℃~125℃) ;
  - -B class (Operating temperature -55℃~125℃) ;
  - Package compatible: STM32F7 series.

## II. Product introducion

The BST32F7 series is based on a high-performance 32-bit RISC core with a typical operating frequency of 216MHz, integrated single and double precision floating point units, memory protection unit (MPU), supports single and double precision data processing instructions and data types, and supports DSP instructions.

The BST32F7 series has built-in 2M FLASH, 512K SRAM, including 128KB DTCM; 16K ITCM, 4KB Backup SRAM can be powered by VBAT to maintain data. The bus matrix supports multiple bus devices to access the memory at the same time, and supports access to internal and external storage.

The BST32F7 series integrates a wealth of peripherals, including 3 independent 12-bit 1.5MSPS ADCs, 2 independent 12-bit DACs, 4 comparators, one USB FS/HS each with

built-in FS PHY, 6 SPIs, 4 I2Cs, 2 SDMMCs, 1 QSPI, 4 USART/UARTs each, 3 CAN2.0 MACs, up to 18 timers, including 2 advanced timers, each supporting 3-way PWM output.

BST32F7 series supports wide voltage (2.1V~3.6V), wide temperature (-55℃~125℃) and various low power modes.

BST32F7 series provides 64PIN,100PIN,144PIN,176PIN,208PIN LQFP/CQFPand176PIN PBGAThe package is pin-compatible with the STM32F7 series and is suitable for high-performance control applications.

### 2.1. Model Naming convention


Figure 1-1 Model naming rules

- XXX represents products developed by XXX company
- 32F767 represents the product model
- Version ID: None means it is the first version of this product series
- Encapsulation
- PIN number
- Grade: Commercial Grade C, Industrial Grade I, Wide Temperature W, Military Temperature E, Military Grade M
- For more information on product grades, please contact your local sales representative

## 2.2. Model function comparisonTable

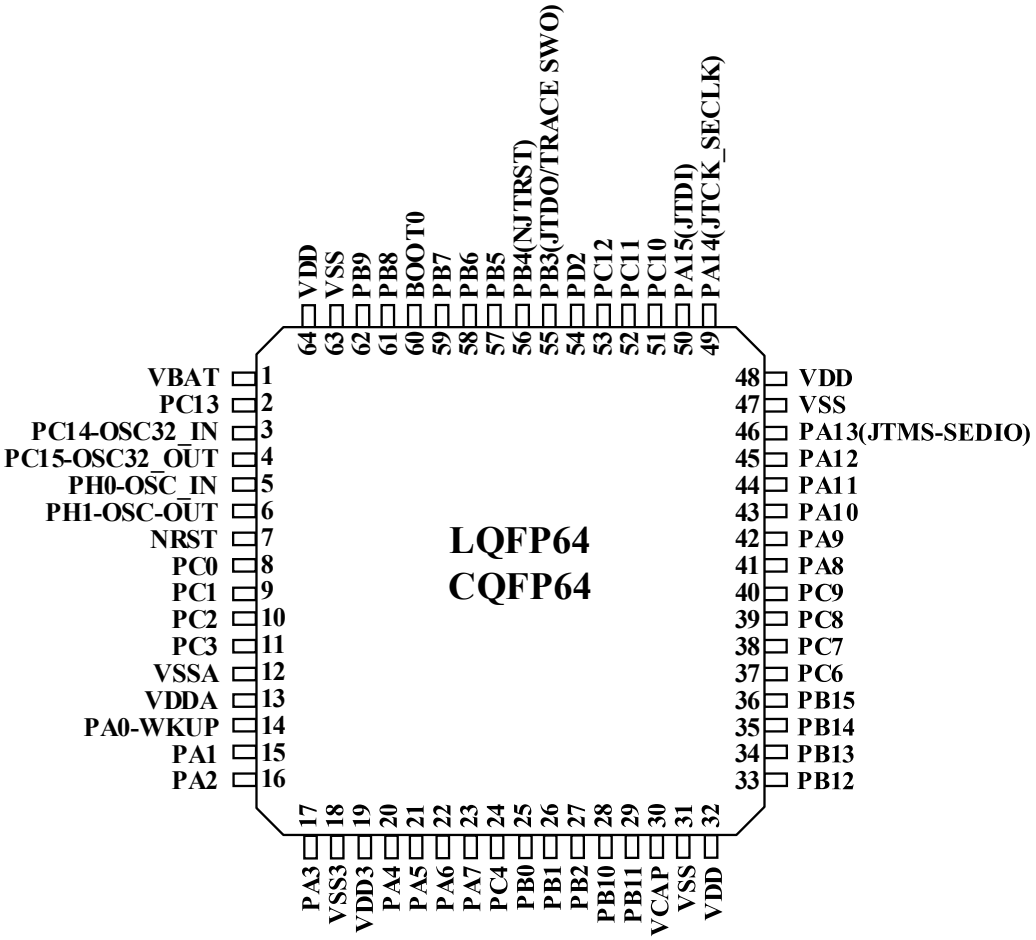
| PIN | | 64PIN | 100PIN | 144PIN | 176PIN | 208PIN |
|---|---|---|---|---|---|---|
| CPU HIGHEST OPERATING FREQUENCY | | 216M | | | | |
| L1 CACHE | | 16K+16K | | | | |
| OPERATING VOLTAGE | | 2.1v~3.6v | | | | |
| OPERATING TEMPERATURE | | -55℃~125℃(Military Temperature/N1)<br>-40℃~85℃(industry) | | | | |
| GPIO | | 50 | 82 | 114 | 140 | 168 |
| FLASH(KB) | | 2048 | | | | |
| SRAM(KB) | SYSTEM | 512 (built-in 128K DTCM) | | | | |
| | INSTRUCTION | 16 ITCM | | | | |
| | BACKUP | 4 | | | | |
| SDMMC | | 1 | 2 | 2 | 2 | 2 |
| FMC | | Not supported | | 1 | | |
| QSPI | | 1 | | | | |
| 10/100M ETHERNET | | 1 | | | | |
| TIMER | GENERAL PURPOSE TIMER | 10 | | | | |
| | ADVANCED TIMER | 2 | | | | |
| | BASIC TIMER | 2 | | | | |
| | LOW POWER TIMER | 1 | | | | |
| COMMUNICATION INTERFACE | SPI | 4 | 6 | | | |
| | I2C | 4(I2C1 does not support SMBUS) | | | | |
| | USART/UART | 4/3 | 4/4 | | | |

| | | |
|---|---|---|
| | USB OTG FS | Built-in FS PHY |
| | USB OTG HS | |

# IV. Product Pin Information

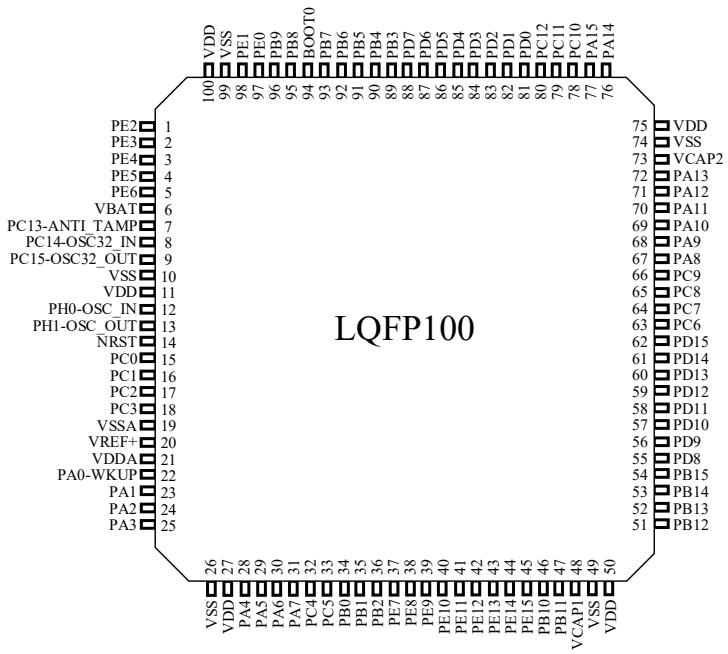
## 4.1. Package Pin Diagram

### 4.1.1. LQFP64 Encapsulation

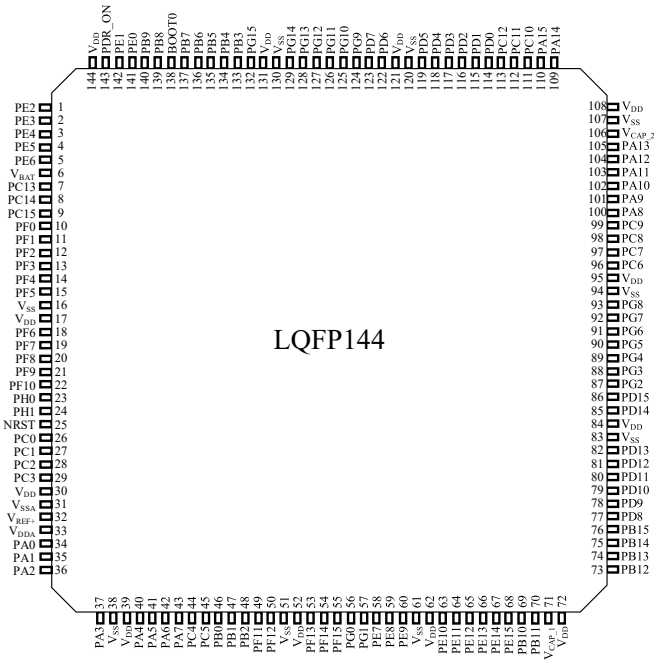



Picture 2-1. BST32F7 Series LQFP64 Pin Arrangement Pin Definition

### 4.1.2. LQFP100 Encapsulation

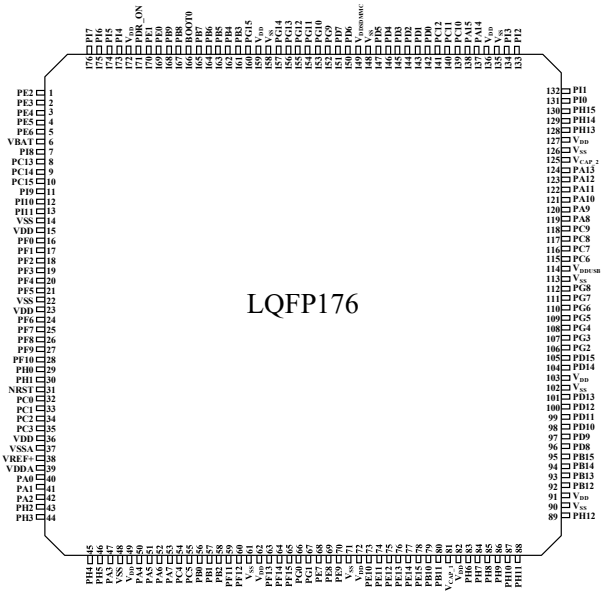



Picture 2-1. BST32F7 Series LQFP100 Pin Arrangement Pin Definition LQFP144 Encapsulation



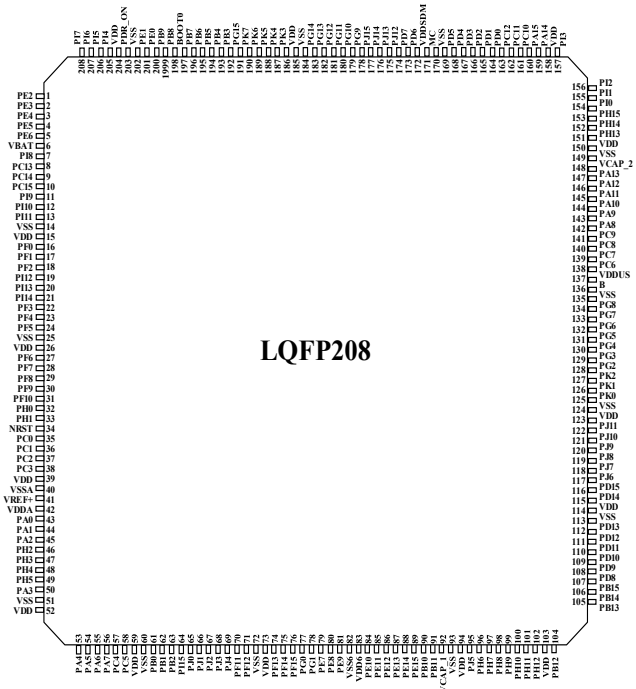

Picture 2-2, BST32F7 Series LQFP144 Pin Arrangement Pin Definition

### 4.1.3. LQFP176 Encapsulation



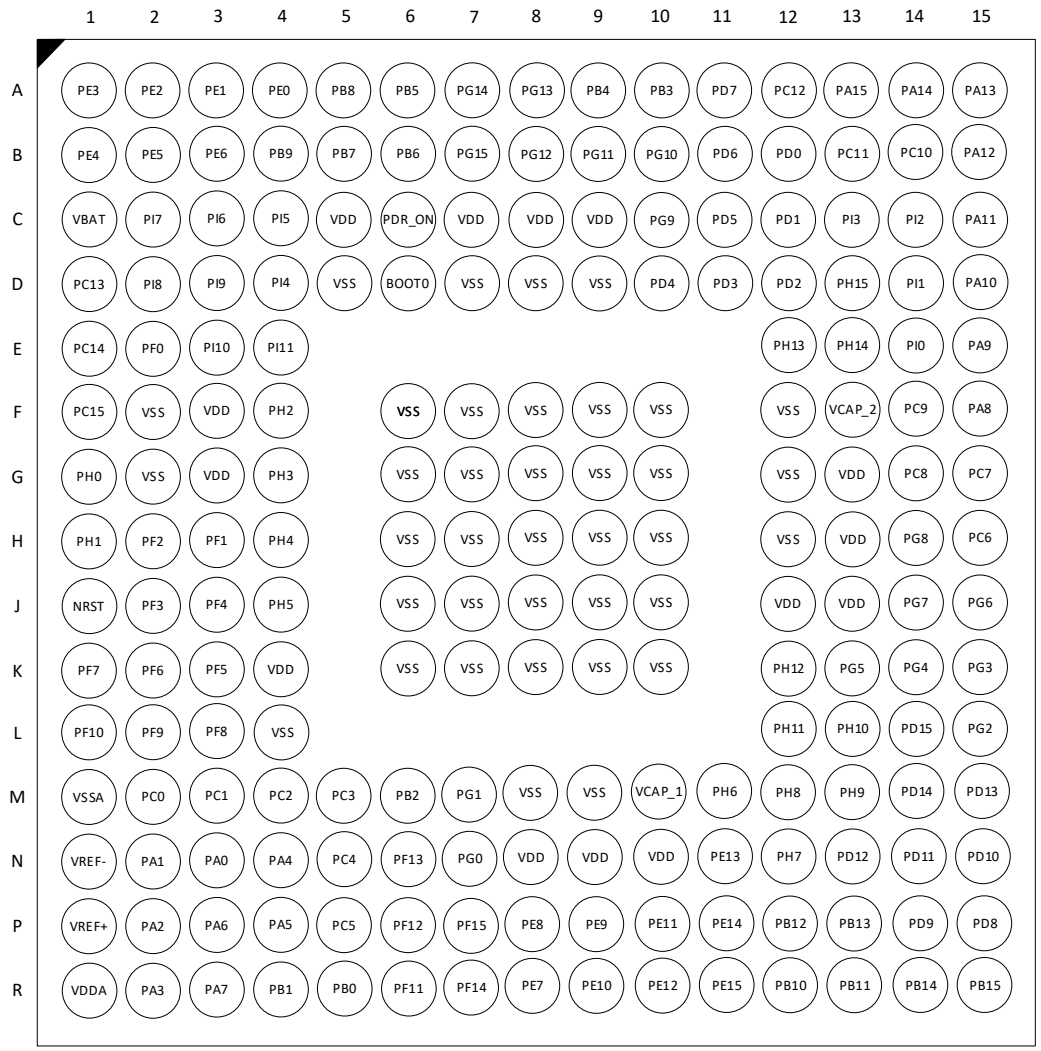

Picture 2-3. BST32F7 Series LQFP176 Pin Arrangement Pin Definition

### 4.1.4. LQFP208 Encapsulation




Picture.2-4. BST32F7 Series LQFP208 Pin Arrangement Pin Definition

### 4.1.5. PBGA176 Encapsulation




Picture 2-5. BST32F7 Series PBGA176 Pin Arrangement Pin Definition

# V. Pin function assignmentTable

## 5.1. Pinout Function Definition

| LQFP64 | LQFP100 | LQFP144 | LQFP176 | PBGA176 | LQFP208 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| - | 1 | 1 | 1 | A2 | 1 | PE2 | I/O | FT | TRACECLK, SPI4_SCK, FMC_A23, SAI1_MCLK_A, QUADSPI_BK1_IO2, ETH_MII_TXD3, EVENTOUT | ANA_VC4_AINP4 |
| - | 2 | 2 | 2 | A1 | 2 | PE3 | I/O | FT | TRACED0, FMC_A19, EVENTOUT, SAI1_SD_B | - |
| - | 3 | 3 | 3 | B1 | 3 | PE4 | I/O | FT | TRACED1, SPI4_NSS, FMC_A20, EVENTOUT, SAI1_FS_A | ANA_VC2_AINP5 |
| - | 4 | 4 | 4 | B2 | 4 | PE5 | I/O | FT | TRACED2, TIM9_CH1, SPI4_MISO, FMC_A21, EVENTOUT, SAI1_SCK_A | - |
| - | 5 | 5 | 5 | B3 | 5 | PE6 | I/O | FT | TRACED3, TIM1_BKIN2, TIM9_CH2, SPI4_MOSI, FMC_A22, EVENTOUT, SAI1_SD_A, SAI2_MCLK_B | - |
| 1 | 6 | 6 | 6 | C1 | 6 | VBAT | S | - | - | - |
| - | - | - | 7 | D2 | 7 | PI8 | I/O | FT | EVENTOUT | RTC_TAMP2, RTC_TS, WKUP5 |
| 2 | 7 | 7 | 8 | D1 | 8 | PC13 | I/O | FT | EVENTOUT | RTC_TAMP1,RTC_TS, RTC_OUT, WKUP4 |
| 3 | 8 | 8 | 9 | E1 | 9 | PC14 (OSC32_IN) | I/O | FT | EVENTOUT | OSC32_IN |

| LQFP64 | LQFP100 | LQFP144 | LQFP176 | PBGA176 | LQFP208 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| 4 | 9 | 9 | 10 | F1 | 10 | PC15 (OSC32_OUT) | I/O | FT | EVENTOUT | OSC32_OUT |
| - | - | - | 11 | D3 | 11 | PI9 | I/O | FT | UART4_RX, CAN1_RX, FMC_D30, EVENTOUT | ANA_VC2_AINP6 |
| - | - | - | 12 | E3 | 12 | PI10 | I/O | FT | ETH_MII_RX_ER, FMC_D31, EVENTOUT | - |
| - | - | - | 13 | E4 | 13 | PI11 | I/O | FT | OTG_HS_ULPI_DIR, EVENTOUT | WKUP6 |
| - | - | - | 14 | F2 | 14 | VSS | S | - | - | - |
| - | - | - | 15 | F3 | 15 | VDD | S | - | - | - |
| - | - | 10 | 16 | E2 | 16 | PF0 | I/O | FT | I2C2_SDA, FMC_A0, EVENTOUT | - |
| - | - | 11 | 17 | H3 | 17 | PF1 | I/O | FT | I2C2_SCL、FMC_A1、EVENTOUT | ANA_VC2_AINP7 |
| - | - | 12 | 18 | H2 | 18 | PF2 | I/O | FT | I2C2_SMBA, FMC_A2, EVENTOUT | - |
| - | - | - | - | - | 19 | PI12 | I/O | FT | EVENTOUT | - |
| - | - | - | - | - | 20 | PI13 | I/O | FT | EVENTOUT | - |
| - | - | - | - | - | 21 | PI14 | I/O | FT | EVENTOUT | - |
| - | - | 13 | 19 | J2 | 22 | PF3 | I/O | FT | FMC_A3, EVENTOUT | ADC3_IN9 |
| - | - | 14 | 20 | J3 | 23 | PF4 | I/O | FT | FMC_A4、EVENTOUT | ADC3_IN14 |

| LQFP64 | LQFP100 | LQFP144 | LQFP176 | PBGA176 | LQFP208 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| - | - | 15 | 21 | K3 | 24 | PF5 | I/O | FT | FMC_A5、EVENTOUT | ADC3_IN15 |
| - | 10 | 16 | 22 | G2 | 25 | VSS | S | - | - | - |
| - | 11 | 17 | 23 | G3 | 26 | VDD | S | - | - | - |
| - | - | 18 | 24r | K2 | 27 | PF6 | I/O | FT | TIM10_CH1, SPI5_NSS, UART7_Rx, SAI1_SD_B, QUADSPI_BK1_IO3, EVENTOUT, | ADC3_IN4 |
| - | - | 19 | 25 | K1 | 28 | PF7 | I/O | FT | TIM11_CH1, SPI5_SCK, UART7_TX, SAI1_MCLK_B, QUADSPI_BK1_IO2, EVENTOUT | ADC3_IN5 |
| - | - | 20 | 26 | L3 | 29 | PF8 | I/O | FT | SPI5_MISO, UART7_RTS, TIM13_CH1, SAI1_SCK_B QUADSPI_BK1_IO0, EVENTOUT | ADC3_IN6 |
| - | - | 21 | 27 | L2 | 30 | PF9 | I/O | FT | SPI5_MOSI, UART7_CTS, TIM14_CH1, SAI1_FS_B, QUADSPI_BK1_IO1, EVENTOUT | ADC3_IN7 |
| - | - | 22 | 28 | L1 | 31 | PF10 | I/O | FT | QUADSPI_CLK、EVENTOUT | ADC3_IN8 |
| 5 | 12 | 23 | 29 | G1 | 32 | PH0(OSC_IN) | I/O | FT | EVENTOUT | OSC_IN |
| 6 | 13 | 24 | 30 | H1 | 33 | PH1(OSC_OUT) | I/O | FT | EVENTOUT | OSC_OUT |
| 7 | 14 | 25 | 31 | J1 | 34 | NRST | I/O | RST | - | - |
| 8 | 15 | 26 | 32 | M2 | 35 | PC0 | I/O | FT | OTG_HS_ULPI_STP, FMC_SDNWE, EVENTOUT, SAI2_FS_B | ADC1_IN10, ADC2_IN10, ADC3_IN10 |

| LQFP64 | LQFP100 | LQFP144 | LQFP176 | PBGA176 | LQFP208 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| 9 | 16 | 27 | 33 | M3 | 36 | PC1 | I/O | FT | TRACED0, SPI2_MOSI/I2S2_SD, ETH_MDC, MDIOS_MDC, EVENTOUT, SAI1_SD_A | ADC1_IN11, ADC2_IN11, ADC3_IN11, RTC_TAMP3, WKUP3 |
| 10 | 17 | 28 | 34 | M4 | 37 | PC2 | I/O | FT | SPI2_MISO, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT | ADC1_IN12, ADC2_IN12, ADC3_IN12, ANA_VC3_AINP0 |
| 11 | 18 | 29 | 35 | M5 | 38 | PC3 | I/O | FT | SPI2_MOSI/I2S2_SD, EVENTOUT, FMC_SDCKE0, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, | ADC1_IN13, ADC2_IN13, ADC3_IN13, ANA_VC3_AINN0 |
| - | - | 30 | 36 | - | 39 | VDD | S | - | - | - |
| 12 | 19 | 31 | 37 | M1 | 40 | VSSA | S | - | - | - |
| - | - | - | - | N1 | - | VREF- | S | - | - | - |
| - | 20 | 32 | 38 | P1 | 41 | VREF+ | S | - | - | - |
| 13 | 21 | 33 | 39 | R1 | 42 | VDDA | S | - | - | - |
| 14 | 22 | 34 | 40 | N3 | 43 | PA0-WKUP | I/O | FT | TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, ETH_MII_CRS, EVENTOUT, SAI2_SD_B | ADC1_IN0, ADC2_IN0, ADC3_IN0, WKUP1 |

| LQFP64 | LQFP100 | LQFP144 | LQFP176 | PBGA176 | LQFP208 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 23 | 35 | 41 | N2 | 44 | PA1 | I/O | FT | TIM2_CH2, TIM5_CH2, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCLK_B, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, EVENTOUT | ADC1_IN1, ADC2_IN1, ADC3_IN1 |
| 16 | 24 | 36 | 42 | P2 | 45 | PA2 | I/O | FT | TIM2_CH3, TIM5_CH3, TIM9_CH1, USART2_TX,ETH_MDIO, MDIOS_MDIO, EVENTOUT, SAI2_SCK_B | ADC1_IN2, ADC2_IN2, ADC3_IN2, WKUP2 |
| - | - | - | 43 | F4 | 46 | PH2 | I/O | FT | LPTIM1_IN2, QUADSPI_BK2_IO0, ETH_MII_CRS, FMC_SDCKE0, EVENTOUT, SAI2_SCK_B | - |
| - | - | - | 44 | G4 | 47 | PH3 | I/O | FT | QUADSPI_BK2_IO1, ETH_MII_COL, FMC_SDNE0, EVENTOUT, SAI2_MCLK_B | - |
| - | - | - | 45 | H4 | 48 | PH4 | I/O | FT | I2C2_SCL, OTG_HS_ULPI_NXT, EVENTOUT | - |
| - | - | - | 46 | J4 | 49 | PH5 | I/O | FT | I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT | - |
| 17 | 25 | 37 | 47 | R2 | 50 | PA3 | I/O | FT | TIM2_CH4, TIM5_CH4, TIM9_CH2, USART2_RX, OTG_HS_ULPI_D0, ETH_MII_COL, EVENTOUT | ADC1_IN3, ADC2_IN3, ADC3_IN3 |
| 18 | 26 | 38 | 48 | L4 | 51 | VSS | S | - | - | - |
| 19 | 27 | 39 | 49 | K4 | 52 | VDD | S | - | - | - |
| 20 | 28 | 40 | 50 | N4 | 53 | PA4 | I/O | TTa | SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS, OTG_HS_SOF, EVENTOUT | ADC1_IN4, ADC2_IN4, DAC_OUT1 |
| 21 | 29 | 41 | 51 | P4 | 54 | PA5 | I/O | TTa | TIM2_CH1/TIM2_ETR, EVENTOUT, TIM8_CH1N, SPI1_SCK/I2S1_CK, SPI6_SCK, OTG_HS_ULPI_CK, | ADC1_IN5, ADC2_IN5, DAC_OUT2 |

| LQFP64 | LQFP100 | LQFP144 | LQFP176 | PBGA176 | LQFP208 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| 22 | 30 | 42 | 52 | P3 | 55 | PA6 | I/O | FT | TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO, SPI6_MISO, TIM13_CH1, MDIOS_MDC, EVENTOUT | ADC1_IN6, ADC2_IN6 |
| 23 | 31 | 43 | 53 | R3 | 56 | PA7 | I/O | FT | TIM1_CH1N, TIM3_CH2, TIM8_CH1N, FMC_SDNWE, SPI1_MOSI/I2S1_SD, SPI6_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, EVENTOUT | ADC1_IN7, ADC2_IN7 |
| 24 | 32 | 44 | 54 | N5 | 57 | PC4 | I/O | FT | I2S1_MCK, SPDIF_RX2, FMC_SDNE0, ETH_MII_RXD0/ETH_RMII_RXD0, EVENTOUT | ADC1_IN14, ADC2_IN14, ANA_VC1/2/3_AINP1 |
| - | 33 | 45 | 55 | P5 | 58 | PC5 | I/O | FT | SPDIF_RX3, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, EVENTOUT | ADC1_IN15, ADC2_IN15, ANA_VC1/2/3_AINN1 |
| - | - | - | - | - | 59 | VDD | S | - | - | - |
| - | - | - | - | - | 60 | VSS | S | - | - | - |
| 25 | 34 | 46 | 56 | R5 | 61 | PB0 | I/O | FT | TIM1_CH2N, TIM3_CH3, TIM8_CH2N, UART4_CTS, OTG_HS_ULPI_D1, ETH_MII_RXD2, EVENTOUT | ADC1_IN8, ADC2_IN8, ANA_VC1/2/4_AINP0 |
| 26 | 35 | 47 | 57 | R4 | 62 | PB1 | I/O | FT | TIM1_CH3N, TIM3_CH4, TIM8_CH3N, OTG_HS_ULPI_D2, ETH_MII_RXD3, EVENTOUT | ADC1_IN9, ADC2_IN9, ANA_VC1/2/4_AINN0 |
| 27 | 36 | 48 | 58 | M6 | 63 | PB2 | I/O | FT | SPI3_MOSI/I2S3_SD, QUADSPI_CLK, , EVENTOUT | ANA_VC1/2/3/4_AINP2 |
| - | - | - | - | - | 64 | PI15 | I/O | FT | EVENTOUT | - |
| - | - | - | - | - | 65 | PJ0 | I/O | FT | EVENTOUT | - |

| LQFP64 | LQFP100 | LQFP144 | LQFP176 | PBGA176 | LQFP208 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| - | - | - | - | - | 66 | PJ1 | I/O | FT | EVENTOUT | - |
| - | - | - | - | - | 67 | PJ2 | I/O | FT | EVENTOUT | - |
| - | - | - | - | - | 68 | PJ3 | I/O | FT | EVENTOUT | - |
| - | - | - | - | - | 69 | PJ4 | I/O | FT | EVENTOUT | - |
| - | - | 49 | 59 | R6 | 70 | PF11 | I/O | FT | SPI5_MOSI, SAI2_SD_B, FMC_SDNRAS, EVENTOUT | - |
| - | - | 50 | 60 | P6 | 71 | PF12 | I/O | FT | FMC_A6、EVENTOUT | - |
| - | - | 51 | 61 | M8 | 72 | VSS | S | - | - | - |
| - | - | 52 | 62 | N8 | 73 | VDD | S | - | - | - |
| - | - | 53 | 63 | N6 | 74 | PF13 | I/O | FT | I2C4_SMBA、FMC_A7、EVENTOUT | - |
| - | - | 54 | 64 | R7 | 75 | PF14 | I/O | FT | I2C4_SCL、FMC_A8、EVENTOUT | - |
| - | - | 55 | 65 | P7 | 76 | PF15 | I/O | FT | I2C4_SDA, FMC_A9, EVENTOUT | - |
| - | - | 56 | 66 | N7 | 77 | PG0 | I/O | FT | FMC_A10, EVENTOUT | - |
| - | - | 57 | 67 | M7 | 78 | PG1 | I/O | FT | FMC_A11, EVENTOUT | - |
| - | 37 | 58 | 68 | R8 | 79 | PE7 | I/O | FT | TIM1_ETR, UART7_Rx, QUADSPI_BK2_IO0, FMC_D4, EVENTOUT | ANA_VC1/2/3/4_AINN2 |

| LQFP64 | LQFP100 | LQFP144 | LQFP176 | PBGA176 | LQFP208 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| - | 38 | 59 | 69 | P8 | 80 | PE8 | I/O | FT | TIM1_CH1N, UART7_Tx, QUADSPI_BK2_IO1, FMC_D5, EVENTOUT | |
| - | 39 | 60 | 70 | P9 | 81 | PE9 | I/O | FT | TIM1_CH1, UART7_RTS, QUADSPI_BK2_IO2,, FMC_D6, EVENTOUT | ANA_VC1/2/3/4_AINP3 |
| - | - | 61 | 71 | M9 | 82 | VSS | S | - | - | - |
| - | - | 62 | 72 | N9 | 83 | VDD | S | - | - | - |
| - | 40 | 63 | 73 | R9 | 84 | PE10 | I/O | FT | TIM1_CH2N, UART7_CTS, QUADSPI_BK2_IO3, FMC_D7, EVENTOUT | ANA_VC1/2/3/4_AINN3 |
| - | 41 | 64 | 74 | P10 | 85 | PE11 | I/O | FT | TIM1_CH2, SPI4_NSS, FMC_D8, EVENTOUT, SAI2_SD_B | ANA_VC1/2/3_AINP4 |
| - | 42 | 65 | 75 | R10 | 86 | PE12 | I/O | FT | TIM1_CH3N, SPI4_SCK, FMC_D9, EVENTOUT, SAI2_SCK_B | - |
| - | 43 | 66 | 76 | N11 | 87 | PE13 | I/O | FT | TIM1_CH3, SPI4_MISO, FMC_D10, EVENTOUT, SAI2_FS_B | - |
| - | 44 | 67 | 77 | P11 | 88 | PE14 | I/O | FT | TIM1_CH4, SPI4_MOSI, FMC_D11, EVENTOUT, SAI2_MCLK_B | - |
| - | 45 | 68 | 78 | R11 | 89 | PE15 | I/O | FT | TIM1_BKIN, FMC_D12, EVENTOUT | - |
| 28 | 46 | 69 | 79 | R12 | 90 | PB10 | I/O | FT | TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, USART3_TX, QUADSPI_BK1_NCS, OTG_HS_ULPI_D3, ETH_MII_RX_ER, EVENTOUT | - |

| LQFP64 | LQFP100 | LQFP144 | LQFP176 | PBGA176 | LQFP208 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | |
| 29 | 47 | 70 | 80 | R13 | 91 | PB11 | I/O | FT | TIM2_CH4, I2C2_SDA, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, EVENTOUT | - |
| 30 | 48 | 71 | 81 | M10 | 92 | VCAP_1 | S | - | - | - |
| 31 | 49 | | | | 93 | VSS | S | | - | - |
| 32 | 50 | 72 | 82 | N10 | 94 | VDD | S | - | - | - |
| - | - | - | - | - | 95 | PJ5 | I/O | FT | EVENTOUT | - |
| - | - | - | 83 | M11 | 96 | PH6 | I/O | FT | I2C2_SMBA, SPI5_SCK, TIM12_CH1, ETH_MII_RXD2, FMC_SDNE1, EVENTOUT | - |
| - | - | - | 84 | N12 | 97 | PH7 | I/O | FT | I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, EVENTOUT | ANA_VC1_AINP5 |
| - | - | - | 85 | M12 | 98 | PH8 | I/O | FT | I2C3_SDA, FMC_D16, EVENTOUT | - |
| - | - | - | 86 | M13 | 99 | PH9 | I/O | FT | I2C3_SMBA, TIM12_CH2, FMC_D17, EVENTOUT | - |
| - | - | - | 87 | L13 | 100 | PH10 | I/O | FT | TIM5_CH1, I2C4_SMBA, ,FMC_D18, EVENTOUT | - |
| - | - | - | 88 | L12 | 101 | PH11 | I/O | FT | TIM5_CH2, I2C4_SCL, FMC_D19, EVENTOUT | ANA_VC1_AINP6 |

| LQFP64 | LQFP100 | LQFP144 | LQFP176 | PBGA176 | LQFP208 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| - | - | - | 89 | K12 | 102 | PH12 | I/O | FT | TIM5_CH3, I2C4_SDA, FMC_D20, EVENTOUT | - |
| - | - | - | 90 | H12 | - | VSS | S | - | - | - |
| - | - | - | 91 | J12 | 103 | VDD | S | - | - | - |
| 33 | 51 | 73 | 92 | P12 | 104 | PB12 | I/O | FT | TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, USART3_CK, UART5_RX, CAN2_RX, OTG_HS_ULPI_D5, EVENTOUT, OTG_HS_ID ETH_MII_TXD0/ETH_RMII_TXD0, EVENTOUT | - |
| 34 | 52 | 74 | 93 | P13 | 105 | PB13 | I/O | FT | TIM1_CH1N, SPI2_SCK/I2S2_CK, USART3_CTS, UART5_TX, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, EVENTOUT | OTG_HS_VBUS |
| 35 | 53 | 75 | 94 | R14 | 106 | PB14 | I/O | FT | TIM1_CH2N, TIM8_CH2N, USART1_TX, SPI2_MISO, USART3_RTS, UART4_RTS, TIM12_CH1, SDMMC2_D0, OTG_HS_DM, EVENTOUT | - |
| 36 | 54 | 76 | 95 | R15 | 107 | PB15 | I/O | FT | RTC_REFIN, TIM1_CH3N, TIM8_CH3N, USART1_RX, SPI2_MOSI/I2S2_SD, UART4_CTS, TIM12_CH2, SDMMC2_D1, OTG_HS_DP, EVENTOUT | ANA_VC1_AINP7 |
| - | 55 | 77 | 96 | P15 | 108 | PD8 | I/O | FT | USART3_TX, SPDIF_RX1,, FMC_D13, EVENTOUT | ANA_VC3_AINP5 |
| - | 56 | 78 | 97 | P14 | 109 | PD9 | I/O | FT | USART3_RX, FMC_D14, EVENTOUT | - |

| LQFP64 | LQFP100 | LQFP144 | LQFP176 | PBGA176 | LQFP208 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| - | 57 | 79 | 98 | N15 | 110 | PD10 | I/O | FT | USART3_CK, FMC_D15, EVENTOUT | - |
| - | 58 | 80 | 99 | N14 | 111 | PD11 | I/O | FT | I2C4_SMBA, USART3_CTS, QUADSPI_BK1_IO0, FMC_A16/FMC_CLE, EVENTOUT, SAI2_SD_A | ANA_VC3_AINP6 |
| - | 59 | 81 | 100 | N13 | 112 | PD12 | I/O | FT | TIM4_CH1, LPTIM1_IN1, I2C4_SCL, USART3_RTS, QUADSPI_BK1_IO1, FMC_A17/FMC_ALE, EVENTOUT, SAI2_FS_A | - |
| - | 60 | 82 | 101 | M15 | 113 | PD13 | I/O | FT | TIM4_CH2, LPTIM1_OUT, I2C4_SDA, QUADSPI_BK1_IO3, FMC_A18, EVENTOUT, SAI2_SCK_A | ANA_VC3_AINP7 |
| - | - | 83 | 102 | - | 114 | VSS | S | - | - | - |
| - | - | 84 | 103 | J13 | 115 | VDD | S | - | - | - |
| - | 61 | 85 | 104 | M14 | 116 | PD14 | I/O | FT | TIM4_CH3, UART8_CTS, FMC_D0, EVENTOUT | - |
| - | 62 | 86 | 105 | L14 | 117 | PD15 | I/O | FT | TIM4_CH4, UART8_RTS, FMC_D1, EVENTOUT | - |
| - | - | - | - | - | 118 | PJ6 | I/O | FT | EVENTOUT | - |
| - | - | - | - | - | 119 | PJ7 | I/O | FT | EVENTOUT | - |
| - | - | - | - | - | 120 | PJ8 | I/O | FT | EVENTOUT | - |
| - | - | - | - | - | 121 | PJ9 | I/O | FT | EVENTOUT | - |
| - | - | - | - | - | 122 | PJ10 | I/O | FT | EVENTOUT | - |

| LQFP64 | LQFP100 | LQFP144 | LQFP176 | PBGA176 | LQFP208 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| - | - | - | - | - | 123 | PJ11 | I/O | FT | EVENTOUT | - |
| - | - | - | - | - | 124 | VDD | S | - | - | - |
| - | - | - | - | - | 125 | VSS | S | - | - | - |
| - | - | - | - | - | 126 | PK0 | I/O | FT | EVENTOUT | - |
| - | - | - | - | - | 127 | PK1 | I/O | FT | EVENTOUT | - |
| - | - | - | - | - | 128 | PK2 | I/O | FT | EVENTOUT | - |
| - | - | 87 | 106 | L15 | 129 | PG2 | I/O | FT | FMC_A12, EVENTOUT | - |
| - | - | 88 | 107 | K15 | 130 | PG3 | I/O | FT | FMC_A13, EVENTOUT | - |
| - | - | 89 | 108 | K14 | 131 | PG4 | I/O | FT | FMC_A14/FMC_BA0, EVENTOUT | - |
| - | - | 90 | 109 | K13 | 132 | PG5 | I/O | FT | FMC_A15/FMC_BA1, EVENTOUT | - |
| - | - | 91 | 110 | J15 | 133 | PG6 | I/O | FT | FMC_NE3, EVENTOUT | - |
| - | - | 92 | 111 | J14 | 134 | PG7 | I/O | FT | USART6_CK, FMC_INT, EVENTOUT, SAI1_MCLK_A | - |
| - | - | 93 | 112 | H14 | 135 | PG8 | I/O | FT | SPI6_NSS, SPDIF_RX2, USART6_RTS, ETH_PPS_OUT, FMC_SDCLK, EVENTOUT | - |

| LQFP64 | LQFP100 | LQFP144 | LQFP176 | PBGA176 | LQFP208 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| - | - | 94 | 113 | G12 | 136 | VSS | S | - | - | - |
| - | - | 95 | 114 | H13 | 137 | VDD | S | - | - | - |
| 37 | 63 | 96 | 115 | H15 | 138 | PC6 | I/O | FT | TIM3_CH1, TIM8_CH1, USART6_TX, FMC_NWAIT, SDMMC2_D6, SDMMC1_D6, EVENTOUT, I2S2_MCK | - |
| 38 | 64 | 97 | 116 | G15 | 139 | PC7 | I/O | FT | TIM3_CH2, TIM8_CH2、I2S3_MCK、USART6_RX, FMC_NE1, SDMMC2_D7, SDMMC1_D7, EVENTOUT | - |
| 39 | 65 | 98 | 117 | G14 | 140 | PC8 | I/O | FT | TRACED1, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, FMC_NE2/FMC_NCE, SDMMC1_D0, EVENTOUT | ANA_VC4_AINP1 |
| 40 | 66 | 99 | 118 | F14 | 141 | PC9 | I/O | FT | MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, UART5_CTS, QUADSPI_BK1_IO0, SDMMC1_D1, I2S_CKIN, EVENTOUT | ANA_VC4_AINN1 |
| 41 | 67 | 100 | 119 | F15 | 142 | PA8 | I/O | FT | MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, CAN3_RX, UART7_RX, EVENTOUT | - |
| 42 | 68 | 101 | 120 | E15 | 143 | PA9 | I/O | FT | TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, EVENTOUT | OTG_FS_VBUS |
| 43 | 69 | 102 | 121 | D15 | 144 | PA10 | I/O | FT | TIM1_CH3, USART1_RX, OTG_FS_ ID, MDIOS_MDIO, EVENTOUT | - |
| 44 | 70 | 103 | 122 | C15 | 145 | PA11 | I/O | TTa | TIM1_CH4, SPI2_NSS/I2S2_WS, UART4_RX, USART1_CTS, CAN1_RX, OTG_FS_DM, EVENTOUT | - |
| 45 | 71 | 104 | 123 | B15 | 146 | PA12 | I/O | TTa | TIM1_ETR, SPI2_SCK/I2S2_CK, UART4_TX, USART1_RTS, CAN1_TX, OTG_FS_DP, EVENTOUT, SAI2_FS_B | - |

| LQFP64 | LQFP100 | LQFP144 | LQFP176 | PBGA176 | LQFP208 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| 46 | 72 | 105 | 124 | A15 | 147 | PA13(JTMS-SWDIO) | I/O | FT | JTMS/SWDIO、EVENTOUT | - |
| - | 73 | 106 | 125 | F13 | 148 | VCAP_2 | S | - | - | - |
| 47 | 74 | 107 | 126 | F12 | 149 | VSS | S | - | - | - |
| 48 | 75 | 108 | 127 | G13 | 150 | VDD | S | - | - | - |
| - | - | - | 128 | E12 | 151 | PH13 | I/O | FT | TIM8_CH1N, UART4_TX, CAN1_TX, FMC_D21, EVENTOUT | - |
| - | - | - | 129 | E13 | 152 | PH14 | I/O | FT | TIM8_CH2N, UART4_RX, CAN1_RX, FMC_D22, EVENTOUT | - |
| - | - | - | 130 | D13 | 153 | PH15 | I/O | FT | TIM8_CH3N, FMC_D23, EVENTOUT | - |
| - | - | - | 131 | E14 | 154 | PI0 | I/O | FT | TIM5_CH4, SPI2_NSS/I2S2_WS, FMC_D24, EVENTOUT | - |
| - | - | - | 132 | D14 | 155 | PI1 | I/O | FT | TIM8_BKIN2, SPI2_SCK/I2S2_CK, FMC_D25, EVENTOUT | - |
| - | - | - | 133 | C14 | 156 | PI2 | I/O | FT | TIM8_CH4, SPI2_MISO, FMC_D26, EVENTOUT | - |
| - | - | - | 134 | C13 | 157 | PI3 | I/O | FT | TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, EVENTOUT | - |

| LQFP64 | LQFP100 | LQFP144 | LQFP176 | PBGA176 | LQFP208 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| - | - | - | 135 | D9 | - | VSS | S | - | - | - |
| - | - | - | 136 | C9 | 158 | VDD | S | - | - | - |
| 49 | 76 | 109 | 137 | A14 | 159 | PA14(JTCK-SWCLK) | I/O | FT | JTCK-SWCLK, EVENTOUT | - |
| 50 | 77 | 110 | 138 | A13 | 160 | PA15(JTDI) | I/O | FT | JTDI, TIM2_CH1/TIM2_ETR, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI6_NSS, UART4_RTS, CAN3_TX, UART7_TX, EVENTOUT | - |
| 51 | 78 | 111 | 139 | B14 | 161 | PC10 | I/O | FT | SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDMMC1_D2, EVENTOUT | - |
| 52 | 79 | 112 | 140 | B13 | 162 | PC11 | I/O | FT | SPI3_MISO, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDMMC1_D3, EVENTOUT | ANA_VC4_AINP5 |
| 53 | 80 | 113 | 141 | A12 | 163 | PC12 | I/O | FT | TRACED3, SPI3_MOSI/I2S3_SD, USART3_CK, SDMMC1_CK, UART5_TX, EVENTOUT | - |
| - | 81 | 114 | 142 | B12 | 164 | PD0 | I/O | FT | UART4_RX, CAN1_RX, FMC_D2, EVENTOUT | - |
| - | 82 | 115 | 143 | C12 | 165 | PD1 | I/O | FT | UART4_TX, CAN1_TX, FMC_D3, EVENTOUT | - |
| 54 | 83 | 116 | 144 | D12 | 166 | PD2 | I/O | FT | TRACED2, TIM3_ETR, UART5_RX, SDMMC1_CMD, EVENTOUT | ANA_VC4_AINP6 |
| - | 84 | 117 | 145 | D11 | 167 | PD3 | I/O | FT | SPI2_SCK/I2S2_CK, USART2_CTS, FMC_CLK, EVENTOUT | - |

| LQFP64 | LQFP100 | LQFP144 | LQFP176 | PBGA176 | LQFP208 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| - | 85 | 118 | 146 | D10 | 168 | PD4 | I/O | FT | USART2_RTS, FMC_NOE, EVENTOUT | - |
| - | 86 | 119 | 147 | C11 | 169 | PD5 | I/O | FT | USART2_TX, FMC_NWE, EVENTOUT | - |
| - | - | 120 | 148 | D8 | 170 | VSS | S | - | - | - |
| - | - | 121 | 149 | C8 | 171 | VDD | S | - | - | - |
| - | 87 | 122 | 150 | B11 | 172 | PD6 | I/O | FT | SPI3_MOSI/I2S3_SD, SAI1_SD_A, USART2_RX, SDMMC2_CK, FMC_NWAIT, EVENTOUT | - |
| - | 88 | 123 | 151 | A11 | 173 | PD7 | I/O | FT | SPI1_MOSI/I2S1_SD, USART2_CK, SPDIF_RX0, SDMMC2_CMD, FMC_NE1, EVENTOUT | - |
| - | - | - | - | - | 174 | PJ12 | I/O | FT | EVENTOUT | - |
| - | - | - | - | - | 175 | PJ13 | I/O | FT | EVENTOUT | ANA_VC4_AINP7 |
| - | - | - | - | - | 176 | PJ14 | I/O | FT | EVENTOUT | - |
| - | - | - | - | - | 177 | PJ15 | I/O | FT | EVENTOUT | - |
| - | - | 124 | 152 | C10 | 178 | PG9 | I/O | FT | SPI1_MISO, SPDIF_RX3,, USART6_RX, QUADSPI_BK2_IO2, SDMMC2_D0, FMC_NE2/FMC_NCE, EVENTOUT, SAI2_FS_B | - |
| - | - | 125 | 153 | B10 | 179 | PG10 | I/O | FT | SPI1_NSS/I2S1_WS, SDMMC2_D1, SAI2_SD_B, FMC_NE3, EVENTOUT | - |

| LQFP64 | LQFP100 | LQFP144 | LQFP176 | PBGA176 | LQFP208 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| - | - | 126 | 154 | B9 | 180 | PG11 | I/O | FT | SPI1_SCK/I2S1_CK, SPDIF_RX0, SDMMC2_D2, ETH_MII_TX_EN/ETH_RMII_TX_EN, EVENTOUT | - |
| - | - | 127 | 155 | B8 | 181 | PG12 | I/O | FT | LPTIM1_IN1, SPI6_MISO, SPDIF_RX1, USART6_RTS, SDMMC2_D3, FMC_NE4, EVENTOUT | - |
| - | - | 128 | 156 | A8 | 182 | PG13 | I/O | FT | TRACED0,, LPTIM1_OUT, SPI6_SCK, USART6_CTS, EVENTOUT, ETH_MII_TXD0/ETH_RMII_TXD0, FMC_A24 | - |
| - | - | 129 | 157 | A7 | 183 | PG14 | I/O | FT | TRACED1, LPTIM1_ETR, SPI6_MOSI, QUADSPI_BK2_IO3, FMC_A25, ETH_MII_TXD1/ETH_RMII_TXD1, USART6_TX, EVENTOUT | - |
| - | - | 130 | 158 | D7 | 184 | VSS | S | - | - | - |
| - | - | 131 | 159 | C7 | 185 | VDD | S | - | - | - |
| - | - | - | - | - | 186 | PK3 | I/O | FT | EVENTOUT | - |
| - | - | - | - | - | 187 | PK4 | I/O | FT | EVENTOUT | - |
| - | - | - | - | - | 188 | PK5 | I/O | FT | EVENTOUT | - |
| - | - | - | - | - | 189 | PK6 | I/O | FT | EVENTOUT | - |
| - | - | - | - | - | 190 | PK7 | I/O | FT | EVENTOUT | - |
| - | - | 132 | 160 | B7 | 191 | PG15 | I/O | FT | USART6_CTS, FMC_SDNCAS, EVENTOUT | - |

| LQFP64 | LQFP100 | LQFP144 | LQFP176 | PBGA176 | LQFP208 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| 55 | 89 | 133 | 161 | A10 | 192 | PB3 (JTDO/TRACESWO) | I/O | FT | JTDO/TRACESWO, TIM2_CH2, SPI1_SCK/I2S1_CK, SPI6_SCK, SPI3_SCK/I2S3_CK, SDMMC2_D2, CAN3_RX, UART7_RX 、EVENTOUT | - |
| 56 | 90 | 134 | 162 | A9 | 193 | PB4(NJTRST) | I/O | FT | NJTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, EVENTOUT, SPI2_NSS/I2S2_WS, SPI6_MISO, SDMMC2_D3, CAN3_TX, UART7_TX | - |
| 57 | 91 | 135 | 163 | A6 | 194 | PB5 | I/O | FT | UART5_RX, TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, FMC_SDCKE1, EVENTOUT, SPI6_MOSI, CAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT | - |
| 58 | 92 | 136 | 164 | B6 | 195 | PB6 | I/O | FT | UART5_TX, TIM4_CH1, I2C1_SCL, USART1_TX, CAN2_TX, QUADSPI_BK1_NCS, I2C4_SCL, FMC_SDNE1, EVENTOUT | - |
| 59 | 93 | 137 | 165 | B5 | 196 | PB7 | I/O | FT | TIM4_CH2, I2C1_SDA, USART1_RX, I2C4_SDA, FMC_NL, EVENTOUT | - |
| 60 | 94 | 138 | 166 | D6 | 197 | BOOT0 | I | B | - | VPP |
| 61 | 95 | 139 | 167 | A5 | 198 | PB8 | I/O | FT | I2C4_SCL, TIM4_CH3, TIM10_CH1, I2C1_SCL, UART5_RX, CAN1_RX, SDMMC2_D4, ETH_MII_TXD3, SDMMC1_D4, EVENTOUT | - |
| 62 | 96 | 140 | 168 | B4 | 199 | PB9 | I/O | FT | I2C4_SDA, TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, UART5_TX, CAN1_TX, SDMMC2_D5, I2C4_SMBA, SDMMC1_D5, EVENTOUT | - |
| - | 97 | 141 | 169 | A4 | 200 | PE0 | I/O | FT | TIM4_ETR, LPTIM1_ETR, UART8_Rx, FMC_NBL0, EVENTOUT, SAI2_MCLK_A | - |

| LQFP64 | LQFP100 | LQFP144 | LQFP176 | PBGA176 | LQFP208 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| - | 98 | 142 | 170 | A3 | 201 | PE1 | I/O | FT | LPTIM1_IN2, UART8_TX, FMC_NBL1, EVENTOUT | - |
| 63 | 99 | - | 171 | D5 | 202 | VSS | S | - | - | - |
| - | - | 143 | - | C6 | 203 | PDR_ON | S | - | - | - |
| 64 | 100 | 144 | 172 | C5 | 204 | VDD | S | - | - | - |
| - | - | - | 173 | D4 | 205 | PI4 | I/O | FT | TIM8_BKIN, FMC_NBL2, EVENTOUT, SAI2_MCLK_A | - |
| - | - | - | 174 | C4 | 206 | PI5 | I/O | FT | TIM8_CH1, FMC_NBL3, EVENTOUT, SAI2_SCK_A | - |
| - | - | - | 175 | C3 | 207 | PI6 | I/O | FT | TIM8_CH2, FMC_D28, EVENTOUT, SAI2_SD_A | - |
| - | - | - | 176 | C2 | 208 | PI7 | I/O | FT | TIM8_CH3, FMC_D29, EVENTOUT, SAI2_FS_A | - |

## 5.2. Pinout Function Reuse

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMMC1/MDIOS/OTG2_FS | - | - | SYS |
| PA | PA0 | - | TIM2_CH1/TIM2_ETR | TIM5_CH1 | TIM8_ETR | - | - | - | USART2_CTS | UART4_TX | - | SAI2_SD_B | ETH_MII_CRS | - | - | - | EVENTOUT |
| | PA1 | - | TIM2_CH2 | TIM5_CH2 | - | - | - | - | USART2_RTS | UART4_RX | QUADSPI_BK1_IO3 | SAI2_MCLK_B | ETH_MII_RX_CLK/ETH_RMII_REF_CLK | - | - | - | EVENTOUT |
| | PA2 | - | TIM2_CH3 | TIM5_CH3 | TIM9_CH1 | - | - | - | USART2_TX | SAI2_SCK_B | - | - | ETH_MDIO | MDIOS_MDIO | - | - | EVENTOUT |
| | PA3 | - | TIM2_CH4 | TIM5_CH4 | TIM9_CH2 | - | - | - | USART2_RX | - | - | OTG_HS_ULPI_D0 | ETH_MII_COL | - | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMMC1/MDIOS/OTG2_FS | - | - | SYS |
| | PA4 | - | - | - | - | - | SPI1_NSS/I2S1_WS | SPI3_NSS/I2S3_WS | USART2_CK | SPI6_NSS | - | - | - | OTG_HS_SOF | - | - | EVENTOUT |
| | PA5 | - | TIM2_CH1/TIM2_ETR | - | TIM8_CH1N | - | SPI1_SCK/I2S1_CK | - | - | SPI6_SCK | - | OTG_HS_ULPI_CK | - | - | - | - | EVENTOUT |
| | PA6 | - | TIM1_BKIN_COMP0_OUT | TIM3_CH1 | TIM8_BKIN_COMP2_OUT | - | SPI1_MISO | - | - | SPI6_MISO | TIM13_CH1 | - | - | MDIOS_MDC | - | - | EVENTOUT |
| | PA7 | - | TIM1_CH1N | TIM3_CH2 | TIM8_CH1N | - | SPI1_MOSI/I2S1_SD | - | - | SPI6_MOSI | TIM14_CH1 | - | ETH_MII_RX_DV/ETH_RMII_CRS_DV | FMC_SDNWE | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMC1/MDIOS/OTG2_FS | - | - | SYS |
| | PA8 | MCO1 | TIM1_CH1 | - | TIM8_BKIN2_COMP3_OUT | I2C3_SCL | - | - | USART1_CK | - | - | OTG_FS_SOF | CAN3_RX | UART7_RX | - | - | EVENTOUT |
| | PA9 | - | TIM1_CH2 | - | - | I2C3_SMBA | SPI2_SCK/I2S2_CK | - | USART1_TX | - | - | - | - | - | - | - | EVENTOUT |
| | PA10 | - | TIM1_CH3 | - | - | - | - | - | USART1_RX | - | - | OTG_FS_ID | - | MDIOS_MDIO | - | - | EVENTOUT |
| | PA11 | - | TIM1_CH4 | - | - | - | SPI2_NSS/I2S2_WS | UART4_RX | USART1_CTS | - | CAN1_RX | OTG_FS_DM | - | - | - | - | EVENTOUT |
| | PA12 | - | TIM1_ETR | - | - | - | SPI2_SCK/I2S2_CK | UART4_TX | USART1_RTS | SAI2_FS_B | CAN1_TX | OTG_FS_DP | - | - | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMMC1/MDIOS/OTG2_FS | - | - | SYS |
| | PA13 | JTMS-SWDIO | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PA14 | JTCK-SWCLK | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PA15 | JTDI | TIM2_CH1/TIM2_ETR | - | - | | SPI1_NSS/I2S1_WS | SPI3_NSS/I2S3_WS | SPI6_NSS | UART4_RTS | - | - | CAN3_TX | UART7_TX | - | - | EVENTOUT |
| PB | PB0 | - | TIM1_CH2N | TIM3_CH3 | TIM8_CH2N | - | - | | - | UART4_CTS | - | OTG_HS_ULPI_D1 | ETH_MII_RXD2 | - | - | - | EVENTOUT |
| | PB1 | - | TIM1_CH3N | TIM3_CH4 | TIM8_CH3N | - | - | | - | - | - | OTG_HS_ULPI_D2 | ETH_MII_RXD3 | - | - | - | EVENTOUT |
| | PB2 | - | - | - | - | - | - | SAI1_SD_A | SPI3_MOSI/I | - | QUADSPI_CLK | | - | - | - | - | EVENTOUT |

| PORT | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMC1/MDIOS/OTG2_FS | - | - | SYS |
| | | | | | | | | 2S3_SD | | | | | | | | |
| PB3 | JTDO/TRACESWO | TIM2_CH2 | - | - | - | SPI1_SCK/I2S1_CK | SPI3_SCK/I2S3_CK | - | SPI6_SCK | - | SDMMC2_D2 | CAN3_RX | UART7_RX | - | - | EVENTOUT |
| PB4 | NJTRST | - | TIM3_CH1 | - | - | SPI1_MISO | SPI3_MISO | SPI2_NSS/I2S2_WS | SPI6_MISO | - | SDMMC2_D3 | CAN3_TX | UART7_TX | - | - | EVENTOUT |
| PB5 | - | UART5_RX | TIM3_CH2 | - | I2C1_SMBA | SPI1_MOSI/I2S1_SD | SPI3_MOSI/I2S3_SD | - | SPI6_MOSI | CAN2_RX | OTG_HS_ULPI_D7 | ETH_PPS_OUT | FMC_SDCKE1 | - | - | EVENTOUT |
| PB6 | - | UART5_TX | TIM4_CH1 | - | I2C1_SCL | - | | USART1_TX | - | CAN2_TX | QUADSPI_BK1_NCS | I2C4_SCL | FMC_SDNE1 | - | - | EVENTOUT |
| PB7 | - | - | TIM4_CH2 | - | I2C1_SDA | - | | USART1_RX | - | - | - | I2C4_SDA | FMC_NL | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMC1/MDIOS/OTG2_FS | - | - | SYS |
| | PB8 | - | I2C4_SCL | TIM4_CH3 | TIM10_CH1 | I2C1_SCL | - | | UART5_RX | - | CAN1_RX | SDMMC2_D4 | ETH_MII_TXD3 | SDMMC1_D4 | - | - | EVENTOUT |
| | PB9 | - | I2C4_SDA | TIM4_CH4 | TIM11_CH1 | I2C1_SDA | SPI2_NSS/I2S2_WS | | UART5_TX | - | CAN1_TX | SDMMC2_D5 | I2C4_SMBA | SDMMC1_D5 | - | - | EVENTOUT |
| | PB10 | - | TIM2_CH3 | - | - | I2C2_SCL | SPI2_SCK/I2S2_CK | | USART3_TX | - | QUADSPI_BK1_NCS | OTG_HS_ULPI_D3 | ETH_MII_RX_ER | - | - | - | EVENTOUT |
| | PB11 | - | TIM2_CH4 | - | - | I2C2_SDA | - | | USART3_RX | - | - | OTG_HS_ULPI_D4 | ETH_MII_TX_EN/ETH_RMII_TX_EN | - | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMMC1/MDIOS/OTG2_FS | - | - | SYS |
| | PB12 | - | TIM1_BKIN_COMP0_OUT | - | - | I2C2_SMBA | SPI2_NSS/I2S2_WS | | USART3_CK | UART5_RX | CAN2_RX | OTG_HS_ULPI_D5 | ETH_MII_TXD0/ETH_RMII_TXD0 | OTG_HS_ID | - | - | EVENTOUT |
| | PB13 | - | TIM1_CH1N | - | - | - | SPI2_SCK/I2S2_CK | | USART3_CTS | UART5_TX | CAN2_TX | OTG_HS_ULPI_D6 | ETH_MII_TXD1/ETH_RMII_TXD1 | - | - | - | EVENTOUT |
| | PB14 | - | TIM1_CH2N | - | TIM8_CH2N | USART1_TX | SPI2_MISO | | USART3_RTS | UART4_RTS | TIM12_CH1 | SDMMC2_D0 | - | OTG_HS_DM | - | - | EVENTOUT |
| | PB15 | RTC_REFIN | TIM1_CH3N | - | TIM8_CH3N | USART1_RX | SPI2_MOSI/I2S2_SD | | - | UART4_CTS | TIM12_CH2 | SDMMC2_D1 | - | OTG_HS_DP | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMMC1/MDIOS/OTG2_FS | - | - | SYS |
| PC | PC0 | - | - | - | | - | - | | - | SAI2_FS_B | - | OTG_HS_ULPI_STP | - | FMC_SDNWE | - | - | EVENTOUT |
| | PC1 | TRACED0 | - | - | | - | SPI2_MOSI/I2S2_SD | SAI1_SD_A | - | - | - | - | ETH_MDC | MDIOS_MDC | - | - | EVENTOUT |
| | PC2 | - | - | - | | - | SPI2_MISO | | - | - | - | OTG_HS_ULPI_DIR | ETH_MII_TXD2 | FMC_SDNE0 | - | - | EVENTOUT |
| | PC3 | - | - | - | | - | SPI2_MOSI/I2S2_SD | - | - | - | - | OTG_HS_ULPI_NXT | ETH_MII_TX_CLK | FMC_SDCKE0 | - | - | EVENTOUT |
| | PC4 | - | - | - | | - | I2S1_MCK | - | - | - | - | - | ETH_MII_RXD0/ETH_R | FMC_SDNE0 | - | - | EVENTOUT |

| PORT | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMMC1/MDIOS/OTG2_FS | - | - | SYS |
| | | | | | | | | | | | | MII_RXD0 | | | | |
| PC5 | - | - | - | | - | - | - | - | - | - | - | ETH_MII_RXD1/ETH_RMII_RXD1 | FMC_SDCKE0 | COMP0_OUT | - | EVENTOUT |
| PC6 | - | - | TIM3_CH1 | TIM8_CH1 | - | I2S2_MCK | - | - | USART6_TX | FMC_NWAIT | SDMMC2_D6 | - | SDMMC1_D6 | - | - | EVENTOUT |
| PC7 | - | - | TIM3_CH2 | TIM8_CH2 | - | - | I2S3_MCK | - | USART6_RX | FMC_NE1 | SDMMC2_D7 | - | SDMMC1_D7 | - | - | EVENTOUT |
| PC8 | TRACED1 | - | TIM3_CH3 | TIM8_CH3 | - | - | - | UART5_RTS | USART6_CK | FMC_NE2/FMC_NCE | - | - | SDMMC1_D0 | - | - | EVENTOUT |
| PC9 | MCO2 | - | TIM3_CH4 | TIM8_CH4 | I2C3_SDA | I2S_CKIN | - | UART5_CTS | - | QUADSPI_B | - | - | SDMMC1_D1 | - | - | EVENTOUT |

| PORT | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMMC1/MDIOS/OTG2_FS | - | - | SYS |
| | | | | | | | | | | K1_IO0 | | | | | | |
| PC10 | - | - | - | - | - | - | SPI3_SCK/I2S3_CK | USART3_TX | UART4_TX | QUADSPI_BK1_IO1 | - | - | SDMMC1_D2 | - | - | EVENTOUT |
| PC11 | - | - | - | - | - | - | SPI3_MISO | USART3_RX | UART4_RX | QUADSPI_BK2_NCS | - | - | SDMMC1_D3 | - | - | EVENTOUT |
| PC12 | TRACED3 | - | - | - | - | - | SPI3_MOSI/I2S3_SD | USART3_CK | UART5_TX | - | - | - | SDMMC1_CK | - | - | EVENTOUT |
| PC13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| PC14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMC1/MDIOS/OTG2_FS | - | - | SYS |
| | PC15 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| PD | PD0 | - | - | - | - | - | - | - | - | UART4_RX | CAN1_RX | - | - | FMC_D2 | - | - | EVENTOUT |
| | PD1 | - | - | - | - | - | - | - | - | UART4_TX | CAN1_TX | - | - | FMC_D3 | - | - | EVENTOUT |
| | PD2 | TRACED2 | - | TIM3_ETR | - | - | - | - | - | UART5_RX | - | - | - | SDMMC1_CMD | - | - | EVENTOUT |
| | PD3 | - | - | - | - | - | SPI2_SCK/I2S2_CK | - | USART2_CTS | - | - | - | - | FMC_CLK | - | - | EVENTOUT |
| | PD4 | - | - | - | - | - | - | - | USART2_RTS | - | - | - | - | FMC_NOE | - | - | EVENTOUT |
| | PD5 | - | - | - | - | - | - | - | USART2_TX | - | - | - | - | FMC_NWE | - | - | EVENTOUT |

| PORT | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMC1/MDIOS/OTG2_FS | - | - | SYS |
| PD6 | - | - | - | - | - | SPI3_MOSI/I2S3_SD | SAI1_SD_A | USART2_RX | - | - | - | SDMMC2_CK | FMC_NWAIT | - | - | EVENTOUT |
| PD7 | - | - | - | - | - | SPI1_MOSI/I2S1_SD | - | USART2_CK | - | - | - | SDMMC2_CMD | FMC_NE1 | - | - | EVENTOUT |
| PD8 | - | - | - | - | - | - | - | USART3_TX | - | - | - | - | FMC_D13 | - | - | EVENTOUT |
| PD9 | - | - | - | - | - | - | - | USART3_RX | - | - | - | - | FMC_D14 | - | - | EVENTOUT |
| PD10 | - | - | - | - | - | - | - | USART3_CK | - | - | - | - | FMC_D15 | - | - | EVENTOUT |
| PD11 | - | - | - | - | I2C4_SMBA | - | - | USART3_CTS | - | QUADSPI_BK1_IO0 | SAI2_SD_A | - | FMC_A16/FMC_CLE | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMMC1/MDIOS/OTG2_FS | - | - | SYS |
| | PD12 | - | - | TIM4_CH1 | LPTIM1_IN1 | I2C4_SCL | - | - | USART3_RTS | - | QUADSPI_BK1_IO1 | SAI2_FS_A | - | FMC_A17/FMC_ALE | - | - | EVENTOUT |
| | PD13 | - | - | TIM4_CH2 | LPTIM1_OUT | I2C4_SDA | - | - | - | - | QUADSPI_BK1_IO3 | SAI2_SCK_A | - | FMC_A18 | - | - | EVENTOUT |
| | PD14 | - | - | TIM4_CH3 | - | - | - | - | - | UART8_CTS | - | - | - | FMC_D0 | - | - | EVENTOUT |
| | PD15 | - | - | TIM4_CH4 | - | - | - | - | - | UART8_RTS | - | - | - | FMC_D1 | - | - | EVENTOUT |
| PE | PE0 | - | - | TIM4_ETR | LPTIM1_ETR | - | - | - | - | UART8_RX | - | SAI2_MCLK_A | - | FMC_NBL0 | - | - | EVENTOUT |
| | PE1 | - | - | - | LPTIM1_IN2 | - | - | - | - | UART8_TX | - | - | - | FMC_NBL1 | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMC1/MDIOS/OTG2_FS | - | - | SYS |
| | PE2 | TRACECLK | - | - | - | - | SPI4_SCK | SAI1_MCLK_A | - | - | QUADSPI_BK1_IO2 | - | ETH_MII_TXD3 | FMC_A23 | - | - | EVENTOUT |
| | PE3 | TRACED0 | - | - | - | - | - | SAI1_SD_B | - | - | - | - | - | FMC_A19 | - | - | EVENTOUT |
| | PE4 | TRACED1 | - | - | - | - | SPI4_NSS | SAI1_FS_A | - | - | - | - | - | FMC_A20 | - | - | EVENTOUT |
| | PE5 | TRACED2 | - | - | TIM9_CH1 | - | SPI4_MISO | SAI1_SCK_A | - | - | - | - | - | FMC_A21 | - | - | EVENTOUT |
| | PE6 | TRACED3 | TIM1_BKIN2_COMP1_OUT | - | TIM9_CH2 | - | SPI4_MOSI | SAI1_SD_A | - | - | - | SAI2_MCLK_B | - | FMC_A22 | - | - | EVENTOUT |
| | PE7 | - | TIM1_ETR | - | - | - | - | - | - | UART7_RX | - | QUADSPI_B | - | FMC_D4 | - | - | EVENTOUT |

| PORT | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMC1/MDIOS/OTG2_FS | - | - | SYS |
| | | | | | | | | | | | K2_IO0 | | | | | |
| PE8 | - | TIM1_CH1N | - | - | - | - | - | - | UART7_TX | - | QUADSPI_BK2_IO1 | - | FMC_D5 | COMP2_OUT | - | EVENTOUT |
| PE9 | - | TIM1_CH1 | - | - | - | - | - | - | UART7_RTS | - | QUADSPI_BK2_IO2 | - | FMC_D6 | - | - | EVENTOUT |
| PE10 | - | TIM1_CH2N | - | - | - | - | - | - | UART7_CTS | - | QUADSPI_BK2_IO3 | - | FMC_D7 | - | - | EVENTOUT |
| PE11 | - | TIM1_CH2 | - | - | - | SPI4_NSS | - | - | - | - | SAI2_SD_B | - | FMC_D8 | - | - | EVENTOUT |
| PE12 | - | TIM1_CH3N | - | - | - | SPI4_SCK | - | - | - | - | SAI2_SCK_B | - | FMC_D9 | COMP1_OUT | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMC1/MDIOS/OTG2_FS | - | - | SYS |
| | PE13 | - | TIM1_CH3 | - | - | - | SPI4_MISO | - | - | - | - | SAI2_FS_B | - | FMC_D10 | COMP3_OUT | - | EVENTOUT |
| | PE14 | - | TIM1_CH4 | - | - | - | SPI4_MOSI | - | - | - | - | SAI2_MCLK_B | - | FMC_D11 | - | - | EVENTOUT |
| | PE15 | - | TIM1_BKIN_COMP0_OUT | - | - | - | - | - | - | - | - | - | - | FMC_D12 | - | - | EVENTOUT |
| PF | PF0 | - | - | - | - | I2C2_SDA | - | - | - | - | - | - | - | FMC_A0 | - | - | EVENTOUT |
| | PF1 | - | - | - | - | I2C2_SCL | - | - | - | - | - | - | - | FMC_A1 | - | - | EVENTOUT |
| | PF2 | - | - | - | - | I2C2_SMBA | - | - | - | - | - | - | - | FMC_A2 | - | - | EVENTOUT |
| | PF3 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A3 | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMC1/MDIOS/OTG2_FS | - | - | SYS |
| | PF4 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A4 | - | - | EVENTOUT |
| | PF5 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A5 | - | - | EVENTOUT |
| | PF6 | - | - | - | TIM10_CH1 | - | SPI5_NSS | SAI1_SD_B | - | UART7_RX | QUADSPI_BK1_IO3 | - | - | - | - | - | EVENTOUT |
| | PF7 | - | - | - | TIM11_CH1 | - | SPI5_SCK | SAI1_MCLK_B | - | UART7_TX | QUADSPI_BK1_IO2 | - | - | - | - | - | EVENTOUT |
| | PF8 | - | - | - | - | - | SPI5_MISO | SAI1_SCK_B | - | UART7_RTS | TIM13_CH1 | QUADSPI_BK1_IO0 | - | - | - | - | EVENTOUT |
| | PF9 | - | - | - | - | - | SPI5_MOSI | SAI1_FS_B | - | UART7_CTS | TIM14_CH1 | QUADSPI_B | - | - | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMC1/MDIOS/OTG2_FS | - | - | SYS |
| | | | | | | | | | | | | K1_IO1 | | | | | |
| | PF10 | - | - | - | - | - | - | - | - | - | QUADSPI_CLK | - | - | - | - | - | EVENTOUT |
| | PF11 | - | - | - | - | - | SPI5_MOSI | - | - | - | - | SAI2_SD_B | - | FMC_SDNRAS | - | - | EVENTOUT |
| | PF12 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A6 | - | - | EVENTOUT |
| | PF13 | - | - | - | - | I2C4_SMBA | - | - | - | - | - | - | - | FMC_A7 | - | - | EVENTOUT |
| | PF14 | - | - | - | - | I2C4_SCL | - | - | - | - | - | - | - | FMC_A8 | - | - | EVENTOUT |
| | PF15 | - | - | - | - | I2C4_SDA | - | - | - | - | - | - | - | FMC_A9 | - | - | EVENTOUT |
| PG | PG0 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A10 | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMMC1/MDIOS/OTG2_FS | - | - | SYS |
| | PG1 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A11 | - | - | EVENTOUT |
| | PG2 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A12 | - | - | EVENTOUT |
| | PG3 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A13 | - | - | EVENTOUT |
| | PG4 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A14/FMC_BA0 | - | - | EVENTOUT |
| | PG5 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A15/FMC_BA1 | - | - | EVENTOUT |
| | PG6 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_NE3 | - | - | EVENTOUT |

| PORT | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMMC1/MDIOS/OTG2_FS | - | - | SYS |
| PG7 | - | - | - | - | - | - | SAI1_MCLK_A | - | USART6_CK | - | - | - | FMC_INT | - | - | EVENTOUT |
| PG8 | - | - | - | - | - | SPI6_NSS | - | - | USART6_RTS | - | - | ETH_PPS_OUT | FMC_SDCLK | - | - | EVENTOUT |
| PG9 | - | - | - | - | - | SPI1_MISO | - | - | USART6_RX | QUADSPI_BK2_IO2 | SAI2_FS_B | SDMMC2_D0 | FMC_NE2/FMC_NCE | - | - | EVENTOUT |
| PG10 | - | - | - | - | - | SPI1_NSS/I2S1_WS | - | - | - | - | SAI2_SD_B | SDMMC2_D1 | FMC_NE3 | - | - | EVENTOUT |
| PG11 | - | - | - | - | - | SPI1_SCK/I2S1_CK | - | - | - | - | SDMMC2_D2 | ETH_MII_TX_EN/ETH_R | - | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMC1/MDIOS/OTG2_FS | - | - | SYS |
| | | | | | | | | | | | | | MII_TX_EN | | | | |
| | PG12 | - | - | - | LPTIM1_IN1 | - | SPI6_MISO | - | | USART6_RTS | - | - | SDMMC2_D3 | FMC_NE4 | - | - | EVENTOUT |
| | PG13 | TRACED0 | - | - | LPTIM1_OUT | - | SPI6_SCK | - | - | USART6_CTS | - | - | ETH_MII_TXD0/ETH_RMII_TXD0 | FMC_A24 | - | - | EVENTOUT |
| | PG14 | TRACED1 | - | - | LPTIM1_ETR | - | SPI6_MOSI | - | - | USART6_TX | QUADSPI_BK2_IO3 | - | ETH_MII_TXD1/ETH_RMII_TXD1 | FMC_A25 | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMC1/MDIOS/OTG2_FS | - | - | SYS |
| | PG15 | - | - | - | - | - | - | - | - | USART6_CTS | - | - | - | FMC_SDNCAS | - | - | EVENTOUT |
| PH | PH0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PH1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PH2 | - | - | - | LPTIM1_IN2 | - | - | - | - | - | QUADSPI_BK2_IO0 | SAI2_SCK_B | ETH_MII_CRS | FMC_SDCKE0 | - | - | EVENTOUT |
| | PH3 | - | - | - | - | - | - | - | - | - | QUADSPI_BK2_IO1 | SAI2_MCLK_B | ETH_MII_COL | FMC_SDNE0 | - | - | EVENTOUT |
| | PH4 | - | - | - | - | I2C2_SCL | - | - | - | - | - | OTG_HS_ULPI_NXT | - | - | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMC1/MDIOS/OTG2_FS | - | - | SYS |
| | PH5 | - | - | - | - | I2C2_SDA | SPI5_NSS | - | - | - | - | - | - | FMC_SDNWE | - | - | EVENTOUT |
| | PH6 | - | - | - | - | I2C2_SMBA | SPI5_SCK | - | - | - | TIM12_CH1 | - | ETH_MII_RXD2 | FMC_SDNE1 | - | - | EVENTOUT |
| | PH7 | - | - | - | - | I2C3_SCL | SPI5_MISO | - | - | - | - | - | ETH_MII_RXD3 | FMC_SDCKE1 | - | - | EVENTOUT |
| | PH8 | - | - | - | - | I2C3_SDA | - | - | - | - | - | - | - | FMC_D16 | - | - | EVENTOUT |
| | PH9 | - | - | - | - | I2C3_SMBA | - | - | - | - | TIM12_CH2 | - | - | FMC_D17 | - | - | EVENTOUT |
| | PH10 | - | - | TIM5_CH1 | - | I2C4_SMBA | - | - | - | - | - | - | - | FMC_D18 | - | - | EVENTOUT |
| | PH11 | - | - | TIM5_CH2 | - | I2C4_SCL | - | - | - | - | - | - | - | FMC_D19 | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMMC1/MDIOS/OTG2_FS | - | - | SYS |
| | PH12 | - | - | TIM5_CH3 | - | I2C4_SDA | - | - | - | - | - | - | - | FMC_D20 | - | - | EVENTOUT |
| | PH13 | - | - | - | TIM8_CH1N | - | - | - | - | UART4_TX | CAN1_TX | - | - | FMC_D21 | - | - | EVENTOUT |
| | PH14 | - | - | - | TIM8_CH2N | - | - | - | - | UART4_RX | CAN1_RX | - | - | FMC_D22 | - | - | EVENTOUT |
| | PH15 | - | - | - | TIM8_CH3N | - | - | - | - | - | - | - | - | FMC_D23 | - | - | EVENTOUT |
| PI | PI0 | - | - | TIM5_CH4 | - | - | SPI2_NSS/I2S2_WS | - | - | - | CAN4_TX | - | - | FMC_D24 | - | - | EVENTOUT |
| | PI1 | - | - | - | TIM8_BKIN2_COMP3_OUT | - | SPI2_SCK/I2S2_CK | - | - | - | CAN4_RX | - | - | FMC_D25 | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMMC1/MDIOS/OTG2_FS | - | - | SYS |
| | PI2 | - | - | - | TIM8_CH4 | - | SPI2_MISO | - | - | - | - | - | - | FMC_D26 | - | - | EVENTOUT |
| | PI3 | - | - | - | TIM8_ETR | - | SPI2_MOSI/I2S2_SD | - | - | - | - | - | - | FMC_D27 | - | - | EVENTOUT |
| | PI4 | - | - | - | TIM8_BKIN_COMP2_OUT | - | - | - | - | - | CAN5_TX | SAI2_MCLK_A | - | FMC_NBL2 | - | - | EVENTOUT |
| | PI5 | - | - | - | TIM8_CH1 | - | - | - | - | - | CAN5_RX | SAI2_SCK_A | - | FMC_NBL3 | - | - | EVENTOUT |
| | PI6 | - | - | - | TIM8_CH2 | - | - | - | - | - | - | SAI2_SD_A | - | FMC_D28 | - | - | EVENTOUT |
| | PI7 | - | - | - | TIM8_CH3 | - | - | - | - | - | - | SAI2_FS_A | - | FMC_D29 | - | - | EVENTOUT |

| PORT | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMMC1/MDIOS/OTG2_FS | - | - | SYS |
| PI8 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| PI9 | - | - | - | - | - | - | - | - | UART4_RX | CAN1_RX | - | - | FMC_D30 | - | - | EVENTOUT |
| PI10 | - | - | - | - | - | - | - | - | - | - | - | ETH_MII_RX_ER | FMC_D31 | - | - | EVENTOUT |
| PI11 | - | - | - | - | - | - | - | - | - | - | OTG_HS_ULPI_DIR | - | - | - | - | EVENTOUT |
| PI12 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| PI13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| PI14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMC1/MDIOS/OTG2_FS | - | - | SYS |
| | PI15 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| PJ | PJ0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PJ1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PJ2 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PJ3 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PJ4 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PJ5 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PJ6 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMC1/MDIOS/OTG2_FS | - | - | SYS |
| | PJ7 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PJ8 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PJ9 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PJ10 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PJ11 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PJ12 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PJ13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PJ14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMC1/MDIOS/OTG2_FS | - | - | SYS |
| | PJ15 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| PK | PK0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PK1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PK2 | | | | | | | | | | | | | | | - | EVENTOUT |
| | PK3 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PK4 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PK5 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PK6 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMMC1/MDIOS/OTG2_FS | - | - | SYS |
| | PK7 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |

# VI. Functional Description

## 6.1. CPU

BST32F7 series integrated 32-bit RISC processor operates at a frequency of 216MHz, supports single- and double-precision floating-point operations, and has excellent computing performance and low interrupt latency.

- Built-in 16KB instruction cache and 16KB data cache;
- 64-bit ITCM interface;
- Two 32-bit DTCM interfaces;
- Dedicated low-latency peripheral interface.

## 6.2. Memory Map

For detailed information on the memory map and address boundaries of all peripherals, refer to the BST32F7 Series Technical Reference Manual.

## 6.3. Memory Protection unit

The memory protection unit (MPU) is used to manage the CPU's access to the entire 4G address space, improving system security by preventing unauthorized access.

The MPU is usually managed by an RTOS (Real-Time Operating System), which can detect when a program accesses a memory location that is prohibited by the MPU. In an RTOS environment, the kernel can dynamically update the settings of the MPU area based on the executed process.

## 6.4. Embedded FLASH

The BST32F7 series products have built-in Flash memory up to 2MB for storing programs and data, with the following features:

- Single/dual bank operation mode, support read and write synchronization;
- Level 3 Read Protection (RDP):

  - level 0: no read protection;
  - level 1: no access to the flash memory (read, erase, write), backup SRAM is executed during debug functions, when booting from RAM or system memory bootloader;
  - level 2: Debug or chip read operations are prohibited.
- Write Protect (WRP): The protected area can be prevented from being erased and written.
- Dedicated code read protection.

### 6.5. CRC (Cyclic Redundancy Check) calculation unit

The CRC (Cyclic Redundancy Check) calculation unit generates a CRC code from a 32-bit data word using a polynomial generator of configurable value and size.

In many applications, CRC is often used to verify the integrity of data transmission or storage.

### 6.6. On-chip SRAM

All products have built-in:

- 512KB System SRAM:
  - SRAMH bus includes SRAM1: 368KB, SRAM2: 16KB;
  - DTCM-RAM: 128KB;
- ITCM-RAM 16KB:
  - ITCM-RAM is located in the TCM interface and is only retained when the CPU is executing/instructions are useful for critical real-time programs;
  - DTCM-RAM can be accessed by DMA, and ITCM-RAM only supports CPU access and 0 wait CPU clock.
  - 4KB backup SRAM

Supports CPU access only, supports write protection, and can retain data in Standby or VBAT mode.

### 6.7. Flexible Memory Controller (FMC)

The Flexible Memory Controller (FMC) includes three memory controllers:

- NOR/PSRAM Memory Controller;
- NAND memory controller;
- Synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) Controller.

The main features of the FMC controller include:

- Static memory mapped device interface:
  - Static Random Access Memory (SRAM);
  - NOR flash memory/OneNAND flash memory;
  - PSRAM (4 memory sticks);
  - NAND flash, up to 8KB of data can be checked with ECC hardware;
  - Synchronous DRAM memory interface (SRAM/Mobile LPSDR SDRAM);
  - 8, 16, 32-bit data bus width;
  - Each memory has independent chip select control;
  - Each memory can be configured independently;
  - Write FIFO;
  - Read FIFO for SDRAM controller;
  - The maximum synchronous access frequency of FMC_CLK/FMC_SDCLK is HCLK/2;

### 6.7. Direct Memory Access Controller (DMA)

The product has 2 general DMA controllers, each controller supports 8 data streams, each data stream can have up to 8 channels. Each data stream can manage the transfer from memory to memory, peripheral to memory, memory to peripheral, built-in dedicated FIFO

for connecting peripherals, support burst transfer, support circular buffer, double buffer, no program code control is required when using it.

Each data stream can be configured by software hardware DMA request or software trigger, and the amount of data transferred between the data source and the data destination is unlimited.

DMA-capable peripherals include: SPI, I2C, USART, general-purpose, basic and advanced control timers TIMx, DAC, SDIO, ADC

### 6.8. Nesting Vector Interrupt Controller (NVIC)

The product has a built-in nested vectored interrupt controller that can manage 16 priority levels and handles kernel support for maskable interrupt channels and 16 interrupt lines.

This hardware block provides flexible interrupt management capabilities with minimal interrupt latency.

### 6.9. External Interrupt/Event Controller (EXTI)

External interrupt (EXTI) and NVIC Direct connection, EXTI Include25 edge detectors for generating interrupt requests. Each interrupt line can be independently configured with its trigger event (rising edge, falling edge, or both edges) and can be individually masked.16Root can be fromGPIO, select Connect.

### 6.10. Clock

At power-on reset, the core first uses the 16MHz internal HSI RC oscillator as the default clock, which is calibrated according to industrial standards to provide 2% accuracy. Then, the user can select the RC oscillator or external 4-26 MHz clock source as the system clock through register configuration, and can monitor the clock status. When a clock failure is detected, it automatically switches to the internal RC oscillator and generates a software interrupt (if enabled).

The clock source can be multiplied to 216MHz by PLL inside the chip, and the PLL clock can also be monitored and interrupted.

### 6.11. Startup Mode

The boot mode can be selected through the BOOT pin and BOOT_ADDx, supporting a programming range of 0x0000 0000 to 0x3FFF FFFF, and can be selected from the following three modes:

- Boot from the chip's internal FLASH;
- Boot from internal SRAM;
- Booting from the boot code area;

## VII. Power Solution

### 7.1. Power supply solution

- $V_{DD}$= 2.1～3.6V: pass VDD Pins are GPIO Pins and internal modules such as voltage regulator (LDO)powered by VDDA = 2.1～3.6 V:pass VDDA Pins are ADC and DAC powered by VDDA and VSSA Must be with VDD and VSS E qui potential;
- VBAT =2.0 ~3.6 V: VBAT pin allows the device to be powered from an external battery, external super capacitor VBAT When there is no external battery or external super capacitor, VDD When there is no VDD When it exists, VBAT pin (through an internal power switch) isRTC,external32 kHz Crystal Oscillator (LEXT) and the battery supply register (BPR)powered by;

### 7.2. Reset

This product integrates power-on reset (POR) and low voltage reset (LVR) circuit, which is always in working state, so that the device can2.1VWhen working; VDD When the voltage

drops below a set threshold, the device can be placed in reset without the need for external reset circuitry.

### 7.2. Power supply monitoring

Products that include the PDR_ON PIN can DR_ON The internal power monitor is enabled by setting the PDR_ON PIN to high. Products that do not include the PDR_ON PIN keep the power monitor enabled after power-on.

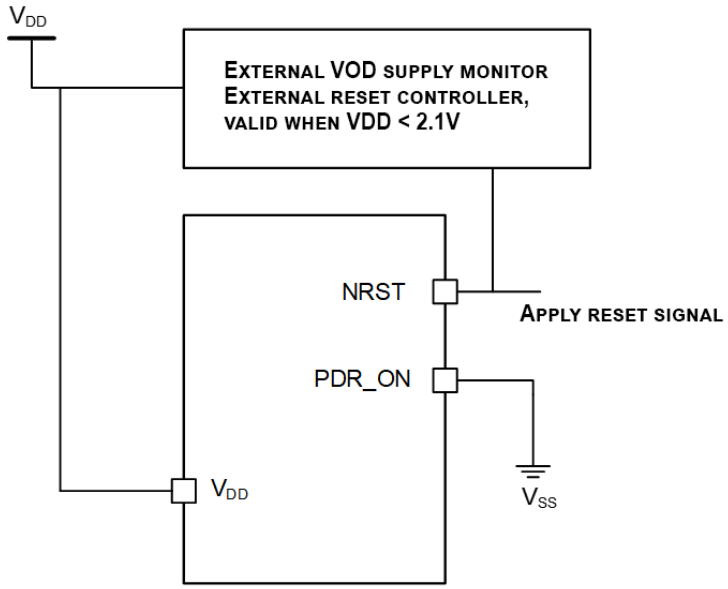
All products integrate a power-on reset (POR)/power-down reset (PDR) circuit and are coupled with a brown-out reset (BOR) circuit. When powered on, the POR/PDR is activated to ensure that the operating voltage of the MCU is above 2.1v. When the threshold level of the 2.1v POR is reached, the register configuration is loaded, and the default BOR threshold is confirmed or modified according to the user settings, or the BOR is turned off. Three BOR thresholds can be set through the corresponding registers. When VDD is lower than the specified threshold VPOR/PDR or VBOR, the product will remain in reset mode without an external reset circuit.

The product also has an embedded programmable voltage detector (PVD), which can be turned off or enabled by the application program, which can be used to monitor the VDD/VDDA supply. When VDD/VDDA is lower than the VPVD threshold and/or VDD/VDDA is higher than the VPVD threshold, an interrupt will be generated. Subsequently, the interrupt service routine will generate a warning message and/or put the MCU into a safe state.

### 7.3. Products packaged with PDR_ON PIN support the following functions:

- Internal Power-On Reset (POR)/Power-Down Reset (PDR) circuit can be disabled via PDR_ON PIN
- When PDR_ON is connected to VSS, an external reset circuit must be used to hold the device in reset when VDD < 2.1 V.picture3-1 When VDD is below the

threshold voltage (such as picture 3-1 Use PDR_ON to turn off the internal reset circuit and use external reset) must remain in the reset state.




Picture 3-1. Use PDR_ON to turn off the internal reset circuit and use external reset

### 7.4. Internal voltage regulator (LDO)

The internal LDO has three operating modes:

- MR Mode.

MR mode is used in normal mode (default mode), overdrive mode (enabled by software), or stop mode. Different voltage levels are provided to achieve the best balance between maximum frequency and dynamic power consumption. For a given voltage level, overdrive mode can operate at a higher frequency than normal mode.

During stop mode, MR has two configurations:

- MR works in normal mode (MR's default mode in stop mode),
- MR works in low load mode (reduced leakage current mode)
- LPR mode.

When entering stop mode, the LP regulator mode is configured by software. Similar to MR mode, there are two configurations of LPR during stop mode:

- LPR works in normal mode (default mode when LPR is ON),
- LPR works in low load mode (reduced leakage current mode)
- Power-down.

The power-down function can be activated only when entering the standby mode. At this time, the voltage regulator outputs high impedance, the core circuit is powered off, and zero power consumption is achieved. The register and SRAM contents are lost.

Table 3-1 It explains the operating modes that the voltage regulator can support in different operating modes of the chip.

Note that two 2.2μF capacitors with an equivalent series resistance (ESR) < 2Ω should be connected to the VCAP_1 and VCAP_2 pins (or a 4.7μF capacitor with an equivalent series resistance (ESR) between 0.1-0.2Ω when only the VCAP_1 pin is provided (LQFP64 package)).

Table .3-1.Regulator Configuration Modes and Device Operating Modes

| VOLTAGE REGULATOR CONFIGURATION | RUN MODEL | SLEEP MODEL | STOP MODEL | STANDBY MODEL |
|---|---|---|---|---|
| Ordinary model | MR | MR | MR or LPR | - |
| Overload model | MR | MR | - | - |
| Underactuated model | - | - | MR or LPR | - |
| Power off model | - | - | - | Yes |

- "-" means the corresponding configuration is not available

### 7.5. Low Power Mode

The product supports three low-power modes to achieve the best balance between low power consumption, short startup time and available wake-up sources:

**Sleep Mode**

- In sleep mode, only the CPU stops working, all peripherals continue to operate and can be interrupted/event
- **Stop Mode**

  The shutdown mode can achieve the lowest power consumption while maintaining the contents of SRAM and registers.

  All clocks will stop, including PLL, HSI RC and HSE.

  In stop mode, the regulator can operate in MR or LPR mode andTable 3-3Configuration:

  - Normal mode (default mode when MR or LPR is enabled)
  - Under-drive mode

In Stop mode, the chip can be awakened by EXTI, which can be any of 16 external interrupt sources, PVD output, RTC alarm/wakeup/timestamp event, USB OTG FS/HS wakeup.

Table 3-2. Regulator Mode in Stop Mode

| VOLTAGE REGULATOR CONFIGURATION | HOST VOLTAGE REGULATOR (MR) | LOW POWER REGULATOR (LPR) |
|---|---|---|
| Ordinary model | MR ON | LPR ON |
| Low load model | Low load Mode MR | Low load Mode LPR |

- **Standby mode**

  The standby mode is designed to provide the user with the lowest power consumption, therefore, the internal voltage regulator is turned off and the 1.2V voltage domain

  The power supply will be stopped. The PLL, HSI RC and HSE crystal oscillators will also be turned off. After entering standby mode, the contents of the SRAM and

registers will be lost except for the registers in the selected backup domain and backup SRAM.

The chip can exit standby mode by an external reset (NRST pin), an IWDG reset, a rising or falling edge on the WKUP pin (PA0, PA2, PC1, PC13, PI8, PI11), or an RTC alarm/wake-up/timestamp event.

### 7.6. VBAT Operation

When VDD is not powered, the chip can power the VBAT domain from an external battery or supercapacitor through the VBAT pin, including: RTC, backup registers, and backup SRAM can all be powered by VBAT.

Note:

- When the chip is powered from VBAT, external interrupts and RTC alarms/events will not exit it from VBAT operating mode.
- When the PDR_ON pin is connected to VDD, the switching between VDD and VBAT power supplies will cause the backup domain to reset. To avoid the power reset causing the backup domain to reset, we need to connect PDR_ON to VSS and use an external reset circuit to keep the device in reset state when VDD<2.1v.

## VIII. Real-time clock (RTC), Backup SRAM, backup registers BKR

The real-time clock (RTC) is a counter that stores time information in BCD format. It records specific calendar times from 00 to 99. It supports both 12/24 hour time systems and automatically calculates the days 28, 29 (leap year), 30 and 31 according to the month and year.

RTC and Backup SRAM, backup The register (BPR) is powered through a switch that selects VDD power when VDD is valid, otherwise it is powered by the VBAT pin. When the

PDR_ON pin is connected to Vss, RTC and Backup SRAM, The registers are not reset by system or power reset sources; nor are they reset when waking up from standby mode.

### 8.1. Timer and Watchdog

The chip includes 2 advanced control timers, 10 general timers, 2 basic timers, and 2 watchdog timers. Table 3-3 The features of the advanced control timer, general purpose timer, and basic timer are compared.

Table 3-1. Timing comparison of the characteristics

| TIMER TYPE | TIMER | COUNTER RESOLUTI | COUNTER TYPE | PRESCALER FACTOR | DMA REQUEST | CAPTURE/ COMPARE CHANNEL | COMPLE MENTARY OUTPUT | MAXIMUM INTERFAC E CLOCK (MHZ) | MAXIMUM TIMER CLOCK (MHZ) |
|---|---|---|---|---|---|---|---|---|---|
| Advanced Control | TIM1<br>TIM8 | 16-bit | Increment, decrement, increment/ decrement | Any integer between 1 and 65536 | have | 4 | have | 108 | 180 |
| General | TIM2<br>TIM5 | 32-bit | Increment, decrement, increment/ decrement | Any integer between 1 and 65536 | have | 4 | none | 54 | 108 |
| | TIM3<br>TIM4 | 16-bit | Increment, decrement, increment/ decrement | Any integer between 1 and 65536 | have | 4 | none | 54 | 108 |
| | TIM9 | 16-bit | Increment | Any integer between 1 and 65536 | none | 2 | none | 108 | 180 |
| | TIM10<br>TIM11 | 16-bit | Increment | Any integer between 1 and 65536 | none | 1 | none | 108 | 180 |
| | TIM12 | 16-bit | Increment | Any integer between 1 and 65536 | none | 2 | none | 54 | 108 |
| | TIM13<br>TIM14 | 16-bit | Increment | Any integer between 1 and 65536 | none | 1 | none | 54 | 108 |

| TIMER TYPE | TIMER | COUNTER RESOLUTI | COUNTER TYPE | PRESCALER FACTOR | DMA REQUEST | CAPTURE/ COMPARE CHANNEL | COMPLE MENTARY OUTPUT | MAXIMUM INTERFAC E CLOCK (MHZ) | MAXIMUM TIMER CLOCK (MHZ) |
|---|---|---|---|---|---|---|---|---|---|
| Basics | TIM6 TIM7 | 16-bit | Increment | Any integer between 1 and 65536 | have | 0 | none | 54 | 108 |

- Depending on the configuration of the TIMPRE bits in the RCC_DCKCFGR register, the maximum timer clock can be 108MHz or 216MHz.

### 8.1.1 Advanced control timer (TIM1, TIM8)

The advanced control timers (TIM1, TIM8) can be viewed as three-phase PWM generators multiplexed on six channels. They have complementary PWM outputs with programmable dead-time insertion and can also be used as complete general-purpose timers.

4 independent channels can be used for:

- Input Capture
- Output Compare
- PWM generation (edge or center-aligned mode)
- Single pulse mode output

If configured as a standard 16-bit timer, the functionality is the same as the generic TIMx timers. If configured as a 16-bit PWM generator, it has full modulation capability (0-100%).

Advanced control timers can work with TIMx timers through the timer link function to provide synchronization or event linking capabilities.

TIM1 and TIM8 support the generation of independent DMA requests.

### 8.1.2. General purpose timer (TIMx)

The chip has 10 built-in synchronous general-purpose timers (see Table 3-3 to understand the difference).

- TIM2, TIM3, TIM4, and TIM5

The BST32F7 series includes 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, TIM4. The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. They all have 4 independent channels for input capture/output comparison, PWM, and single pulse mode output. In the largest package, up to 16 input capture/output comparison/PWM are available.

The TIM2, TIM3, TIM4, and TIM5 general-purpose timers can work together or with other general-purpose timers and the advanced control timers TIM1 and TIM8 through the timer chaining feature to achieve synchronization or event chaining.

Any general purpose timer can be used to generate PWM output.

TIM2, TIM3, TIM4, TIM5 can generate independent DMA requests. They can process quadrature (incremental) encoder signals and can also process the digital outputs of 1 to 4 Hall effect sensors.

- TIM9, TIM10, TIM11, TIM12, TIM13, TIM14

  These timers are based on a 16-bit auto-reload up-counter and a 16-bit prescaler. TIM10, TIM11, TIM13, TIM14 have one independent channel, while TIM9 and TIM12 have two independent channels for input capture/output compare, PWM, single pulse mode output. They can be synchronized with TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as a simple time base.

### 8.1.3. Basic timers TIM6 and TIM7

These timers are primarily used to generate DAC trigger signals and waveforms, but can also be used as a general-purpose 16-bit time base.

TIM6 and TIM7 support the generation of independent DMA requests.

### 8.1.4. Independent watchdog

The independent watchdog is based on a 12-bit down counter and an 8-bit prescaler. It is clocked by an independent 32 kHz internal RC, and since the internal RC is independent of the main clock, it can work in stop and standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free-running timer to provide timeout management for the application. It can be configured by hardware or software through the option byte.

### 8.1.5. Window Watchdog

The window watchdog is based on a 7-bit down counter that can be set to free-run. It can be used as a watchdog to reset the device if a problem occurs. It is driven by the main clock. There is an early warning interrupt function and the counter can be frozen in debug mode.

### 8.1.6. SysTick Timer

This timer is designed for use in real-time operating systems, but can also be used as a standard down counter. It has the following features:

- 24-bit down counter
- Automatic reload function
- When the counter reaches 0, a maskable system interrupt is generated
- Programmable clock source

## 8.2. Inter-Integrated Circuit Interface (I2C)

There are 4 I2Cs embedded in the device, which can be referred toTable 3-4To understand its functionality.

The I2C bus interface handles the communication between the chip and the I2C bus, controlling the timing, protocol, and arbitration of the I2C bus.

The chip's I2C peripherals meet the following characteristics:

- Compatible with I2C bus specifications:
- Master-slave mode, allowing multiple hosts.
- Standard mode (Sm) with a maximum bit rate of 100 kb/s
- Fast mode (Fm) with a maximum bit rate of 400 kb/s
- Fast-mode+ (Fm+) with up to 1Mb/s bit rate and 20mA output drive IO
- 7-bit and 10-bit addressing modes, allowing multiple 7-bit slave addresses
- Programmable setup and hold times
- Optional clock stretching
- Compatible with SMBUS 2.0 specification
- Hardware PEC (Packet Error Check) generation and acknowledgement with ACK control
- Support Address Resolution Protocol (ARP)
- SMBus Alerts
- Compatible with Power System Management Bus Protocol Rev1.1
- Independent clock: You can select an independent clock source, which is the I2C communication speed and PCLK reprogrammable
- Programmable analog and digital noise filters
- 1-byte buffer with DMA support

Table 3-2. I2C Implementation

| I2C FEATURES (1) | I2C1~I2C4 |
|---|---|
| Standard mode (up to 100 kbit/s) | X |
| Fast mode (up to 100 kbit/s) | X |
| Fast-mode+ with 20mA output drive I/O (up to 1Mbit/s) | X |
| Programmable analog and digital noise filters | X |
| SMBus/PMBus Hardware Support | X |
| Independent clock | X |

- X：Supported.

### 8.3. Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The device has built-in USART, and its performance can be referenced Table 3-5.

The universal synchronous/asynchronous receiver/transmitter provides a flexible full-duplex data exchange mode and can exchange data with external devices that comply with the NRZ standard.

USART peripheral support:

- Full-duplex asynchronous communication
- Configurable 16- or 8-times oversampling provides flexibility in data and clock tolerances.
- Dual clock domains, convenient baud rate programming, independent of PCLK reprogramming.
- Automatic baud rate detection
- Programmable data word length (7/8/9 bits)
- Programmable MSB-first or LSB-first shift data order
- Programmable parity (odd, even or no parity)
- Configurable stop bits (1, 1.5 or 2 stop bits)

- Output clock for synchronous communication in synchronous mode
- Single-line half-duplex communication
- Individual signal polarity controls for transmit and receive
- Tx/Rx pin configurations are swappable
- Hardware flow control for modems and RS-485 transceivers
- Multiprocessor Communication
- LIN master mode synchronous break transmission function and LIN slave mode break detection function
- Support ModBus communication

Table 3-3. USART Implementation

| FEATURES(1) | USART1/2/3/6 | UART4/5/7 |
|---|---|---|
| Single-line half-duplex communication | X | X |
| LIN Mode | X | X |
| Dual clock domains | X | X |
| Receiver timeout interrupt | X | X |
| Modbus Communication | X | X |
| Automatic baud rate detection | X | X |
| Drive enable | X | X |
| Synchronous Mode | X | - |

- X = Support.

### 8.4. Serial Peripheral Interface (SPI)

The chip has 6 SPIs, supporting master-slave mode, full-duplex and simplex communication modes with a communication rate of up to 25Mbit/s. The 3-bit prescaler can generate 8 master mode frequencies, the frame can be configured to 4-16 bits, and all SPIs can use the DMA controller.

- When SPI acts as a slave and only receives, it can operate at a frequency of 54M.
- When SPI is a slave receiving and transmitting, it can work at 37M
- When SPI is a slave device that only transmits, it can operate at a frequency of 37M.
- SPI is used as the host. If it only transmits and does not care whether the received data is correct, it can work at 40M.
- SPI is used as the host. If it needs to receive while transmitting, and ensure that the received and transmitted data are correct, the maximum operating frequency is 30M.

### 8.4. Secure Digital Input interface (SDMMC)

The product provides an SD/SDIO/MMC host interface that supports three different data bus modes in MultiMedia Card System Specification Version 4.2: 1-bit (default), 4-bit, and 8-bit.

The interface has a data transfer rate of up to 50MHz and complies with the SD Memory Card Specification Version 2.0.

The interface also supports two different data bus modes in the SDMMC Card Specification Version 2.0: 1-bit (default) and 4-bit.

The current version supports only one SD/SDMMC/MMC4.2 card at a time, but supports multiple MMC4.1 or earlier cards.

The SDMMC can use the DMA controller.

### 8.5. Controller Area Network (CAN)

Supports up to 3 CANs compatible with 2.0A and B (active) specifications, with a bit rate of up to 1 Mbit/s. They can receive and send standard frames with 11-bit identifiers and extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two

receive FIFOs, with 3 levels and 28 shared adjustable filter groups (even if only one CAN is used, all resources can be used), CAN1, CAN2 are equipped with 256 bytes of SRAM, and CAN3 is equipped with 512 bytes of SRAM.

### 8.6. Universal Serial Bus on-the-go full speed (OTG_FS)

The chip has a built-in USB OTG full-speed device/host/OTG peripheral with an integrated transceiver. The USB OTG FS peripheral is compatible with the USB 2.0 specification and the OTG 2.0 specification, has software-configurable endpoint settings, and supports suspend/resume functions. The USB OTG controller requires a dedicated 48MHz clock generated by a PLL connected to the HSE oscillator. When operating in OTG/host mode, a power switch is required when the bus is connected to a device.

The main features are:

- Combined Rx and Tx FIFO size of 4KB with dynamic FIFO size
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
- 1 bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- 12 host channels, support periodic OUT
- Software configurable operation mode: OTG1.3 and OTG2.0
- Supports USB 2.0 LPM (Link Power Management)
- Support built-in FS OTG PHY
- Built-in HNP/SNP/IP (does not require any external resistors)
- Supports charging port detection as described in Battery Charging Specification Version 1.2

### 8.7. Universal Serial Bus on-the-go High Speed (OTG_HS)

The chip has a built-in peripheral that supports USB OTG high-speed device (up to 480 Mb/s)/host/OTG, supporting full-speed and high-speed operation. The integrated transceiver is used for full-speed operation (12 MB/s), and the UTMI pin-less interface

(ULPI) is used for high-speed operation (480 MB/s). When using USB OTG HS in HS mode, an external PHY device is required to connect to ULPI.

The USB OTG HS peripheral is compatible with the USB 2.0 specification and the OTG 2.0 specification. It has software configurable endpoint settings and supports suspend/resume functionality. The USB OTG controller requires a dedicated 48 MHz clock generated by a PLL connected to the HSE oscillator.

- When working in OTG/host mode, the bus needs a power switch when connecting to the device

The main features are:

- Combined Rx and Tx FIFO size of 4KB with dynamic FIFO size.
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels, support periodic OUT
- Software configurable operation mode: OTG1.3 and OTG2.0
- Supports USB 2.0 LPM (Link Power Management)
- Built-in USB DMA
- Built-in HNP/SNP/IP (does not require any external resistors)

### 8.8. Cryptographic Processor (CRYP)

With the help of encryption processor (CRYP), can be used DES, Triple-DES(3DES)or AES The algorithm encrypts the data and Decryption. The cryptographic processor is fully compliant with the following standards:

- Federal Information Processing Standards Publication (FIPS PUB 46-3,1999Year10American National Standards Institute(ANSI X9.52)Data Encryption Standard(DES)and3DES (TDES)

- Federal Information Processing Standards Publication (FIPS PUB 197,2001Year11Advanced Encryption Standard(AES)
- Supports multiple key sizes and chaining modes:
- AES Link Mode ECB/CBC/OFB/CTR, support128,192or256Bit Key size
- DES/TDES Link Mode EC Band CBC, support standard56bit keys (each with8bit parity check)

### 8.9. Hash Processor (HASH)

The hash processor is fully compatible with the Secure Hash Algorithm (SHA-1, SHA-224 and SHA-256), MD5 (Message Digest Algorithm 5) hash algorithms and suitable for a variety of applications HMAC (Keyed-Hash Message Authentication Code) hashing algorithm. HMAC The algorithm uses a hash function to authenticate the message. The algorithm requires two calls SHA-1, SHA-224, SHA-256 orMD5Hash function.(264−1)bits of the message, the hash processor computes the message digest (SHA-1 The algorithm is 160 bits, and the SHA-256 algorithm is 256 bits, SHA-224 algorithm is 224 The MD5 algorithm is 128 bits).

### 8.10. General Purpose Input /Output (GPIOs)

Each GPIO pin can be configured by software as an output (push-pull or open-drain, with or without pull-up/pull-down), input (floating, with or without pull-up/pull-down), or peripheral multiplexing function. Most GPIO pins have digital or analog multiplexing functions. All GPIOs have high current capabilities and have speed selection to better manage internal noise, power consumption, and electromagnetic radiation.

If desired, the I/O configuration can be locked after a specific sequence to avoid accidental writes to the I/O registers.

Except for DAC and USB multiplexed I/O, other I/Os support 5v-input tolerant.

### 8.11. Analog-to-Digital Converters (ADCs)

There are three built-in 12-bit analog-to-digital converters (ADCs), each of which can share up to 15 external channels and perform conversions in single-shot or scan mode. In scan mode, automatic conversions are performed on a selected group of analog inputs.

Other logic functions built into the ADC interface allow:

- Synchronous Sample and Hold

The ADC can use the DMA controller to very accurately monitor the conversion voltage of one, multiple or all selected channels using the analog watchdog function, and generate an interrupt when the conversion voltage exceeds the programmed threshold.

To synchronize the A/D conversion and the timer, the ADC can be triggered by any of the timers TIM1, TIM2, TIM3, TIM4, TIM5, and TIM8.

### 8.12. Temperature Sensor

The temperature sensor must produce a voltage that varies linearly with temperature. The conversion range is 2.0 V to 3.6 V. The temperature sensor is internally connected to the same input channel of VBAT, ADC1_IN18, which is used to convert the sensor output voltage to a digital value. When both the temperature sensor and VBAT conversion are enabled, only the VBAT conversion is performed.

Due to different processes, the offset of the temperature sensor varies from chip to chip, so the internal temperature sensor is mainly suitable for applications that detect temperature changes rather than applications that detect absolute temperature. If you need to read the exact temperature, you should use an external temperature sensor.

The on-chip temperature sensor can obtain the temperature inside the chip. After the temperature measurement is started by software or hardware trigger, the test result needs

to be sampled and recorded by ADC1_IN18.The temperature value is calculated by the formula.

### 8.13. Digital-to-Analog Converter (DAC)

Two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

The DAC supports the following functions:

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- In 12-bit mode, data is left-aligned or right-aligned
- Synchronous update function
- Generate noise waves
- Generate a triangle wave
- DAC dual channels convert individually or simultaneously
- Each channel has DMA function
- Conversion by external trigger signal
- Input reference voltage VREF+

The chip uses 8 DAC trigger inputs, and the DAC channels are triggered via timer update outputs, which are also connected to different DMA data streams.

### 8.13. Analog Comparator (COMP)

The device integrates 2 COMP. The COMP function mainly generates a flag signal by comparing the level, which can be used for waking up the CPU from low power consumption through an analog signal, analog signal detection, and timer DAC and PWM combined output loop control.

Key Features:

- Optional inverting analog input:
  - I/OPinout (varies by channel)
  - DACaisle1and Channel2Output
  - Internal reference voltage and three voltage divider values (1/4, 1/2, 3/4) provided by a regulator (buffer divider)
- Each channel has two I/O Pin can be selected as non-inverting analog input
- Programmable hysteresis
- Programmable speed/Power consumption
- Map the output to I/O
- Redirect the output to the timer input which is used to trigger the following events:
  - Capturing events
  - OCREF_CLREvents (for cycle-by-cycle current control)
  - Circuit breaker event (for fastPWMShutdown)
- Blanking comparator output
- Window Comparator
- Can generate interrupts to wake the device from Sleep and Stop modes (via EXIT Controller)
- Direct interrupt output to CPU

### 8.14. Operation Amplifier (OPAMP）

The device contains four op amps, each with two inputs and one output. The three I/Os can be connected to external pins, thus enabling any type of external interconnection. The op amps can be configured internally as a follower and an amplifier with non-inverting gains from 2 to 16 or inverting gains from -1 to -15. The positive input can be connected to the internal DAC. One of the outputs can be connected to the internal ADC.

### 8.15. Serial Wire JTAG Debug Port (SWJ-DP)

The built-in SWJ-DP interface is a combination of JTAG and Serial Wire Debug ports, enabling either a Serial Wire Debug probe or a JTAG probe to be connected to the target.

Debugging is performed using only 2 pins instead of 5 required by JTAG (JTAG pins can be reused as GPIOs with multiplexed functionality): JTAG TMS and TCK pins are shared with SWDIO and SWCLK respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

## IX. Electrical Characteristics

### 9.1. Parameter conditions

All voltages are referenced to VSS.

#### 9.1.1. Minimum and Maximum Values

Minimum and maximum values for all devices. All Tests have been performed during production at ambient temperatures of TA = 25°C and TA max (depending on the temperature range of the selected device).

#### 9.1.2. Typical Value

Typical data are at TA = 25°C, VDD = 3.3 Vtest.

#### 9.1.3. Absolute Maximum Ratings

The chip cannot be operated under any conditions exceeding this value. If it is exceeded, it may cause permanent damage to the chip. And long-term operation under the maximum rated value may affect the reliability of the chip.

### 9.1.4. Limit voltage characteristics

Table 4-1. Limit voltage list

| SYMBOL | RATING | MINIMUM | MAXIMUM | UNIT |
|---|---|---|---|---|
| VDD | External main power supply (including VDDA, VDD, VBAT) | -0.3 | 4.0 | V |
| VIN | Input voltage on FT pin | VSS-0.3 | VSS+4 | |
| | Any other input voltage on the pin | VSS-0.3 | 4.0 | |
| | Input voltage on BOOT pin | VSS | 4.0 | |
| VESD(HBM) | Electrostatic Discharge Voltage (Human Body Model) | +25°C 2000V | | |

### 9.1.5. Limiting current characteristics

Table 4-2. Limiting current characteristics

| SYMBOL | RATING | MAXIMUM | UNIT |
|---|---|---|---|
| ΣIVDD | Total current flowing into all VDD supply rails (source current) (1) | 300 | mA |
| ΣIVSS | Total current drawn from all VSS ground lines (sinking current) (1) | -300 | |
| IVDD | Maximum current flowing into each VDD_x supply line (source current) (1) | 25 | |
| IVSS | Maximum current that can flow from each VSS_x ground line (sink current) (1) | -25 | |
| IIO | Current sinking for any I/O and control pin output | 20 | |
| | Any I/O and control pin can source current | -20 | |
| ΣIIO | Total current sunk by all I/O and control pins | 100 | |
| | Total sink current for all USB I/O outputs | 20 | |
| | Total current sourced by all I/O and control pins | -100 | |
| IINJ(PIN) | Injection current on FT, RST and B pins | -5/+0 | |
| | Injection current on TTa pin | ±5 | |
| ΣIINJ(PIN) | Total injected current (all I/O and control pins) | ±25 | |

- All power and ground pins must remain connected to the external power supply at all times.

### 9.1.6. Extreme temperature characteristics

- Storage temperature range (TSTG): -65°C to +150°C
- Maximum Junction Temperature (TJ): 150°C

## 9.2. Working Parameters

### 9.2.1. Recommended operating conditions

Table 4-3. Recommended operating conditions

| SYMBOL | PARAMETER | CONDITION | | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|---|
| fHCLK | Internal AHB clock frequency | power supply set up: VOS[1:0]=0x01 in PWR_CR register, voltage regulator ON, overload(over-drive)OFF | | 0 | - | 144 | MHz |
| | | power supply set up: VOS[1:0]=0x10 in the PWR_CR register, the voltage regulator is ON | Overload OFF | 0 | - | 168 | |
| | | | Overtake ON | | - | 180 | |
| | | power supply set up: VOS[1:0]=0x11 in the PWR_CR register, the voltage regulator is ON | Overload OFF | 0 | - | 180 | |
| | | | Overload ON | | - | 216 | |
| VDD | Standard operating voltage | - | | 2.1 | - | 3.6 | V |
| VDDA | Analog operating voltage | - | | 2.1 | - | 3.6 | |
| VBAT | Backup working voltage | | | 2.0 | - | 3.6 | |

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| VIN | Input voltage on RST and FT pins | 2.0V≤VDD≤3.6V | -0.3 | - | 5.5 | |
| | | VDD≤2V | -0.3 | - | 5.2 | |
| | Input voltage on TT a pin | - | -0.3 | - | VDDA | |

### 9.2.2. VCAP1/VCAP2 external capacitors

The internal voltage regulator needs to beVCAP1/VCAP2 Pins Connect external capacitors to achieve voltage regulation. CEXT Table 4-4. In the description.

Table 4-4. VCAP1/VCAP2 Operating Conditions

| SYMBOL | PARAMETER | CONDITION |
|---|---|---|
| CEXT | External capacitor value | 2.2μF |
| ESR | ESR of external capacitor | <2Ω |

### 9.2.3. Working conditions during power-on/power-off

Table 4-5. Working conditions during power-on/power-off

| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNIT |
|---|---|---|---|---|
| tVDD | VDD rise time rate | 20 | ∞ | μs/V |
| | VDD Fall Time Rate | 20 | ∞ | |

### 9.2.4. Reset and Power Control Block Features

Table 4-6 The parameters given in Table 4-3 resulting from tests under the ambient temperature and VDD supply voltage conditions summarized in .

Table 4-6. Reset and Power Control Block Features

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| VPVD | Programmable voltage detector level selection | PLS[2:0]=000 (rising edge) | 2.09 | 2.14 | 2.19 | V |
| | | PLS[2:0]=000 (falling edge) | 1.98 | 2.04 | 2.08 | V |
| | | PLS[2:0]=001 (rising edge) | 2.23 | 2.30 | 2.37 | V |
| | | PLS[2:0]=001 (falling edge) | 2.13 | 2.19 | 2.25 | V |
| | | PLS[2:0]=010 (rising edge) | 2.39 | 2.45 | 2.51 | V |
| | | PLS[2:0]=010 (falling edge) | 2.29 | 2.35 | 2.39 | V |
| | | PLS[2:0]=011 (rising edge) | 2.54 | 2.60 | 2.65 | V |
| | | PLS[2:0]=011 (falling edge) | 2.44 | 2.51 | 2.56 | V |
| | | PLS[2:0]=100 (rising edge) | 2.70 | 2.76 | 2.82 | V |
| | | PLS[2:0]=100 (falling edge) | 2.59 | 2.66 | 2.71 | V |
| | | PLS[2:0]=101 (rising edge) | 2.86 | 2.93 | 2.99 | V |
| | | PLS[2:0]=101 (falling edge) | 2.65 | 2.84 | 2.92 | V |
| | | PLS[2:0]=110 (rising edge) | 2.96 | 3.03 | 3.10 | V |
| | | PLS[2:0]=110 (falling edge) | 2.85 | 2.93 | 2.99 | V |
| | | PLS[2:0]=111 (rising edge) | 3.07 | 3.14 | 3.21 | V |
| | | PLS[2:0]=111 (falling edge) | 2.95 | 3.03 | 3.09 | V |
| VPVD hyst (1) | PVD Hysteresis | - | - | 100 | - | mV |
| VPOR/PDR | Power-on/power-off reset threshold | Falling edge | 1.60 | 1.68 | 2.01 | V |
| | | Rising edge | 1.64 | 1.72 | 2.05 | V |

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| VPDR hyst (1) | PDR Hysteresis | - | - | 40 | - | mV |
| VBOR1 | Level 1 undervoltage threshold | Falling edge | 2.13 | 2.19 | 2.24 | V |
| | | Rising edge | 2.23 | 2.29 | 2.33 | V |
| VBOR2 | 2-level undervoltage threshold | Falling edge | 2.44 | 2.50 | 2.56 | V |
| | | Rising edge | 2.53 | 2.59 | 2.63 | V |
| VBOR3 | 3-level undervoltage threshold | Falling edge | 2.75 | 2.83 | 2.88 | V |
| | | Rising edge | 2.85 | 2.92 | 2.97 | V |
| VBOR hyst (1) | BOR Hysteresis | - | - | 100 | - | mV |
| TRSTTEMPO (1) (2) | POR reset duration | - | 0.5 | 1.5 | 3.0 | ms |

- Guaranteed by design, not tested in production.
- Reset duration is measured from power-on (POR reset or VBAT wake-up) to the moment the first instruction is read by the user application code.

### 9.2.5. Supply current characteristics

Current consumption is a comprehensive indicator of multiple parameters and factors, which is obtained by comprehensive evaluation and is not tested in production. These parameters and factors include: operating voltage, ambient temperature, GPIO pin load, product software configuration, operating frequency, GPIO toggle rate, program location in memory, and executed code, etc.

### 9.2.6. Typical and maximum current consumption

Table 4-7. Typical and maximum current consumption in run mode and sleep mode

| | MODEL | CONDITION | TEMPERATURE | TYPICAL VALUE | MAXIMUM VALUE (1) | UNIT |
|---|---|---|---|---|---|---|
| IDD | Operation Mode | LDO ON, HSE ON, L1 cache enabled, all peripherals enabled, bus maximum frequency, VDD = 3.6V | -55℃≤TA≤125℃ | - | 275 | mA |
| | Sleep Mode | LDO ON, HSE ON, PLL clock 180MHz, all peripherals stopped, bus maximum frequency, VDD = 3.6V | | - | 220 | |

- Unless otherwise noted, guaranteed by characterization results, not production tested.

Table 4-8. Typical and maximum current consumption in stop, standby, VBAT modes

| SYMBOL | MODEL | CONDITION | VDD (V) | TYPICAL VALUE | MAXIMUM VALUE (1) | UNIT |
|---|---|---|---|---|---|---|
| | | | | | -55℃≤ TA ≤125℃ | |
| IDD | Stop Mode | FLASHstop | 3.6 | - | 100 | mA |
| IDD | Standby mode | RTCstop,LSEstop | 3.3 | - | 1.3 | mA |
| | VBATmodel | RTCstop,LSEstop | Power off | - | 980 | uA |

- Guaranteed by characterization results, not production tested.
- When analog peripheral blocks such as ADC, DAC, HSE, LSE, HSI, LSI are ON, additional power consumption should be considered.

### 9.2.7. Wake-up timing in low power mode

Table 4-9 The wake-up time measurement method given in is from the wake-up event trigger to the first instruction executed by the CPU:

- For Stop or Sleep mode: The wakeup event is WFE.
- The WKUP (PA0) pin is used to wake up from Standby, Stop, Sleep modes.
- All timings are tested at ambient temperature and VDD=3.3 V.

Table 4-9. Wake-up timing in low power mode

| SYMBOL | PARAMETER | CONDITION | TYPICAL VALUE (1) | MAXIMUM (1) | UNIT |
|---|---|---|---|---|---|
| tWUSLEEP (2) | Wake up from sleep mode | - | 20 | 20 | CPU clock cycle |
| tWUSTOP (2) | Wake up from stop mode, MR/LP regulator in normal mode | Main voltage regulator ON | 17 | 18 | μs |
| | | The main voltage regulator is ON and the Flash is in deep power-down mode. | 68 | 75 | |
| | | Low power regulator ON | twenty two | 25 | |
| | | Low power regulator is ON, Flash is in deep power-down mode | 72 | 80 | |
| tWUSTOP (2) | Wake-up from stop mode, MR/LP regulator in low load mode | Main regulator in low load mode, Flash is in deep power-down mode | 82 | 95 | μs |
| tWUSTDBY (2) | Wake up from standby mode | Exiting standby mode | 350 | 360 | μs |

- Guaranteed by design, not production tested.
- The wake-up time is measured from the time the wake-up is triggered until the first instruction is read by the application code.

### 9.2.8. External Clock Source Characteristics

Use a high-speed external clock generated by an external oscillator source

Table 4-10High-speed external user clock characteristics

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| fHSE_ext | External user clock source frequency (1) | - | 1 | - | 50 | MHz |
| VHV | OSC_IN input pin high level voltage | | 0.7VDD | - | $V_{DD}$ | V |
| VHSEL | OSC_IN input pin low level voltage | | $V_{SS}$ | - | $0.3V_{DD}$ | |
| tw(HSE) $t_{w(HSE)}$ | OSC_IN high or low time (1) | | 5 | - | - | ns |

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| tr(HSE)<br>tf(HSE) | OSC_IN rise or fall time (1) | | - | - | 5 | |
| Cin(HSE) | OSC_IN input capacitor (1) | - | | 3 | | pF |
| DuCy(HSE) | Duty Cycle | - | 45 | - | 55 | % |

- Guaranteed by design.

### 9.2.9. High-speed external clock generated using a crystal/ceramic oscillator

The high speed external (HSE) clock can be generated using a 4~26MHz crystal/ceramic resonator oscillator. The information given in this section is based on Table 4-11. The typical external components listed in are obtained through comprehensive characterization evaluation. In the application, the resonator and load capacitors must be as close as possible to the oscillator pins to reduce output distortion and stabilization time at startup. For detailed parameters of the crystal resonator, please consult the crystal resonator manufacturer.

Table 4-11. HSE 4-26MHz Oscillator Characteristics

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| fOSC_IN | Oscillator frequency | - | 4 | - | 26 | MHz |
| tSU(HSE)(1) | Startup time | VDD is stable | | 2 | | ms |

- tSU(HSE) is the start-up time, measured from the time HSE is enabled by software until a stable 8MHz oscillation frequency is obtained. This value is based on characterization and is not production tested. This value is measured based on a standard crystal resonator and may vary with different crystal manufacturers.

### 9.2.10. Internal clock characteristics

#### 9.2.10.1. High Speed Internal (HSI) RC Oscillator

Table 4-12. HSI Oscillator Characteristics(1)

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| f | frequency | - | 14 | 16 | 18 | MHz |
| | HSI Users Adjust the scale(2) | - | | 1% | | % |
| | HSI Oscillator Accuracy | TA=125℃ | -2 | - | 2 | % |
| | | TA=25℃ | -1 | | 2 | % |
| | | TA=-55℃ | -2 | | 2 | % |
| tsu(HSI)(2) | HSI Oscillator Stablize time | - | | 2.2 | | μs |

- Unless otherwise specified, VDD=3.3V, TA=-40 to 105℃.
- Guaranteed by design, not tested in production.
- Guaranteed by characterization results, not production tested.

#### 9.2.10.2. Low speed internal (LSI) RC oscillator

Table 4-13. LSI Oscillator Characteristics

| SYMBOL | PARAMETER | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| fLSI | frequency | 20 | 32 | 45 | kHz |
| tsu(LSI) | LSI oscillator start-up time | | 15 | | μs |
| IDD(LSI) | LSI Oscillator Power Consumption | | 0.4 | | μA |

### 9.2.11. PLL Characteristics

Table 4-14. PLL Characteristics

| SYMBOL | PARAMETER | CONDITION | | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|---|
| fPLL_IN | PLL input clock | - | | 0.95 | 1 | 2.0 | MHz |
| fPLL_OUT | PLL frequency multiplier output clock | - | | 24 | - | 216 | |
| Jitter[1)] | Cycle-to-cycle jitter | System clock216MHz | RMS | | 25 | | ps |
| | | | Peak to Peak | | ±150 | | |
| | Periodic Jitter | | RMS | | 15 | | |
| | | | Peak to Peak | | ±200 | | |

- Determined by comprehensive analysis, not tested in production.

### 9.2.12. Memory(FLASH)characteristic

Table 4-15. FLASH Memory characteristics

| SYMBOL | PARAMETER | MINIMUM | TYPICAL VALUE(1) | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| TPROG | Single byte write time | 8 | - | 10 | μs |
| TERASE | Page Erase Time | 3.2 | - | 4 | ms |
| | Full chip erase time | 30 | - | 40 | ms |
| IDDPROG | Single byte write current | - | - | 6.9 | mA |
| IDDERASE | Page/chip erase current | - | - | 2.3 | mA |
| IDDREAD | Read current @24MHz | - | 2 | 3.1 | mA |
| NEND | Erase life | - | 100 | | Thousand times |
| T | Data retention period | 20 | | | Year |

- Typical values are at 1.5V, TT process and 25°C.
- VCORE=1.35~1.65V, VCORE is the core voltage.

### 9.2.13. Electrical sensitivityEMC

Use specific measurement methods to test ESD and LU on sampled products.

#### 9.2.13.1. Electrostatic Discharge (ESD)

Electrostatic discharge is applied to the pins of each sample for each pin combination. This test complies with the JESD22-A114/C101 standard.

Table 4-16. ESD Absolute Maximum Ratings

| SYMBOL | RATING | CONDITION | CLASSIFICATION | MAXIMUM(1) | UNIT |
|---|---|---|---|---|---|
| VESD(HBM) | Electrostatic discharge voltage (Human Model) | TA = +25°C, conform toANSI/ESDA/JEDEC JS-001-2012standard | 2 | 2000 | V |
| VESD(CDM) | Electrostatic discharge voltage (Charging equipment model) | TA = +25 °C,conform toANSI/ESD S5.3.1-2009Standard, packageLQFP208 | 3 | 250 | |
| | | TA = +25 °C, conform toANSI/ESD S5.3.1-2009Standard, packageLQFP208 | 4 | 500 | |

#### 9.2.13.2. Electrostatic latch (Latch-up)

To evaluate latch-up performance, two complementary static latch-up tests are performed on the six devices:

- Apply overvoltage to each power supply pin.
- Apply current injection to each input, output, and configurable GPIO pin.
- These tests comply with the EIA/JESD 78A IC latch-up standard.

Table 4-17Electrical sensitivity

| symbol | parameter | condition | Classification |
|---|---|---|---|
| LU | StaticLockout classification | TA=+105 °C,conform toJESD78A Standard | Class II Category A |

### 9.2.14. GPIO port characteristic

#### 9.2.14.1. General Input /Output Characteristics

All I/Os are CMOS and TTL compatible

Table 4-18. GPIO static characteristics

| SYMBOL | PARAMETER | CONDITION (UNLESS OTHERWISE STATED, -40° C≤TA≤125℃) | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| VIL | GPIO pin input low level voltage | 2.1V≤VDD≤3.6V | - | - | 0.3VDD(1) | V |
| VIH | FT, TTa and NRST I/O input high voltage (5) | 2.1V≤VDD≤3.6V | 0.7VDD | - | - | V |
| | BOOT I/O input high level voltage | 2.1V≤VDD≤3.6V | 0.7VDD | - | - | |
| Ilkg | I/O Input leakage Current | VSS≤VIN≤VDD<br>VSS=0v<br>2.1V≤VDD≤3.6V | - | - | ±3 | μA |
| RPU | Weak pull-up equivalent resistance | Remove all pins except PA10/PA12/PB12/PB15, VDD=3.3v | 18 | - | 50 | kΩ |
| | | PA10/PA12/PB12/PB15, VDD=3.3v | 1.5 | - | 50 | |
| RPD | Weak pull-down equivalent resistance | Except PA10/PA12/PB12/PB15All pins outside, VDD=3.3v | 18 | - | 50 | |
| | | PA10/PA12/PB12/PB15, VDD=3.3v | 1.5 | - | 50 | |
| CIO | I/O Pin Capacitance | - | - | 5 | - | pF |

- Production Test

#### 9.2.14.1.1. Output Current

GPIO (General Purpose Input/Output) can provide a maximum of ±20 mA source or sink current. PC13, PC14, PC15, PI8 can only provide a maximum of ±3 mA source or sink current. When using PC13 to PC15 and PI8 GPIOs in output mode, the speed should not exceed 2MHz with a maximum load of 30pF.

- In the user application, the number of GPIO pins that can drive current must be limited to ensure that the drive current does not exceed Table 4-2. Absolute Maximum Ratings.

#### 9.2.14.1.2. Output voltage

Table 4-19. Output voltage characteristics

| SYMBOL | PARAMETER | CONDITION(UNLESS OTHERWISE STATED, -40°C≤TA≤125℃) | MINIMUM | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| VOL | Output low level | IIO=4mA<br>2.1V≤VDD≤3.6V | - | 0.3VDD | V |
| $VO_H$ | Output high Level | IIO=-4mA, except PC13, PC14, PC15<br>2.1V≤VDD≤3.6V | 0.7VDD | | |
| $VO_H$ | Output high Level | IIO=-1mA, PC13, PC14, PC15<br>2.1V≤VDD≤3.6V | 0.7VDD | | V |

#### 9.2.14.1.3. Input/ Output AC Characteristics

The speed is configured by the OSPEEDRy [1:0] bits. For a description of the GPIOx_ SPEEDR GPIO port output speed register, refer to the BST32F7 Series Technical Reference Manual. If the maximum GPIO frequency exceeds 50MHz, a compensation unit should be used.

Input/output AC characteristics at Table 4-20Given in.

Table 4-20. GPIO communication Features(1)

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| tEXTIpw | EXTI Pulse width of the external signal detected by the controller | - | | 10 | | ns |

1. Guaranteed by design, not tested in production.

### 9.2.15. NRST Pin Characteristics

The NRST pin input driver is based on CMOS technology. It is connected to a permanent pull-up resistor RPU (see Table 4-21).

Table 4-21. NRST Pin Characteristics

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| RPU | Weak pull-up equivalent resistor (1) | VIN=VSS | 30 | 40 | 50 | kΩ |
| TNRST_OUT | The duration of the reset pulse generated | Internal reset source | 20 | - | | μs |

### 9.2.16. TIM counter characteristics

Table 4-21. TIMx features (1)

| SYMBOL | PARAMETER | CONDITION | MINIMUM | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| tres(TIM) | Timer resolution time | | 1 | - | tTIMxCLK |
| fEXT | Timer external clock frequency on CH1 to CH4 | fTIMCLK=216MHz | 0 | fTTIMxCLK/2 | MHz |
| ResTIM | Timer resolution | | - | 16/32 | bit |

- Guaranteed by design, not tested in production.

### 9.2.17. 12-bit ADC Features

Table 4-23. ADC Characteristics

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| VDDA | powered by | -40℃≤TA≤125℃ | 2.1 | - | 3.6 | V |
| VREF+ | Positive reference voltage | | 2.1 | - | VDDA | V |
| VAIN | Conversion voltage range (1) | - | | | VREF+ | V |
| RAIN | External input impedance (1) | - | | | 50 | kΩ |
| f | Sampling frequency (fADC =22.5MHz) | 12-bit resolution<br>Single ADC | | | 1.5 | Msps |

Table 4-24. ADC static accuracy when fADC=22.5MHz

| SYMBOL | PARAMETER | TEST CONDITIONS | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| EO(2) | Offset Error | -40°C≤TA≤125°C<br>VDDA=VREF+=3.3V | | ±4 | LSB |
| EG(3) | Gain Error | | | ±4 | |
| ED | Differential Nonlinearity Linearity error | | | ±4 | |
| EL | Integral No Linearity error | | | ±4 | |

Table 4-22. ADC dynamic accuracy when fADC=22.5MHz

| SYMBOL | PARAMETER | TEST CONDITIONS | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| ENOB(1) | Significant digits | VDDA=VREF+=3.3V<br>Input frequency =20KHz<br>-40°C≤TA≤125°C | 10.6 | 10.8 | | bits |
| SINAD(1) | Signal to Noise and Distortion Ratio | | 64 | 67 | | dB |
| SNR | Signal-to-Noise Ratio | | 60 | | | |
| THD | Total harmonic frequency | | | | -60 | |

- Guaranteed by characterization results, not production tested.
- EO = Offset Error: The deviation between the first actual transition and the first ideal transition.
- EG = Gain Error: The deviation between the last ideal transition and the last actual transition.

### 9.2.18. DAC Electrical Characteristics

Table 4-23. DAC Characteristics

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| VDDA | Analog supply voltage | -40°C≤TA≤125°C | 2.1 | - | 3.6 | V |
| VREF+ | Reference supply voltage | | 2.1 | - | 3.6 | V |
| RLOAD(1) | Buffer Open Load resistance | - | 5 | - | | kΩ |
| RO(1) | Buffer closure Impedance output | - | | - | 15 | kΩ |
| CLOAD(1) | Capacitive load | - | | - | 50 | pF |
| IVREF+(2) | DAC current consumption in standby mode, No load, code=0X800 | - | | 170 | 240 | μA |
| IDDA2) | DAC current consumption in quiescent mode (3) No load, code=OXF1C | - | | | 840 | μA |
| DNL(1) | Differential Linear Distortion | -40°C≤TA≤125°C, VDD=VDDA=3.3V | -4 | - | 4 | LSB |
| INL(2) | Integral nonlinear distortion | | -5 | - | 5 | LSB |
| OE | Offset Error No load, code=0X800 | | -10 | - | 10 | mV |
| GE | Gain Error | | -1.5 | - | 1.5 | % |
| PSRR | Power Supply Rejection Ratio | | | - | -40 | dB |

- Guaranteed by design, not tested in production.

- Guaranteed by characterization results, not production tested.

### 9.2.18. Temperature Sensor Characteristics

Table 4-24. Temperature Sensor Characteristics

| SYMBOL | PARAMETER | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| TL(1) | VSENSE Linearity with Respect to Temperature | | ±1 | | ℃ |
| V25(1) | Voltage at 25℃ | | 0.76 | | V |
| tSTART(2) | Startup time | | 6 | | μs |

- Guaranteed by characteristic analysis results.
- Guaranteed by design.

### 9.2.19. Communication interface

#### 9.2.19.1. I2C Interface Characteristics

- I2C bus interface supports standard mode (up to 100 kHz), fast mode (up to 400 kHz), and overspeed mode (up to 1 MHz)
- The I/O pins mapped to SDA and SCL are not "real" open-drain pins. When configured as open-drain pins, the PMOS connected between the I/O pin and VDD is disabled but still exists.
- Overdrive mode does not support 20mA output drive
- All I2C SDA and SCL I/Os have a built-in analog filter. The analog filter characteristics can be found in the following Table:

Table 4-25. I2C Analog Filter Characteristics (1)

| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNIT |
|---|---|---|---|---|
| FWf | The maximum peak pulse width is limited by the analog filter | 50 | 260 | ns |

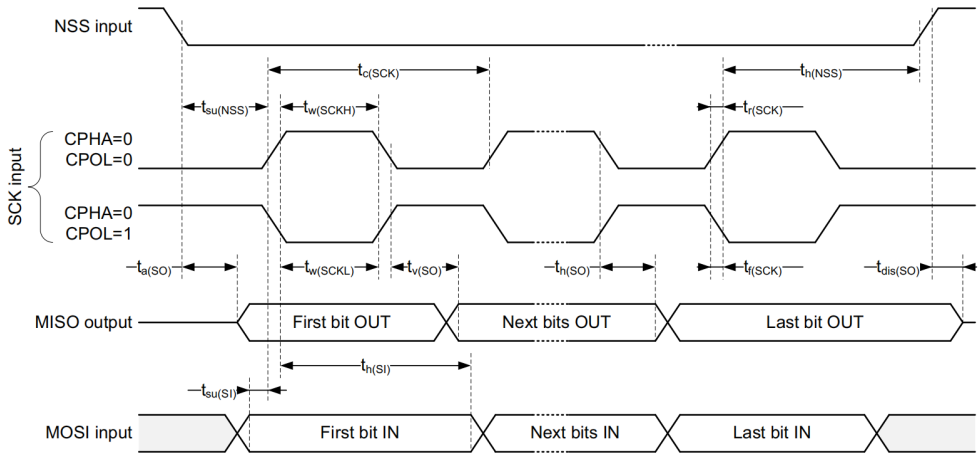
- Guaranteed by characterization results, not production tested.

### 9.2.19.2. SPI Interface Characteristics

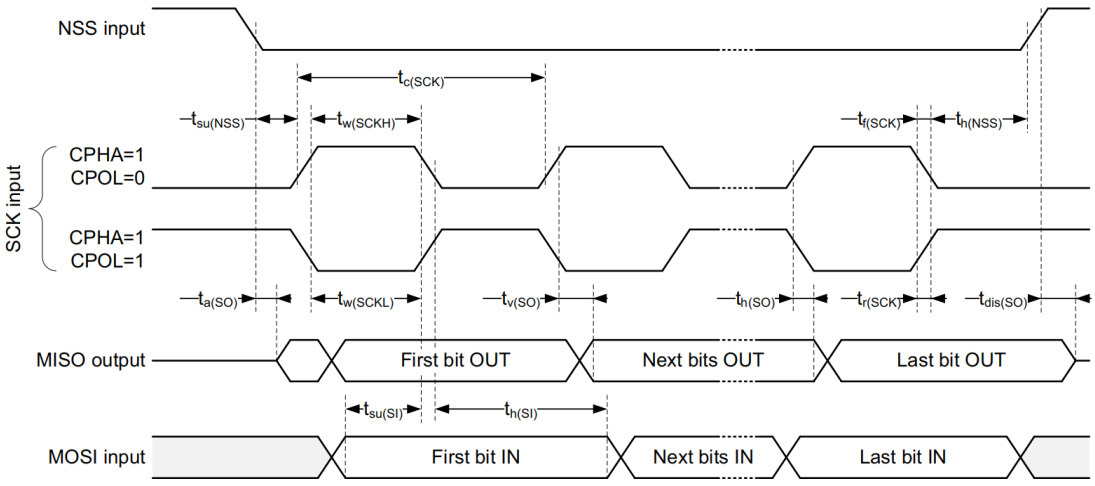
Table 4-26. SPI electrical characteristics(1)

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| f 1/tc(SCK) | SPI clock frequency | Main Mode 2.7≤VDD≤3.6 | - | - | | MHz |
| | | Slave Mode 2.7≤VDD≤3.6 | - | - | | |
| tsu(NSS) | NSS establishment time | Slave mode, SPI prescaler = 2 | 4x$Tp_{clk}$ | - | - | ns |
| th(NSS) | NSS hold time | Slave mode, SPI prescaler = 2 | 2x$Tp_{clk}$ | - | - | |
| tw(SCKH) tw(SCKL) | SCK high and low time | Main Mode | $Tp_{clk}$-1 | $Tp_{clk}$ | $Tp_{clk}$+1 | |
| tsu(MI) | Data input setup time | Main Mode | | - | | ns |
| tsu(SI) | | Slave Mode | | - | | |
| th(MI) | Data input hold time | Main Mode | | - | | |
| th(SI) | | Slave Mode | | - | | |
| tv(SO) | Data output valid time | Slave mode 2.7 ≤ VDD ≤ 3.6 V | | 6.5 | | |
| tv(MO) | | Main mode 2.7 ≤ VDD ≤ 3.6 V | | 2 | | |

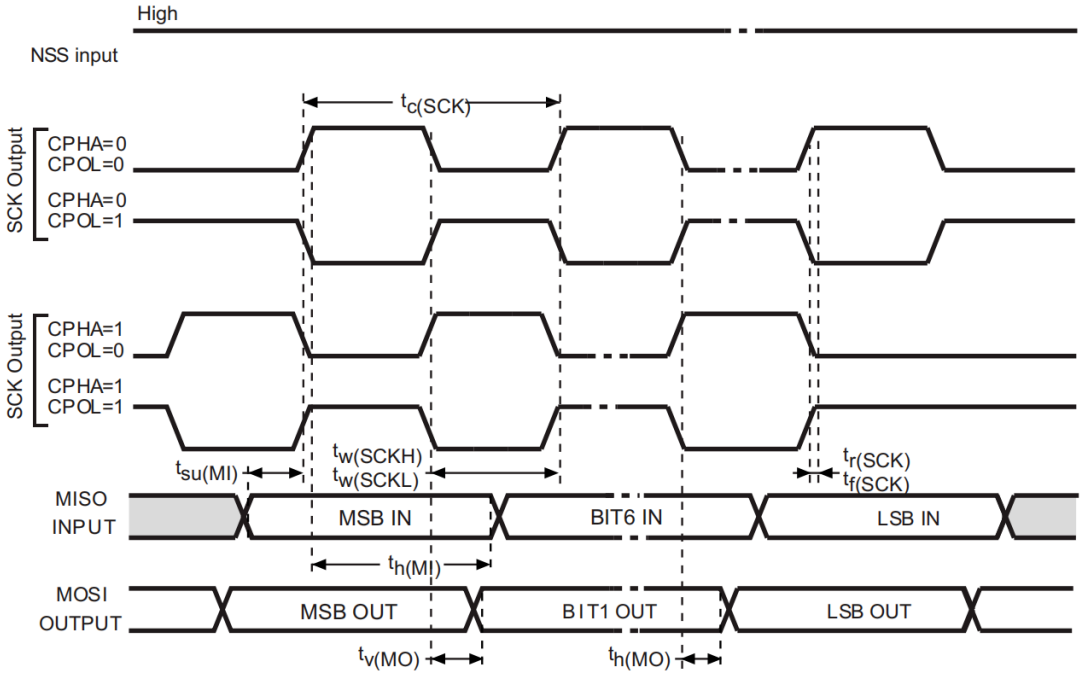
- Guaranteed by characterization results, not production tested.




Picture 4-1. SPI timing diagram - slave mode, CPHA=0




Picture 4-2. SPI timing diagram - slave mode, CPHA=1




Picture 4-3. SPI Timing Diagram - Master Mode

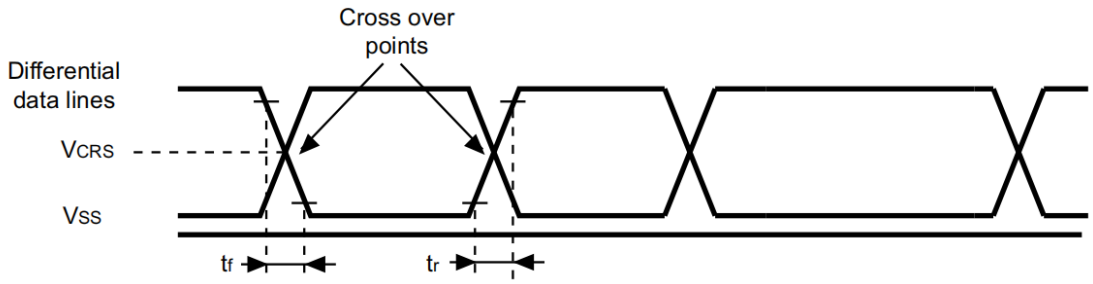
### 9.2.19.3. USB OTG Full Speed (FS) Features

This interface is available on both USB OTG HS and USB OTG FS controllers.

Table 4-27. USB OTG Full Speed DC Electrical Characteristics

| SYMBOL | | PARAMETER | CONDITION | MINIMUM (1) | TYPICAL VALUE | MAXIMUM(1) | UNIT |
|---|---|---|---|---|---|---|---|
| Input Level | VDD | USB OTGFS Operating voltage | - | 3.0 | - | 3.6 | V |
| | VDI(2) | Differential Input Sensitivity | I (USB_FS/HS_D+,USB_FS/HS_D-) | 0.2 | - | | V |
| | VCM(2) | Differential common mode range | Including VDI range | 0.8 | - | 2.5 | |
| | VSE(2) | Single-ended receive threshold | - | 1.3 | - | 2.0 | |
| Output Level | VOL | Static output low level | 1.24 kΩ ofRL is connected to 3.6V (3) | | - | 0.3 | V |
| | VOH | Static output high level | 15kΩRL connected to VSS (3) | 2.4 | - | 3.6 | |
| RPD | | PA11, PA12, PB14, PB15 (USB_FS/HS_D+/D-) Pull-down resistor | VIN=VDD | 17 | - | 24 | kΩ |
| RPU | | PA12(USB_FS/HS_D+) Pull-up resistor | VIN=VSS, idle state | 1.5 | - | 2.1 | |

- All voltages are based on the equipment ground.
- Guaranteed by design, not tested in production.
- RL is the load connected to the USB OTG full-speed driver.




Picture 4-4ю USB OTG full-speed timing: data signal rise and fall time definition

Table 4-28. USB OTG Full Speed Electrical Characteristics(1)

| DRIVER CHARACTERISTICS | | | | | |
|---|---|---|---|---|---|
| SYMBOL | PARAMETER | CONDITION | MINIMUM | MAXIMUM | UNIT |
| tr | Rise time (2) | CL=50pF | 4 | 20 | ns |
| tf | Fall time (2) | CL=50pF | 4 | 20 | ns |
| trfm | Rise/Fall Time Matching | tr/tf | 90 | 110 | % |
| VCRS | Output signal crossover voltage | - | 1.3 | 2.0 | V |
| ZDV | Output drive impedance (3) | Drive high or low | 28 | 44 | Ω |

- Guaranteed by design, not tested in production.
- Measured between 10% and 90% of the data signal

### 9.2.19.4. USB High Speed (HS) features (via ULPI)

Table 4-29. USB HS DC Electrical Characteristics

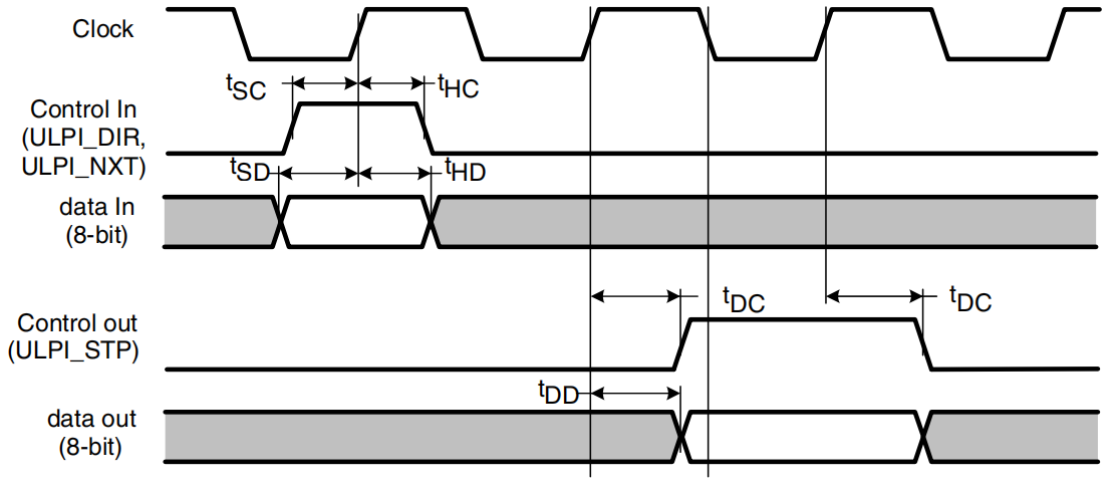
| SYMBOL | | PARAMETER | MINIMUM (1) | MAXIMUM (1) | UNIT |
|---|---|---|---|---|---|
| Input Level | VDD | USB OTG HS operating voltage | 2.1 | 3.6 | V |

- All voltages are referenced to the equipment end ground.

Table 4-30. Dynamic Features: USB ULPI(1)

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| tS | Control signal setup time (ULPI_DIR,ULPI_NXT) | 2.7V<VDD<3.6V CL=20pF OSPEEDRy[1:0]=11 | 2 | - | | ns |
| THC | Control signal holding time (ULPI_DIR,ULPI_NXT) | | 1.5 | - | | |
| tD | Data within the creation time | | 3 | - | | |
| HkDJ | Data within retention time | | 2.2 | - | | |
| tDC/tDD | Data/Control Output Delay | | | 6.5 | 8 | |

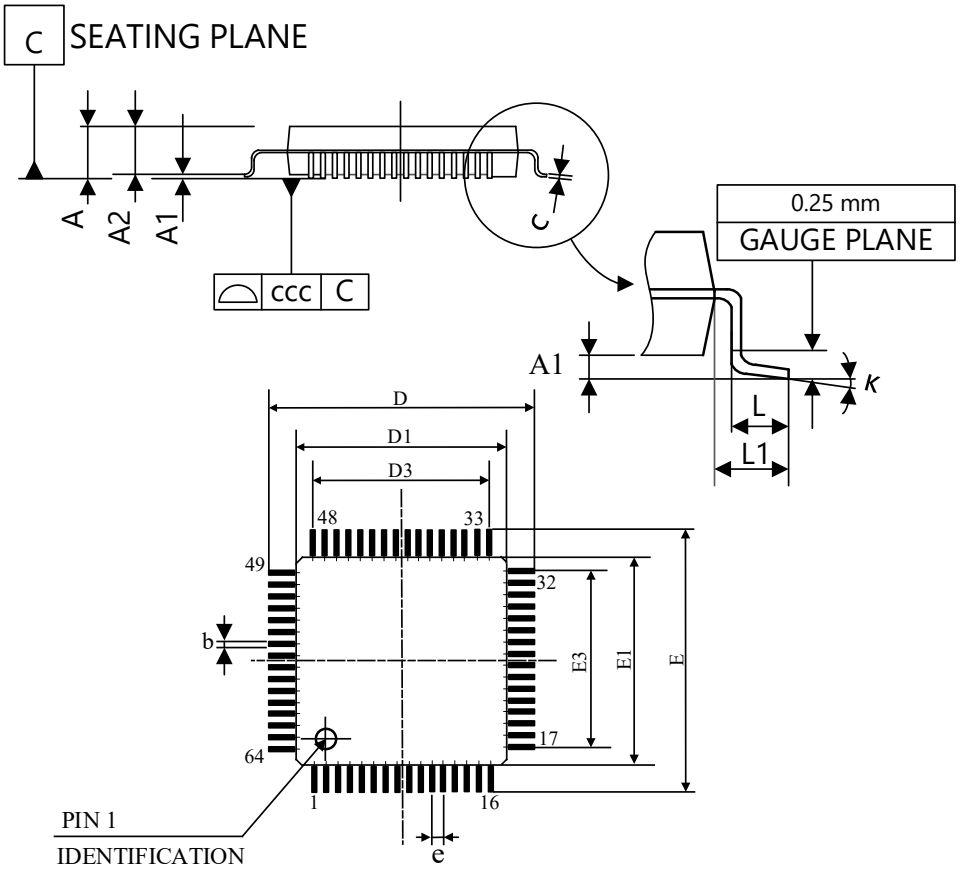
- Guaranteed by characterization results, not production tested.




Picture 4-5. ULPI Timing Diagram

# X. Package size

## 10.1. LQFP64 package




Picture 5-1. BST32F722 LQFP64 package diagram

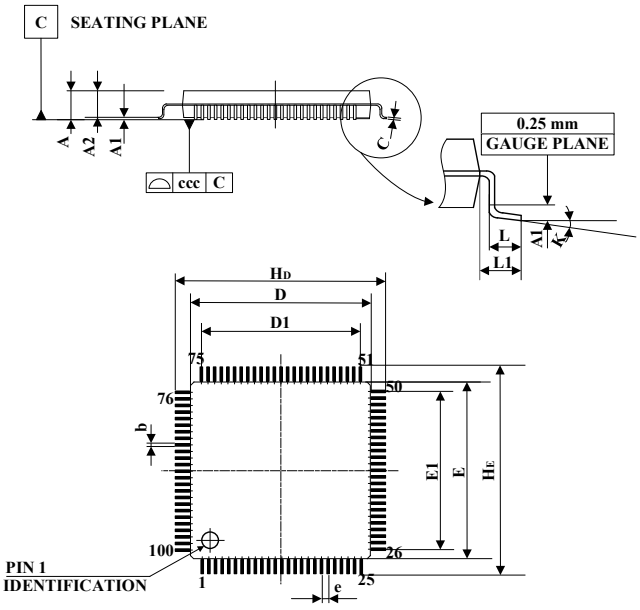
Table 5-1. Package size description

Unit is mm

| DIMENSION SYMBOLS | NUMERIC | | |
|---|---|---|---|
| | MINIMUM | NOMINAL | MAXIMUM |
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.350 | — | 1.45 |
| b | 0.17 | — | 0.27 |

| DIMENSION SYMBOLS | NUMERIC | | |
|---|---|---|---|
| | MINIMUM | NOMINAL | MAXIMUM |
| c | 0.090 | — | 0.200 |
| D | | 12.00 | |
| D1 | | 10.00 | |
| D3 | | 7.5 | |
| E | | 12.00 | |
| E1 | | 10.00 | |
| E3 | | 7.50 | |
| e | — | 0.500 | — |
| K | 0° | | 7° |
| L | 0.45 | 0.60 | 0.75 |
| L1 | — | 1.000 | — |
| ccc | — | — | 0.08 |

## 10.2. LQFP100 package



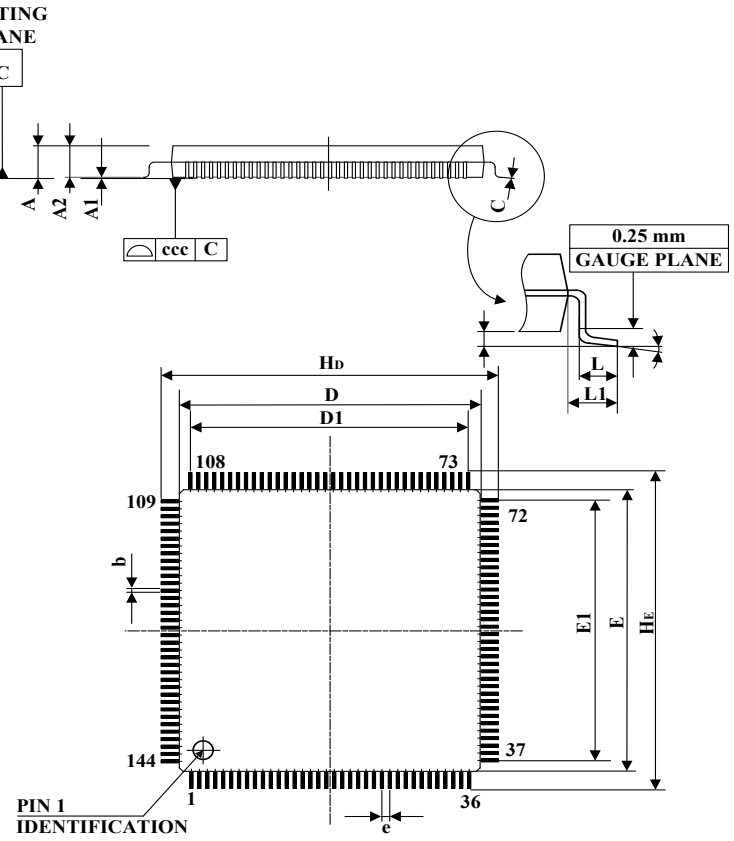

Picture 5-2. BST32F7 series LQFP100 package diagram

Table 5-2. Package size description

Unit is mm

| DIMENSION SYMBOLS | NUMERIC (MM) | | |
|---|---|---|---|
| | MINIMUM | TYPICAL | MAXIMUM |
| A | — | — | 1.70 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.90 | 1.00 | 1.10 |
| b | 0.120 | 0.220 | 0.320 |
| c | 0.040 | — | 0.250 |
| HD | 15.700 | 16.000 | 16.300 |
| D | 13.700 | 14.000 | 14.300 |
| D1 | — | 12.000 | — |
| HE | 15.700 | 16.000 | 16.300 |
| E | 13.700 | 14.000 | 14.300 |
| E1 | — | 12.000 | — |
| e | — | 0.500 | — |
| L | 0.45 | 0.600 | 0.750 |
| L1 | — | 1.000 | — |
| ccc | — | — | 0.08 |
| k | 0° | 3.5° | 7° |

## 10.3. LQFP144 package




Picture 5-3. BST32F7 series LQFP144 package diagram

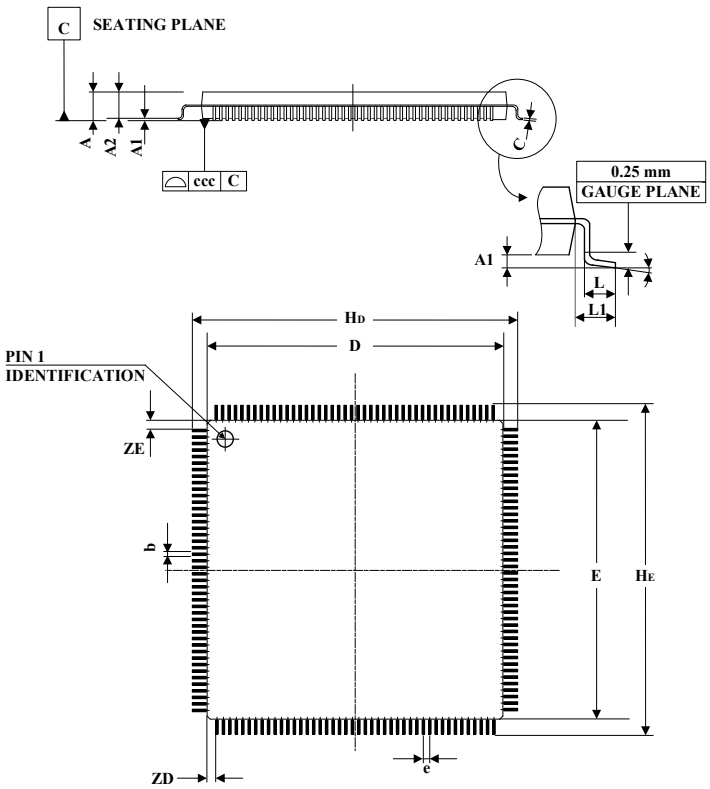
Table 5-3. Package size description

Unit is mm

| DIMENSION SYMBOLS | NUMERIC (MM) | | |
|---|---|---|---|
| | MINIMUM | TYPICAL | MAXIMUM |
| A | — | — | 1.700 |
| A1 | 0.050 | — | 0.150 |
| A2 | 1.300 | 1.400 | 1.500 |
| b | 0.120 | 0.220 | 0.320 |
| c | 0.090 | — | 0.200 |
| HD | 21.700 | 22.000 | 22.300 |
| D | 19.700 | 20.000 | 20.300 |

| DIMENSION SYMBOLS | NUMERIC (MM) | | |
|---|---|---|---|
| | MINIMUM | TYPICAL | MAXIMUM |
| D1 | — | 17.500 | — |
| HE | 21.700 | 22.000 | 22.300 |
| E1 | — | 17.500 | — |
| E | 19.700 | 20.000 | 20.300 |
| e | | 0.500 | — |
| L | 0.450 | 0.600 | 0.750 |
| L1 | — | 1.000 | — |
| ccc | — | — | 0.080 |
| k | 0° | 3.5° | 7° |

## 10.4. LQFP176 package



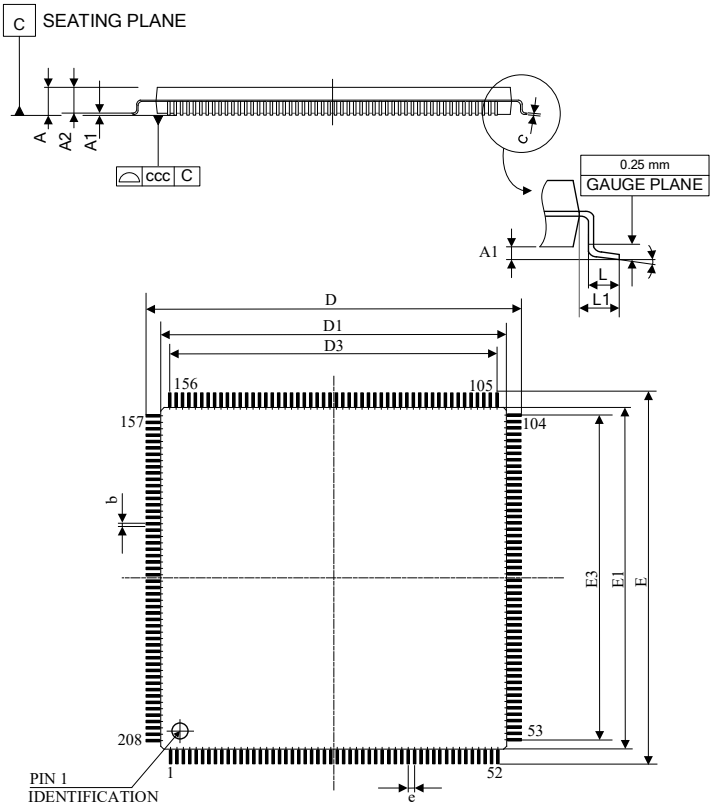

Picture 5-4. BST32F7 series LQFP176 package diagram

Table 5-4. Package size description

Unit is mm

| DIMENSION SYMBOLS | NUMERIC | | |
|---|---|---|---|
| | MINIMUM | NOMINAL | MAXIMUM |
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.350 | — | 1.45 |
| b | 0.17 | — | 0.27 |
| c | 0.090 | — | 0.200 |
| D | 23.900 | — | 24.100 |
| E | 23.900 | — | 24.100 |
| e | — | 0.500 | — |
| HD | 25.800 | — | 26.200 |
| HE | 25.800 | — | 26.200 |
| L | 0.45 | — | 0.75 |
| L1 | — | 1.000 | — |
| ZD | — | 1.250 | — |
| ZE | — | 1.250 | — |
| ccc | — | — | 0.08 |
| k | 0° | — | 7° |

## 10.5. LQFP208 package




Picture 5-5. BST32F7 series LQFP208 package diagram

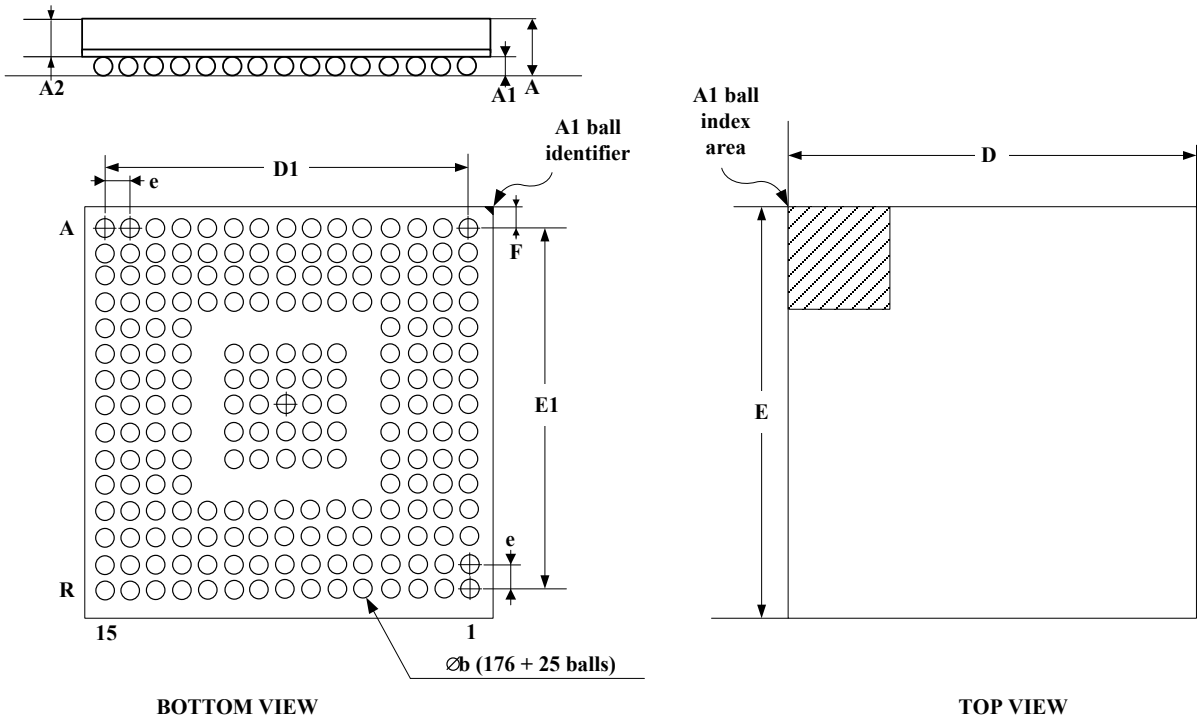
Table 5-5. Package size description

Unit is mm

| DIMENSION SYMBOLS | NUMERIC | | |
|---|---|---|---|
| | MINIMUM | NOMINAL | MAXIMUM |
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.350 | — | 1.45 |
| b | 0.170 | 0.220 | 0.270 |
| c | 0.090 | — | 0.200 |

| | | | |
|---|---|---|---|
| D | 29.900 | 30.000 | 30.200 |
| D1 | 27.800 | 28.000 | 28.200 |
| D3 | — | 25.500 | — |
| E | 29.800 | 30.000 | 30.200 |
| E1 | 27.800 | 28.000 | 28.200 |
| E3 | — | 25.500 | — |
| e | — | 0.500 | — |
| L | 0.45 | 0.600 | 0.750 |
| L1 | — | 1.000 | — |
| ccc | — | — | 0.08 |
| k | 0° | 3.5° | 7° |

## 10.6. PBGA176 package




Picture 5-6. BST32F7 series PBGA176 package diagram

Table 5-6. Package size description

Unit is mm

| DIMENSION SYMBOLS | NUMERIC | | |
|---|---|---|---|
| | MINIMUM | TYPICAL | MAXIMUM |
| A | 1.00 | — | 1.55 |
| A1 | — | — | 0.45 |
| A2 | — | — | 1.10 |
| b | | 0.40 | |
| D | 9.800 | — | 10.200 |
| D1 | | 9.100 | |
| E | 9.800 | — | 10.200 |
| E1 | | 9.1 | |
| e | — | 0.650 | — |
| F | 0.4 | 0.45 | 0.5 |

## XI. Ordering Information

Table 6-1. Product Ordering Information

| PRODUCT MODEL | PACKAGE | MOQ | MPQ | PACKAGE | OPERATING TEMPERATURE | GRADE |
|---|---|---|---|---|---|---|
| BST32F722LQFP64I | LQFP64 | 1 | 1 | tray | -40°～85° | industry |
| BST32F722LQFP64E | LQFP64 | 1 | 1 | tray | -55°～125° | Military Temperature |
| BST32F722MLQFP64 | LQFP64 | 1 | 1 | tray | -55°～125° | N1 |
| BST32F722MCQFP64 | CQFP64 | 1 | 1 | tray | -55°～125° | B |
| BST32F767LQFP100I | LQFP100 | 1 | 1 | tray | -40°～85° | industry |
| BST32F767LQFP100E | LQFP100 | 1 | 1 | tray | -55°～125° | Military Temperature |
| BST32F767LQFP100M3 | LQFP100 | 1 | 1 | tray | -55°～125° | N1 |

| PRODUCT MODEL | PACKAGE | MOQ | MPQ | PACKAGE | OPERATING TEMPERATURE | GRADE |
|---|---|---|---|---|---|---|
| BST32F722LQFP64I | LQFP64 | 1 | 1 | tray | -40°～85° | industry |
| BST32F722LQFP64E | LQFP64 | 1 | 1 | tray | -55°～125° | Military Temperature |
| BST32F722MLQFP64 | LQFP64 | 1 | 1 | tray | -55°～125° | N1 |
| BST32F722MCQFP64 | CQFP64 | 1 | 1 | tray | -55°～125° | B |
| BST32F767LQFP144I | LQFP144 | 1 | 1 | tray | -40°～85° | industry |
| BST32F767LQFP144E | LQFP144 | 1 | 1 | tray | -55°～125° | Military Temperature |
| BST32F767LQFP176I | LQFP176 | 1 | 1 | tray | -40°～85° | industry |
| BST32F767LQFP176E | LQFP176 | 1 | 1 | tray | -55°～125° | Military Temperature |
| BST32F767LQFP208I | LQFP208 | 1 | 1 | tray | -40°～85° | industry |
| BST32F767LQFP208E | LQFP208 | 1 | 1 | tray | -55°～125° | Military Temperature |
| BST32F767PBGA176I | PBGA176 | 1 | 1 | tray | -40°～85° | industry |
| BST32F767PBGA176E | PBGA176 | 1 | 1 | tray | -55°～125° | Military Temperature |
| BST32F767PBGA176M3 | PBGA176 | 1 | 1 | tray | -55°～125° | N1 |

Additional notes:

- M, N1, E product quality grade description, please contact the local market contact window
- For ceramic seal series products, please contact local sales for confirmation
- For more F7 series products, please contact your local sales representative

## XII. Revision History

| SERIAL NUMBER | EDITION | CHANGE DESCRIPTION | CHANGE PERSON | CHANGE DATE | REMARK |
|---|---|---|---|---|---|
| 1. | V2.0 | Modify order model | - | 2024.1 | |