# BST32F4 Series

# Datasheet 1.0

32 - bit RISC core 180MHz main frequency , support single and double precision floating point operations, built-in instruction/data dual 16K cache, 2MB F LASH , 512KB SRAM, support external memory (FMC), integrated USB OTG HS/FS , 10/100 EMAC , 1 SD IO, 1 QSPI , 4 /4 USART / UART , 6 SPI, 4 I 2 C , 1 MDIO, 3 CAN, 3 12-bit ADC, 2 12 -bit DAC

## I. Product Features

- Core

  32-bit RISC core, operating frequency 180MHz, built-in single and double precision floating point unit

- Storage
  - 2M FLASH, support read and write synchronization
  - 512Kbyte SRAM + 16Kbyte ITCM + 4Kbyte backup SRAM
- Power Management and Reset
  - VDD: 2.1v - 3.6v
  - VBAT: 2.0v - 3.6v
  - POR, PDR, PVD, BOR
  - Support external pin reset, software reset, low power mode reset, watchdog timer reset
- Clock
  - HSE (4-26MHz), LSE (32.768K), H SI (16MHz, industrial grade), LSI (32KHz)
  - 1 SDIO

- 1 extended memory control (FMC) interface
- Communication interface
  - 4 USARTs and 4 UARTs
  - 6 SPI
  - 4 I2C, support SMBus protocol
  - 3 CAN 2.0A/B (only 176PIN supports CAN3)
  - 1 MDIO slave
  - 1 x QSPI
- Timer:

  8 16-bit general timers, 2 32-bit general timers, 2 advanced timers (support motor PWM complementary output), 2 basic timers, 2 watchdog timers, 1 low power timer
- GPIO:

  Up to 140 GPIO, up to 108MHz
- Compatible with STM32F407 /STM32F429
- High-speed interface
  - USB 2.0 FS with built-in PHY
  - USB 2.0 HS with ULPI support
  - 10/100 Ethernet port, independent DMA, support MII/RMII
- High-performance simulation
  - 3x12bit,1.5M ADC, up to 24CH
  - 2x12bit DAC
  - Built-in temperature sensor

- 128-bit unique ID
- Debug: SWD/JTAG

- Power consumption
  - Current <270mA in operating mode
- ESD: HBM2000V
- Package:
  - LQFP100, LQFP144, LQFP176
- -PBGA176
  - CQFP144, CQFP176
- Quality Grade:
  - Industrial grade (working temperature -40 ℃ ~ 85 ℃)
  - Military temperature grade (operating temperature -55 ℃ ~125 ℃)
  - N1 level (operating temperature -55 ℃ ~ 125 ℃)
  - Class B (operating temperature -55 ℃ ~125 ℃)

## II. Product Introduction

The BST32F 4 series products are based on a high-performance 32-bit RISC core with a typical operating frequency of 180 MHz . They integrate single and double-precision floating-point units, a memory protection unit (MPU), support single and double-precision data processing instructions and data types, and support DSP instructions.

BST32F 4 series products have built-in 2M FLASH, 512K SRAM, including 128KB DTCM; 16K ITCM, 4KB Backup SRAM can be powered by VBAT to maintain data. The bus matrix

supports multiple bus devices to access the memory at the same time, and supports access to internal and external storage.

The BST32F 4 series products integrate a wealth of peripherals, including 3 independent 12-bit 1.5M ADCs, 2 independent 12-bit DACs, one USB FS/HS, 1 Ethernet interface, 1 SDIO, 1 MDIO, 1 QSPI, 4 USARTs, 4 UARTs, 6 SPIs, 4 I 2 Cs, 3 CAN controllers, up to 18 timers, including 2 advanced timers, each supporting 3-way PWM output.

The BST32F 4 series products support wide voltage (2.1V ~ 3.6V), wide temperature (-55 ℃ ~ 125 ℃) and various low power modes.

## III. Typical applications :

The BST32F4 series products are available in 100 PIN, 1 44 PIN, 1 76 PIN LQFP/ CQFP packages and 1 76 PIN P BGA packages. The package pins are compatible with STM32F407/429 and are suitable for high-performance control applications.

## IV. Model naming rules

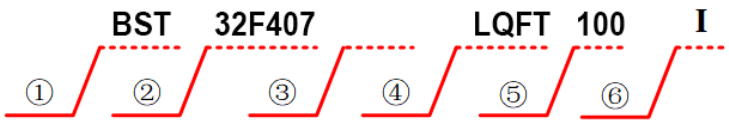


Figure 1 -1Model naming rules

- BST representative products are products developed by BEST
- 32F407 represents the product model
- Version ID (None: indicates the first version of the product series)
- Package
- PIN Number

- Grade: Commercial Grade C, Industrial Grade I, Wide Temperature W, Military Temperature E, Military Grade M (M 1: B Grade, M 3: N1 Grade)

For more information on product grades, please contact your local sales representative

## V. Model function comparison table

| FUNCTION ITEMS | | 100PIN | 144PIN | 176PIN |
|---|---|---|---|---|
| CPU MAXIMUM OPERATING FREQUENCY | | 180 M | | |
| L1 CACHE | | 16K+16K | | |
| OPERATING VOLTAGE | | 2.1v~3.6v | | |
| OPERATING TEMPERATURE | | -55 ℃ ~125 ℃(military temperature / N1)<br>-40 ℃ ~ 85 ℃ (Industrial) | | |
| GPIO | | 82 | 114 | 140 |
| FLASH(KB) | | 2048 | | |
| SRAM(KB) | SYSTEM | 512(128K DTCM) | | |
| | INSTRUCTION | 16 ITCM | | |
| | BACKUP | 4 | | |
| FMC | | 1 | | |
| TIMER | GENERAL PURPOSE TIMER | 10 | | |
| | ADVANCED TIMER | 2 | | |
| | BASIC TIMER | 2 | | |
| ETHERNET | | 1 | | |
| | SPI | 6 | | |

| | | |
|---|---|---|
| | I2C | 4 |
| | USART/UART | 4/4 |
| | USB OTG FS | |

COMMUNICATION

INTERFACE

# VII. Product Pin Information

## 7.1. Package Pin Diagram

### 7.1.1. LQFP100 package

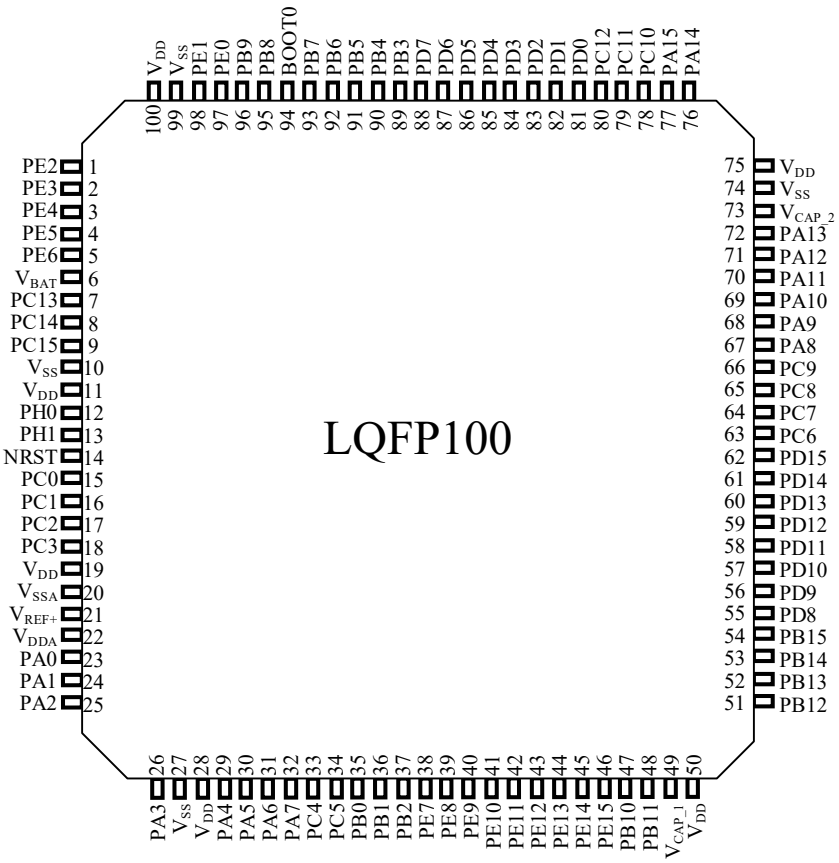


Figure 2 -1. BST32F 4 07 L QFP100 pin arrangement pin definition

### 7.1.2. LQFP144 package

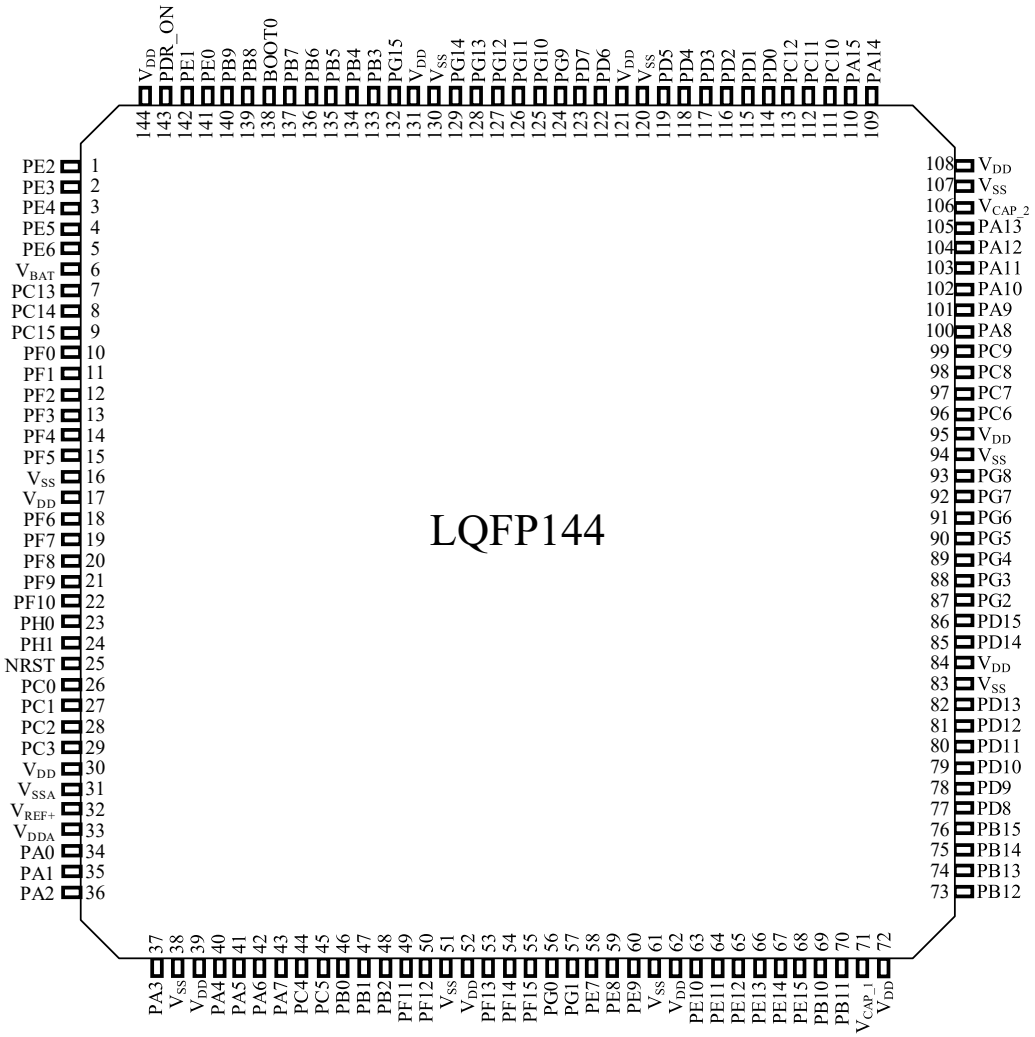


Figure 2 -2. BST32F 4 07 L QFP144 pin arrangement pin definition

### 7.1.3. LQFP176 package

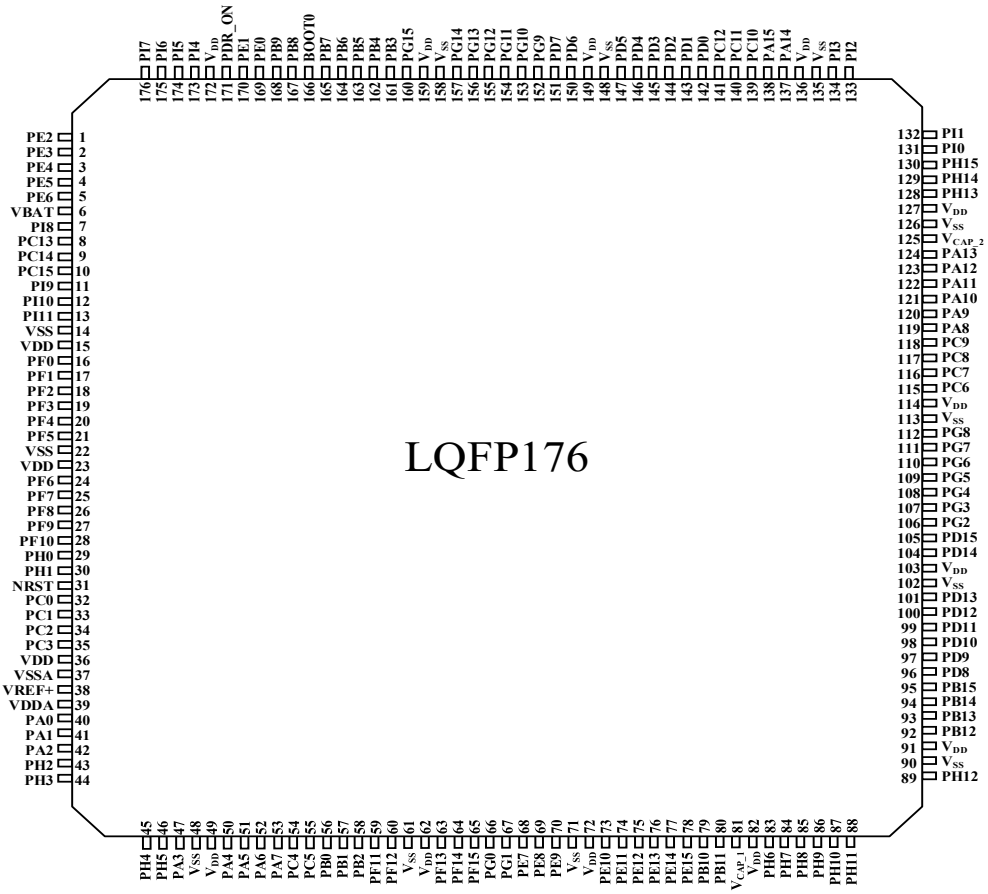


Figure 2 -3. BST32F 4 07 L QFP 176 pin arrangement pin definition

### 7.1.4. PBGA 1 76 package

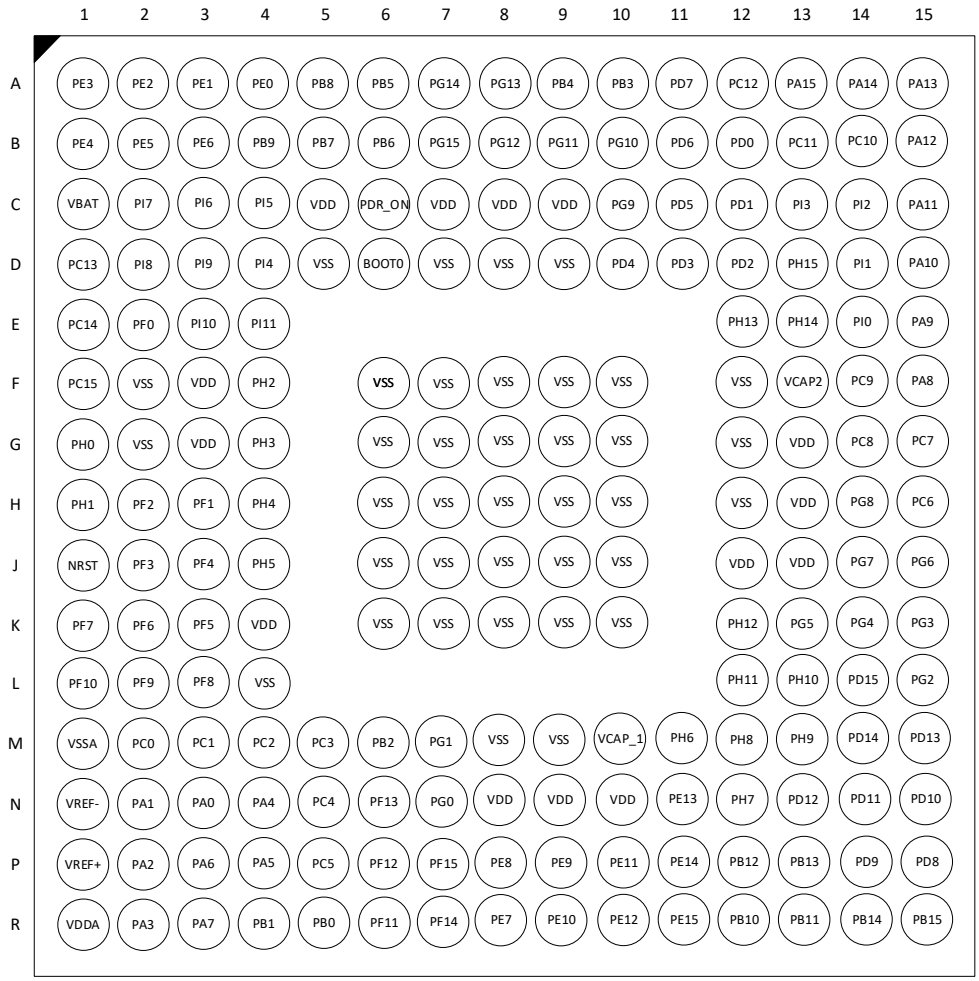


Figure 2 -4 BST32F 4 07 PBGA176 pin arrangement and pin definition

### 7.2. Pin function assignment table

#### 7.2.1. Package pin and solder ball function definition

| LQFP 100 | LQFP 144 | LQFP 176 | PBG A176 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | A2 | PE2 | I/O | FT | TRACECLK , SPI4_SCK , FMC_A23 , SAI1_MCLK_A, QUADSPI_BK1_IO2, ETH_MII_TXD3 , EVENTOUT | ANA_VC4_AIN P4 |
| 2 | 2 | 2 | A1 | PE3 | I/O | FT | TRACED0 , FMC_A19 , EVENTOUT , SAI1_SD_B | |
| 3 | 3 | 3 | B1 | PE4 | I/O | FT | TRACED1 , SPI4_NSS , FMC_A20 , EVENTOUT , SAI1_FS_A | ANA_VC2_AIN P5 |
| 4 | 4 | 4 | B2 | PE5 | I/O | FT | TRACED2 , TIM9_CH1 , SPI4_MISO , FMC_A21 , EVENTOUT , SAI1_SCK_A | |
| 5 | 5 | 5 | B3 | PE6 | I/O | FT | TRACED3 , TIM1_BKIN2 , TIM9_CH2 , SPI4_MOSI , FMC_A22 , EVENTOUT , SAI1_SD_A, SAI2_MCLK_B | |
| 6 | 6 | 6 | C1 | VBAT | S | - | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| - | - | 7 | D2 | PI8 | I/O | FT | EVENTOUT | RTC_TAMP2 , RTC_TS , WKUP5 |
| 7 | 7 | 8 | D1 | PC13 | I/O | FT | EVENTOUT | RTC_TAMP1 , RTC_TS , RTC_OUT, WKUP4 |
| 8 | 8 | 9 | E1 | PC14(OSC32_IN) | I/O | FT | EVENTOUT | OSC32_IN |

| LQFP100 | LQFP144 | LQFP176 | PBGA176 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 9 | 9 | 10 | F1 | PC15 (OSC32_OUT) | I/O | FT | EVENTOUT | OSC32_OUT |
| - | - | 11 | D3 | PI9 | I/O | FT | UART4_RX, CAN1_RX , FMC_D30 , EVENTOUT | ANA_VC2_AINP6 |
| - | - | 12 | E3 | PI10 | I/O | FT | ETH_MII_RX_ER , FMC_D31 , EVENTOUT | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| - | - | 13 | E4 | PI11 | I/O | FT | OTG_HS_ULPI_DIR , EVENTOUT | WKUP6 |
| - | - | 14 | F2 | VSS | S | - | | |
| - | - | 15 | F3 | VDD | S | - | | |
| - | 10 | 16 | E2 | PF0 | I/O | FT | I2C2_SDA , FMC_A0 , EVENTOUT | |
| - | 11 | 17 | H3 | PF1 | I/O | FT | I2C2_SCL , FMC_A1 , EVENTOUT | ANA_VC2_AINP7 |
| - | 12 | 18 | H2 | PF2 | I/O | FT | I2C2_SMBA , FMC_A2 , EVENTOUT | |
| - | 13 | 19 | J2 | PF3 | I/O | FT | FMC_A3 , EVENTOUT | ADC3_IN9 |
| - | 14 | 20 | J3 | PF4 | I/O | FT | FMC_A4 , EVENTOUT | ADC3_IN14 |
| - | 15 | 21 | K3 | PF5 | I/O | FT | FMC_A5 , EVENTOUT | ADC3_IN15 |
| 10 | 16 | 22 | G2 | VSS | S | - | | |
| 11 | 17 | 23 | G3 | VDD | S | - | | |
| - | 18 | 24 | K2 | PF6 | I/O | FT | TIM10_CH1 , SPI5_NSS , UART7_Rx , SAI1_SD_B, QUADSPI_BK1_IO3, EVENTOUT | ADC3_IN4 |

| LQFP 100 | LQFP 144 | LQFP 176 | PBGA 176 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|
| - | 19 | 25 | K1 | PF7 | I/O | FT | TIM11_CH1 , SPI5_SCK , UART7_TX , SAI1_MCLK_B, QUADSPI_BK1_IO2 , EVENTOUT | ADC3_IN5 |
| - | 20 | 26 | L3 | PF8 | I/O | FT | SPI5_MISO , UART7_RTS, TIM13_CH1 , SAI1_SCK_B, QUADSPI_BK1_IO0, EVENTOUT | ADC3_IN6 |
| - | 21 | 27 | L2 | PF9 | I/O | FT | SPI5_MOSI, UART7_CTS, TIM14_CH1, SAI1_FS_B, QUADSPI_BK1_IO1, EVENTOUT | ADC3_IN7 |
| - | 22 | 28 | L1 | PF10 | I/O | FT | QUADSPI_CLK、EVENTOUT | ADC3_IN8 |
| 12 | 23 | 29 | G1 | PH0(OSC_IN) | I/O | FT | EVENTOUT | OSC_IN |
| 13 | 24 | 30 | H1 | PH1(OSC_OUT) | I/O | FT | EVENTOUT | OSC_OUT |
| 14 | 25 | 31 | J1 | NRST | I/O | RST | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 15 | 26 | 32 | M2 | PC0 | I/O | FT | OTG_HS_ULPI_STP, FMC_SDNWE, EVENTOUT, SAI2_FS_B | ADC1_IN10 , ADC2_IN10 , ADC3_IN10 |
| 16 | 27 | 33 | M3 | PC1 | I/O | FT | TRACED0, SPI2_MOSI/I2S2_SD, ETH_MDC, MDIOS_MDC, EVENTOUT, SAI1_SD_A | ADC1_IN11 , ADC2_IN11 , ADC3_IN11 RTC_TAMP3, WKUP3 |
| 17 | 28 | 34 | M4 | PC2 | I/O | FT | SPI2_MISO, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT | ADC1_IN12 , ADC2_IN12 , ADC3_IN12 |

| LQFP100 | LQFP144 | LQFP176 | PBGA176 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | ANA_VC3_AINP0 |
| 18 | 29 | 35 | M5 | PC3 | I/O | FT | SPI2_MOSI/I2S2_SD, EVENTOUT, FMC_SDCKE0, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, | ADC1_IN13 , ADC2_IN13 , ADC3_IN13 ANA_VC3_AINN0 |
| 19 | 30 | 36 | | VDD | S | - | | |
| 20 | 31 | 37 | M1 | VSSA | S | - | | |
| | | | N1 | VREF- | S | | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 21 | 32 | 38 | P1 | VREF+ | S | - | | |
| 22 | 33 | 39 | R1 | VDDA | S | - | | |
| 23 | 34 | 40 | N3 | PA0-WKUP | I/O | FT | TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, USART2_CTS, UART4_TX, ETH_MII_CRS, EVENTOUT, SAI2_SD_B | ADC1_IN0 , ADC2_IN0 , ADC3_IN0 , WKUP 1 |
| 24 | 35 | 41 | N2 | PA1 | I/O | FT | TIM2_CH2, TIM5_CH2, USART2_RTS, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCLK_B, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, EVENTOUT | ADC1_IN1 , ADC2_IN1 , ADC3_IN1 |
| 25 | 36 | 42 | P2 | PA2 | I/O | FT | TIM2_CH3, TIM5_CH3, TIM9_CH1, USART2_TX, ETH_MDIO, MDIOS_MDIO, EVENTOUT, SAI2_SCK_B | ADC1_IN2 , ADC2_IN2 , ADC3_IN2 , WKUP2 |

| LQFP100 | LQFP 144 | LQFP 176 | PBGA 176 | DEFAULT FUNCTION AFTER | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| - | - | 43 | F4 | PH2 | I/O | FT | LPTIM1_IN2, QUADSPI_BK2_IO0, ETH_MII_CRS, FMC_SDCKE0, EVENTOUT, SAI2_SCK_B | |
| - | - | 44 | G4 | PH3 | I/O | FT | QUADSPI_BK2_IO1, ETH_MII_COL, FMC_SDNE0, EVENTOUT, SAI2_MCLK_B | |
| - | - | 45 | H4 | PH4 | I/O | FT | I2C2_SCL , OTG_HS_ULPI_NXT , EVENTOUT | |
| - | - | 46 | J4 | PH5 | I/O | FT | I2C2_SDA , SPI5_NSS , FMC_SDNWE , EVENTOUT | |
| 26 | 37 | 47 | R2 | PA3 | I/O | FT | TIM2_CH4 , TIM5_CH4 , TIM9_CH2 , USART2_RX , OTG_HS_ULPI_D0 , ETH_MII_COL , EVENTOUT | ADC1_IN3 , ADC2_IN3 , ADC3_IN3 |
| 27 | 38 | 48 | L4 | VSS | S | - | | |
| 28 | 39 | 49 | K4 | VDD | S | - | | |
| 29 | 40 | 50 | N4 | PA4 | I/O | TTa | SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS, OTG_HS_SOF, EVENTOUT | ADC1_IN4 , ADC2_IN4 , DAC_OUT1 |
| 30 | 41 | 51 | P4 | PA5 | I/O | TTa | TIM2_CH1/TIM2_ETR, EVENTOUT, TIM8_CH1N, SPI1_SCK/I2S1_CK, SPI6_SCK, OTG_HS_ULPI_CK | ADC1_IN5 , ADC2_IN5 , DAC_OUT2 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 31 | 42 | 52 | P3 | PA6 | I/O | FT | TIM1_BKIN , TIM3_CH1 , TIM8_BKIN , SPI1_MISO , SPI6_MISO, TIM13_CH1, MDIOS_MDC, EVENTOUT | ADC1_IN6 , ADC2_IN6 |
| 32 | 43 | 53 | R3 | PA7 | I/O | FT | TIM1_CH1N, TIM3_CH2, TIM8_CH1N, FMC_SDNWE, SPI1_MOSI/I2S1_SD, SPI6_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, EVENTOUT | ADC1_IN7 , ADC2_IN7 |

| LQFP100 | LQFP144 | LQFP176 | PBGA176 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 33 | 44 | 54 | N5 | PC4 | I/O | FT | I2S1_MCK, SPDIF_RX2, FMC_SDNE0, ETH_MII_RXD0/ETH_RMII_RXD0 , EVENTOUT | ADC1_IN14 , ADC2_IN14 ANA_VC1/2/3_AINP1 |
| 34 | 45 | 55 | P5 | PC5 | I/O | FT | SPDIF_RX3, ETH_MII_RXD1/ETH_RMII_RXD1 , EVENTOUT | ADC1_IN15 , ADC2_IN15 ANA_VC1/2/3_AINN1 |
| - | - | - | - | VDD | S | - | - | - |
| - | - | - | - | V SS | S | - | - | - |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 35 | 46 | 56 | R5 | PB0 | I/O | FT | TIM1_CH2N, TIM3_CH3, TIM8_CH2N, UART4_CTS, OTG_HS_ULPI_D1, ETH_MII_RXD2, EVENTOUT | ADC1_IN8, ADC2_IN8, ANA_VC1/2/4_AINP0 |
| 36 | 47 | 57 | R4 | PB1 | I/O | FT | TIM1_CH3N, TIM3_CH4, TIM8_CH3N, OTG_HS_ULPI_D2, ETH_MII_RXD3, EVENTOUT | ADC1_IN9, ADC2_IN9, ANA_VC1/2/4_AINN0 |
| 37 | 48 | 58 | M6 | PB2 ( BOOT1) | I/O | FT | SPI3_MOSI/I2S3_SD, QUADSPI_CLK, , EVENTOUT | ANA_VC1/2/3/4_AINP2 |
| | | | | P I15 | I/O | FT | EVENTOUT | |
| | | | | P J0 | I/O | FT | EVENTOUT | |
| | | | | P J1 | I/O | FT | EVENTOUT | |
| | | | | P J2 | I/O | FT | EVENTOUT | |
| LQFP100 | LQFP144 | LQFP176 | PBGA176 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
| | | | | P J3 | I/O | FT | EVENTOUT | |
| | | | | P J4 | I/O | FT | EVENTOUT | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| - | 49 | 59 | R6 | PF11 | I/O | FT | SPI5_MOSI , SAI2_SD_B , FMC_SDNRAS , EVENTOUT | |
| - | 50 | 60 | P6 | PF12 | I/O | FT | FMC_A6 , EVENTOUT | |
| - | 51 | 61 | M8 | VSS | S | - | | |
| - | 52 | 62 | N8 | VDD | S | - | | |
| - | 53 | 63 | N6 | PF13 | I/O | FT | FMC_A7 , EVENTOUT | |
| - | 54 | 64 | R7 | PF14 | I/O | FT | I2C4_SCL , FMC_A8 , EVENTOUT | |
| - | 55 | 65 | P7 | PF15 | I/O | FT | I2C4_SDA , FMC_A9 , EVENTOUT | |
| - | 56 | 66 | N7 | PG0 | I/O | FT | FMC_A10 , EVENTOUT | |
| - | 57 | 67 | M7 | PG1 | I/O | FT | FMC_A11 , EVENTOUT | |
| 38 | 58 | 68 | R8 | PE7 | I/O | FT | TIM1_ETR , UART7_Rx , QUADSPI_BK2_IO0, FMC_D4 , EVENTOUT | ANA_VC1/2/3/4_AINN2 |
| 39 | 59 | 69 | P8 | PE8 | I/O | FT | TIM1_CH1N, UART7_Tx, QUADSPI_BK2_IO1, FMC_D5, EVENTOUT | |
| 40 | 60 | 70 | P9 | PE9 | I/O | FT | TIM1_CH1, UART7_RTS, QUADSPI_BK2_IO2,, FMC_D6, EVENTOUT | ANA_VC1/2/3/4_AINP3 |

| - | 61 | 71 | M9 | VSS | S | - | | |
|---|---|---|---|---|---|---|---|---|
| LQFP100 | LQFP144 | LQFP176 | PBGA 176 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
| - | 62 | 72 | N9 | VDD | S | - | | |
| 41 | 63 | 73 | R9 | PE10 | I/O | FT | TIM1_CH2N, UART7_CTS, QUADSPI_BK2_IO3, FMC_D7, EVENTOUT | ANA_VC1/2/3/4_AINN3 |
| 42 | 64 | 74 | P10 | PE11 | I/O | FT | TIM1_CH2, SPI4_NSS, FMC_D8, EVENTOUT, SAI2_SD_B | ANA_VC1/2/3_AINP4 |
| 43 | 65 | 75 | R10 | PE12 | I/O | FT | TIM1_CH3N, SPI4_SCK, FMC_D9, EVENTOUT, SAI2_SCK_B | |
| 44 | 66 | 76 | N11 | PE13 | I/O | FT | TIM1_CH3, SPI4_MISO, FMC_D10, EVENTOUT, SAI2_FS_B | |
| 45 | 67 | 77 | P11 | PE14 | I/O | FT | TIM1_CH4, SPI4_MOSI, FMC_D11, EVENTOUT, SAI2_MCLK_B | |
| 46 | 68 | 78 | R11 | PE15 | I/O | FT | TIM1_BKIN , FMC_D12 , EVENTOUT | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 47 | 69 | 79 | R12 | PB10 | I/O | FT | TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, USART3_TX, QUADSPI_BK1_NCS, OTG_HS_ULPI_D3, ETH_MII_RX_ER, EVENTOUT | |
| 48 | 70 | 80 | R13 | PB11 | I/O | FT | TIM2_CH4 , I2C2_SDA , USART3_RX , OTG_HS_ULPI_D4 , ETH_MII_TX_EN/ETH_RMII_TX_EN , EVENTOUT | |
| 49 | 71 | 81 | M10 | VCAP_1 | S | - | - | - |
| - | - | - | - | V SS | S | - | - | - |
| 50 | 72 | 82 | N10 | VDD | S | - | - - | - |

| LQFP100 | LQFP144 | LQFP176 | PBGA176 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|
| - | - | - | - | PJ5 | I/O | FT | EVENTOUT | - |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| - | - | 83 | M11 | PH6 | I/O | FT | I2C2_SMBA , SPI5_SCK , TIM12_CH1 , ETH_MII_RXD2 , FMC_SDNE1 , EVENTOUT | |
| - | - | 84 | N12 | PH7 | I/O | FT | I2C3_SCL , SPI5_MISO , ETH_MII_RXD3 , FMC_SDCKE1 , EVENTOUT | ANA_VC1_AIN P5 |
| - | - | 85 | M12 | PH8 | I/O | FT | I2C3_SDA , FMC_D16 , EVENTOUT | |
| - | - | 86 | M13 | PH9 | I/O | FT | I2C3_SMBA , TIM12_CH2 , FMC_D17 , EVENTOUT | |
| - | - | 87 | L13 | PH10 | I/O | FT | I2C4_SMBA , TIM5_CH1 , FMC_D18 , EVENTOUT | |
| - | - | 88 | L12 | PH11 | I/O | FT | I2C4_SCL , TIM5_CH2 , FMC_D19 , EVENTOUT | ANA_VC1_AIN P6 |
| - | - | 89 | K12 | PH12 | I/O | FT | I2C4_SDA , TIM5_CH3 , FMC_D20 , EVENTOUT | |
| - | - | 90 | H12 | VSS | S | - | | |
| - | - | 91 | J12 | VDD | S | - | | |
| 51 | 73 | 92 | P12 | PB12 | I/O | FT | TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, USART3_CK, UART5_RX, CAN2_RX, OTG_HS_ID OTG_HS_ULPI_D5, EVENTOUT,ETH_MII_TXD0/ETH_RMII_TXD0, EVENTOUT | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 52 | 74 | 93 | P13 | PB13 | I/O | FT | TIM1_CH1N, SPI2_SCK/I2S2_CK, USART3_CTS, UART5_TX, CAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, EVENTOUT | OTG_HS_VBUS |

| LQFP100 | LQFP144 | LQFP176 | PBGA176 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 53 | 75 | 94 | R14 | PB14 | I/O | FT | TIM1_CH2N, TIM8_CH2N, USART1_TX, SPI2_MISO, USART3_RTS, UART4_RTS, TIM12_CH1, SDMMC2_D0, OTG_HS_DM, EVENTOUT | |
| 54 | 76 | 95 | R15 | PB15 | I/O | FT | RTC_REFIN, TIM1_CH3N, TIM8_CH3N, USART1_RX, SPI2_MOSI/I2S2_SD, UART4_CTS, TIM12_CH2, SDMMC2_D1, OTG_HS_DP, EVENTOUT | ANA_VC1_AINP7 |
| 55 | 77 | 96 | P15 | PD8 | I/O | FT | USART3_TX, SPDIF_RX1,, FMC_D13, EVENTOUT | ANA_VC3_AINP5 |
| 56 | 78 | 97 | P14 | PD9 | I/O | FT | USART3_RX , FMC_D14 , EVENTOUT | |
| 57 | 79 | 98 | N15 | PD10 | I/O | FT | USART3_CK , FMC_D15 , EVENTOUT , | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 58 | 80 | 99 | N14 | PD11 | I/O | FT | I2C4_SMBA, USART3_CTS, QUADSPI_BK1_IO0, FMC_A16/FMC_CLE, EVENTOUT, SAI2_SD_A | ANA_VC3_AINP6 |
| 59 | 81 | 100 | N13 | PD12 | I/O | FT | TIM4_CH1, LPTIM1_IN1, I2C4_SCL, USART3_RTS, QUADSPI_BK1_IO1, FMC_A17/FMC_ALE, EVENTOUT, SAI2_FS_A | |
| 60 | 82 | 101 | M15 | PD13 | I/O | FT | TIM4_CH2, LPTIM1_OUT, I2C4_SDA, FMC_A18, QUADSPI_BK1_IO3, EVENTOUT, SAI2_SCK_A | ANA_VC3_AINP7 |
| - | 83 | 102 | | VSS | S | - | | |
| - | 84 | 103 | J13 | VDD | S | - | | |
| 61 | 85 | 104 | M14 | PD14 | I/O | FT | TIM4_CH3, UART8_CTS, FMC_D0, EVENTOUT | |

| LQFP100 | LQFP144 | LQFP176 | PBGA176 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 53 | 75 | 94 | R14 | PB14 | I/O | FT | TIM1_CH2N, TIM8_CH2N, USART1_TX, SPI2_MISO, USART3_RTS, UART4_RTS, TIM12_CH1, SDMMC2_D0, OTG_HS_DM, EVENTOUT | |
| 54 | 76 | 95 | R15 | PB15 | I/O | FT | RTC_REFIN, TIM1_CH3N, TIM8_CH3N, USART1_RX, SPI2_MOSI/I2S2_SD, UART4_CTS, TIM12_CH2, SDMMC2_D1, OTG_HS_DP, EVENTOUT | ANA_VC1_AINP7 |
| 55 | 77 | 96 | P15 | PD8 | I/O | FT | USART3_TX, SPDIF_RX1,, FMC_D13, EVENTOUT | ANA_VC3_AINP5 |
| 56 | 78 | 97 | P14 | PD9 | I/O | FT | USART3_RX , FMC_D14 , EVENTOUT | |
| 57 | 79 | 98 | N15 | PD10 | I/O | FT | USART3_CK , FMC_D15 , EVENTOUT , | |
| 58 | 80 | 99 | N14 | PD11 | I/O | FT | I2C4_SMBA, USART3_CTS, QUADSPI_BK1_IO0, FMC_A16/FMC_CLE, EVENTOUT, SAI2_SD_A | ANA_VC3_AINP6 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 59 | 81 | 100 | N13 | PD12 | I/O | FT | TIM4_CH1, LPTIM1_IN1, I2C4_SCL, USART3_RTS, QUADSPI_BK1_IO1, FMC_A17/FMC_ALE, EVENTOUT, SAI2_FS_A | |
| 60 | 82 | 101 | M15 | PD13 | I/O | FT | TIM4_CH2, LPTIM1_OUT, I2C4_SDA, FMC_A18, QUADSPI_BK1_IO3, EVENTOUT, SAI2_SCK_A | ANA_VC3_ AINP7 |
| - | 83 | 102 | | VSS | S | - | | |
| - | 84 | 103 | J13 | VDD | S | - | | |
| 61 | 85 | 104 | M14 | PD14 | I/O | FT | TIM4_CH3, UART8_CTS, FMC_D0, EVENTOUT | |

| LQFP100 | LQFP144 | LQFP176 | PBGA176 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 62 | 86 | 105 | L14 | PD15 | I/O | FT | TIM4_CH4, UART8_RTS, FMC_D1, EVENTOUT | - |
| - | - | - | - | P J6 | I/O | FT | EVENTOUT | - |
| - | - | - | - | J7 | I/O | FT | EVENTOUT | - |
| - | - | - | - | P J8 | I/O | FT | EVENTOUT | - |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| - | - | - | - | P J9 | I/O | FT | EVENTOUT | - |
| - | - | - | - | P J10 | I/O | FT | EVENTOUT | - |
| - | - | - | - | P J11 | I/O | FT | EVENTOUT | - |
| - | - | - | - | VDD | S | - | - | - |
| - | - | - | - | V SS | S | - | - | - |
| - | - | - | - | P K | I/O | FT | EVENTOUT | - |
| - | - | - | | P K1 | I/O | FT | EVENTOUT | - |
| - | - | - | | P K2 | I/O | FT | EVENTOUT | - |
| - | 87 | 106 | L15 | PG2 | I/O | FT | FMC_A12 , EVENTOUT | |
| - | 88 | 107 | K15 | PG3 | I/O | FT | FMC_A13 , EVENTOUT | |
| - | 89 | 108 | K14 | PG4 | I/O | FT | FMC_A14/FMC_BA0 , EVENTOUT | |
| - | 90 | 109 | K13 | PG5 | I/O | FT | FMC_A15/FMC_BA1 , EVENTOUT | |
| LQFP100 | LQFP144 | LQFP176 | PBGA176 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| - | 91 | 110 | J15 | PG6 | I/O | FT | FMC_NE3, EVENTOUT | |
| - | 92 | 111 | J14 | PG7 | I/O | FT | USART6_CK , FMC_INT3 , EVENTOUT | |
| - | 93 | 112 | H14 | PG8 | I/O | FT | SPI6_NSS, SPDIF_RX2, USART6_RTS, ETH_PPS_OUT, FMC_SDCLK, EVENTOUT | |
| - | 94 | 113 | G12 | VSS | S | - | | |
| - | 95 | 114 | H13 | VDD | S | - | | |
| 63 | 96 | 115 | H15 | PC6 | I/O | FT | TIM3_CH1, TIM8_CH1, USART6_TX, FMC_NWAIT, SDMMC2_D6, SDMMC1_D6, EVENTOUT, I2S2_MCK | |
| 64 | 97 | 116 | G15 | PC7 | I/O | FT | TIM3_CH2, TIM8_CH2, I2S3_MCK, USART6_RX, FMC_NE1, SDMMC2_D7, SDMMC1_D7, EVENTOUT | |
| 65 | 98 | 117 | G14 | PC8 | I/O | FT | TRACED1, TIM3_CH3, TIM8_CH3, UART5_RTS, USART6_CK, FMC_NE2/FMC_NCE, SDMMC1_D0, EVENTOUT | ANA_VC4_AINP1 |
| 66 | 99 | 118 | F14 | PC9 | I/O | FT | MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, UART5_CTS, QUADSPI_BK1_IO0, SDMMC1_D1, I2S_CKIN, EVENTOUT | ANA_VC4_AINN1 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 67 | 100 | 119 | F15 | PA8 | I/O | FT | MCO1, TIM1_CH1, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, CAN3_RX, UART7_RX, EVENTOUT | |
| 68 | 101 | 120 | E15 | PA9 | I/O | FT | TIM1_CH2, I2C3_SMBA, SPI2_SCK/I2S2_CK, | OTG_FS_VBUS |

| LQFP100 | LQFP144 | LQFP176 | PBGA176 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | USART1_TX , EVENTOUT | |
| 69 | 102 | 121 | D15 | PA10 | I/O | FT | IM1_CH3, USART1_RX, OTG_FS_ ID, MDIOS_MDIO, EVENTOUT | |
| 70 | 103 | 122 | C15 | PA11 | I/O | TTa | TIM1_CH4, SPI2_NSS/I2S2_WS, UART4_RX, USART1_CTS, CAN1_RX, OTG_FS_DM, EVENTOUT | |
| 71 | 104 | 123 | B15 | PA12 | I/O | TTa | TIM1_ETR, SPI2_SCK/I2S2_CK, UART4_TX, USART1_RTS, CAN1_TX, OTG_FS_DP, EVENTOUT, SAI2_FS_B | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 72 | 105 | 124 | A15 | PA13(JTMS-SWDIO) | I/O | FT | JTMSSWDIO , EVENTOUT | |
| 73 | 106 | 125 | F13 | VCAP_2 | S | - | | |
| 74 | 107 | 126 | F12 | VSS | S | - | | |
| 75 | 108 | 127 | G13 | VDD | S | - | | |
| - | - | 128 | E12 | PH13 | I/O | FT | TIM8_CH1N, UART4_TX, CAN1_TX, FMC_D21, EVENTOUT | |
| - | - | 129 | E13 | PH14 | I/O | FT | TIM8_CH2N, UART4_RX, CAN1_RX, FMC_D22, EVENTOUT | |
| - | - | 130 | D13 | PH15 | I/O | FT | TIM8_CH3N , FMC_D23 , EVENTOUT | |
| | | | | | | | | |

| LQFP100 | LQFP144 | LQFP176 | BGA176 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|
| - | - | 131 | E14 | PI0 | I/O | FT | TIM5_CH4, SPI2_NSS/I2S2_WS, FMC_D24, EVENTOUT | |
| - | - | 132 | D14 | PI1 | I/O | FT | TIM8_BKIN2, SPI2_SCK/I2S2_CK, FMC_D25, EVENTOUT | |
| - | - | 133 | C14 | PI2 | I/O | FT | TIM8_CH4 , SPI2_MISO , FMC_D26 , EVENTOUT | |
| - | - | 134 | C13 | PI3 | I/O | FT | TIM8_ETR, SPI2_MOSI/I2S2_SD, FMC_D27, EVENTOUT | |
| - | - | 135 | D9 | VSS | S | - | | |
| - | - | 136 | C9 | VDD | S | - | | |
| 76 | 109 | 137 | A14 | PA14(JTCK-SWCLK) | I/O | FT | JTCKSWCLK , EVENTOUT | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 77 | 110 | 138 | A13 | PA15(JTDI) | I/O | FT | JTDI, TIM2_CH1/TIM2_ETR, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI6_NSS, UART4_RTS, CAN3_TX, UART7_TX, EVENTOUT | |
| 78 | 111 | 139 | B14 | PC10 | I/O | FT | SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDMMC1_D2, EVENTOUT | |
| 79 | 112 | 140 | B13 | PC11 | I/O | FT | SPI3_MISO, USART3_RX, UART4_RX, SDMMC1_D3, QUADSPI_BK2_NCS, EVENTOUT | |
| 80 | 113 | 141 | A12 | PC12 | I/O | FT | TRACED3, SPI3_MOSI/I2S3_SD, USART3_CK, UART5_TX, SDMMC1_CK, EVENTOUT | |
| 81 | 114 | 142 | B12 | PD0 | I/O | FT | UART4_RX, CAN1_RX , FMC_D2 , EVENTOUT | |
| 82 | 115 | 143 | C12 | PD1 | I/O | FT | UART4_TX , CAN1_TX , FMC_D3 , EVENTOUT | |

| LQFP100 | LQFP144 | LQFP176 | PBGA176 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 83 | 116 | 144 | D12 | PD2 | I/O | FT | TRACED2, TIM3_ETR, UART5_RX, SDMMC1_CMD, EVENTOUT | ANA_VC4_AINP6 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 84 | 117 | 145 | D11 | PD3 | I/O | FT | SPI2_SCK/I2S2_CK, USART2_CTS, FMC_CLK, EVENTOUT | |
| 85 | 118 | 146 | D10 | PD4 | I/O | FT | USART2_RTS , FMC_NOE , EVENTOUT | |
| 86 | 119 | 147 | C11 | PD5 | I/O | FT | USART2_TX , FMC_NWE , EVENTOUT | |
| - | 120 | 148 | D8 | VSS | S | - | | |
| - | 121 | 149 | C8 | VDD | S | - | | |
| 87 | 122 | 150 | B11 | PD6 | I/O | FT | SPI3_MOSI/I2S3_SD, SAI1_SD_A, USART2_RX, FMC_NWAIT, SDMMC2_CK, EVENTOUT | |
| 88 | 123 | 151 | A11 | PD7 | I/O | FT | SPI1_MOSI/I2S1_SD, USART2_CK, SPDIF_RX0, SDMMC2_CMD, FMC_NE1, EVENTOUT | |
| | | | | P J12 | I/O | FT | EVENTOUT | |
| | | | | P J13 | I/O | FT | EVENTOUT | ANA_VC4_AINP7 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | P J14 | I/O | FT | EVENTOUT | |
| | | | | P J15 | I/O | FT | EVENTOUT | |
| - | 124 | 152 | C10 | PG9 | I/O | FT | SPI1_MISO, SPDIF_RX3, USART6_RX, FMC_NE2, QUADSPI_BK2_IO2, SDMMC2_D0, FMC_NCE, SAI2_FS_B , EVENTOUT | |
| LQFP100 | LQFP144 | LQFP176 | PBGA176 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
| - | 125 | 153 | B10 | PG10 | I/O | FT | SPI1_NSS/I2S1_WS, SDMMC2_D1, SAI2_SD_B, FMC_NE3, EVENTOUT | |
| - | 126 | 154 | B9 | PG11 | I/O | FT | SPI1_SCK/I2S1_CK, SPDIF_RX0, SDMMC2_D2, ETH_MII_TX_EN/ETH_RMII_TX_EN, EVENTOUT | |
| - | 127 | 155 | B8 | PG12 | I/O | FT | LPTIM1_IN1, SPI6_MISO, SPDIF_RX1, USART6_RTS, SDMMC2_D3, FMC_NE4, EVENTOUT | |
| - | 128 | 156 | A8 | PG13 | I/O | FT | TRACED0,, LPTIM1_OUT, SPI6_SCK, USART6_CTS, EVENTOUT, ETH_MII_TXD0/ETH_RMII_TXD0, FMC_A24 | |
| - | 129 | 157 | A7 | PG14 | I/O | FT | TRACED1, LPTIM1_ETR, SPI6_MOSI, USART6_TX, QUADSPI_BK2_IO3, FMC_A25, ETH_MII_TXD1/ETH_RMII_TXD1, EVENTOUT | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| - | 130 | 158 | D7 | VSS | S | - | | |
| - | 131 | 159 | C7 | VDD | S | - | | |
| | | | | P K3 | I/O | FT | EVENTOUT | |
| | | | | P K4 | I/O | FT | EVENTOUT | |
| | | | | P K5 | I/O | FT | EVENTOUT | |
| | | | | P K6 | I/O | FT | EVENTOUT | |
| | | | | K7 | I/O | FT | EVENTOUT | |
| - | 132 | 160 | B7 | PG15 | I/O | FT | USART6_CTS , FMC_SDNCAS , EVENTOUT | |
| LQFP100 | LQFP144 | LQFP176 | PBGA176 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
| 89 | 133 | 161 | A10 | PB3(JTDO/TRACESWO) | I/O | FT | JTDO/TRACESWO, TIM2_CH2, SPI1_SCK/I2S1_CK, SPI6_SCK, SPI3_SCK/I2S3_CK, SDMMC2_D2, CAN3_RX, UART7_RX, EVENTOUT | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 90 | 134 | 162 | A9 | PB4(NJTRST) | I/O | FT | NJTRST, TIM3_CH1, SPI1_MISO, SPI3_MISO, EVENTOUT, SPI2_NSS/I2S2_WS, SPI6_MISO, SDMMC2_D3, CAN3_TX, UART7_TX | |
| 91 | 135 | 163 | A6 | PB5 | I/O | FT | UART5_RX, TIM3_CH2, I2C1_SMBA, CAN2_RX, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, FMC_SDCKE1, SPI6_MOSI, OTG_HS_ULPI_D7, ETH_PPS_OUT, EVENTOUT | |
| 92 | 136 | 164 | B6 | PB6 | I/O | FT | UART5_TX, TIM4_CH1, I2C1_SCL, USART1_TX, CAN2_TX, QUADSPI_BK1_NCS, I2C4_SCL, FMC_SDNE1, EVENTOUT | |
| 93 | 137 | 165 | B5 | PB7 | I/O | FT | I2C4_SDA , TIM4_CH2 , I2C1_SDA , USART1_RX , FMC_NL , EVENTOUT | |
| 94 | 138 | 166 | D6 | BOOT0 | I | B | | VPP |
| 95 | 139 | 167 | A5 | PB8 | I/O | FT | I2C4_SCL, TIM4_CH3, TIM10_CH1, I2C1_SCL, UART5_RX, CAN1_RX, SDMMC2_D4, ETH_MII_TXD3, SDMMC1_D4, EVENTOUT | |
| 96 | 140 | 168 | B4 | PB9 | I/O | FT | I2C4_SDA, TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, UART5_TX,, CAN1_TX, SDMMC2_D5, I2C4_SMBA, SDMMC1_D5, EVENTOUT | |

| LQFP100 | LQFP144 | LQFP176 | PBGA176 | DEFAULT FUNCTION AFTER RESET | PIN TYPE | I/O TYPE | DIGITAL FUNCTIONS | SIMULATION FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 97 | 141 | 169 | A4 | PE0 | I/O | FT | TIM4_ETR, LPTIM1_ETR, UART8_Rx, FMC_NBL0, EVENTOUT, SAI2_MCLK_A | |
| 98 | 142 | 170 | A3 | PE1 | I/O | FT | LPTIM1_IN2, UART8_TX, FMC_NBL1, EVENTOUT | |
| 99 | - | 171 | D5 | VSS | S | - | | |
| - | 143 | | C6 | PDR_ON | S | | | |
| 100 | 144 | 172 | C5 | VDD | S | - | | |
| - | - | 173 | D4 | PI4 | I/O | FT | TIM8_BKIN, FMC_NBL2, EVENTOUT, SAI2_MCLK_A | |
| - | - | 174 | C4 | PI5 | I/O | FT | TIM8_CH1 , FMC_NBL3 , EVENTOUT , SAI2_SCK_A | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| - | - | 175 | C3 | PI6 | I/O | FT | TIM8_CH2 , FMC_D28 , EVENTOUT , SAI2_SD_A | |
| - | - | 176 | C2 | PI7 | I/O | FT | TIM8_CH3 , FMC_D29 , EVENTOUT , SAI2_FS_A | |

### 7.2.2. Pin function multiplexing

| PORT | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PORT | | SYS | I2C4/UART5/TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1 | I2C1/2/3/4/USART1 | SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/5/6 | SPI2/I2S2/SPI3/I2S3/SAI1/I2C4/UART4 | SPI2/I2S2/SPI3/I2S3/SPI6/USART1/2/3/UART5 | SPI6/SAI2/USART6/UART4/5/7/8/OTG_FS | CAN1/2/TIM12/13/14/QUADSPI/FMC | SAI2/QUADSPI/SDMMC2/OTG2_HS/OTG1_FS | I2C4/CAN3/SDMMC2/ETH | UART7/FMC/SDMMC1/MDIOS/OTG2_FS | - | - | SYS |
| PA | PA0 | - | TIM2_CH1/TIM2 | TIM5_CH1 | TIM8_ETR | - | - | - | USART2_CTS | UART4_TX | - | SAI2_SD_B | ETH_MII_CRS | - | - | - | EVENTOUT |

| | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | _ETR | | | | | | | | | | | | | | |
| | PA1 | - | TIM2_CH2 | TIM5_CH2 | - | - | - | - | USART2_RTS | UART4_RX | QUADSPI_BK1_IO3 | SAI2_MCLK_B | ETH_MII_RX_CLK/ETH_RMII_REF_CLK | - | - | - | EVENTOU |
| | PA2 | - | TIM2_CH3 | TIM5_CH3 | TIM9_CH1 | - | - | - | USART2_TX | SAI2_SCK_B | - | - | ETH_MDIO | MDIOS_MDIO | - | - | EVENTOU |
| | PA3 | - | TIM2_CH4 | TIM5_CH4 | TIM9_CH2 | - | - | - | USART2_RX | - | - | OTG_HS_ULPI_D0 | ETH_MII_COL | - | - | - | EVENTOU |
| | PA4 | - | - | - | - | - | SPI1_NSS/I2S1_WS | SPI3_NSS/I2S3_WS | USART2_CK | SPI6_NSS | - | - | - | OTG_HS_SOF | - | - | EVENTOU |
| | PA5 | - | TIM2_CH1/TIM2_ETR | - | TIM8_CH1N | - | SPI1_SCK/I2S1_CK | - | - | SPI6_SCK | - | OTG_HS_ULPI_CK | - | - | - | - | EVENTOUT |

| | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PA6 | - | TIM1_BKIN_COMP0_OUT | TIM3_CH1 | TIM8_BKIN_COMP2_OUT | - | SPI1_MISO | - | - | SPI6_MISO | TIM13_CH1 | - | - | MDIOS_MDC | - | - | EVENTOUT |
| | PA7 | - | TIM1_CH1N | TIM3_CH2 | TIM8_CH1N | - | SPI1_MOSI/I2S1_SD | - | - | SPI6_MOSI | TIM14_CH1 | - | ETH_MII_RX_DV/ETH_RMII_CRS_DV | FMC_SDNWE | - | - | EVENTOU |
| | PA8 | MCO1 | TIM1_CH1 | - | TIM8_BKIN2_COMP | I2C3_SCL | - | - | USART1_CK | - | - | OTG_FS_SOF | CAN3_RX | UART7_RX | - | - | EVENTOU |
| | PA9 | - | TIM1_CH2 | - | - | I2C3_SMBA | SPI2_SCK/I2S2_CK | - | USART1_TX | - | - | - | - | - | - | - | EVENTOU |
| | PA10 | - | TIM1_CH3 | - | - | - | - | - | USART1_RX | - | - | OTG_FS_ID | - | MDIOS_MDIO | - | - | EVENTOU |

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PA11 | - | TIM1_CH4 | - | - | - | SPI2_NSS/I2S2_WS | UART4_RX | USART1_CTS | - | CAN1_RX | OTG_FS_DM | - | - | - | EVENTOU |
| | PA12 | - | TIM1_ETR | - | - | - | SPI2_SCK/I2S2_CK | UART4_TX | USART1_RTS | SAI2_FS_B | CAN1_TX | OTG_FS_DP | - | - | - | EVENTOU |
| | PA13 | JTMS-SWDIO | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PA14 | JTCK-SWCLK | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PA15 | JTDI | TIM2_CH1/TIM2_ETR | - | - | | SPI1_NSS/I2S1_WS | SPI3_NSS/I2S3_WS | SPI6_NSS | UART4_RTS | - | - | CAN3_TX | UART7_TX | - | EVENTOUT |
| PB | PB0 | - | TIM1_CH2N | TIM3_CH3 | TIM8_CH2N | - | - | | - | UART4_CTS | - | OTG_HS_ULPI_D1 | ETH_MII_RXD2 | - | - | EVENTOU |

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| | PB1 | - | TIM1_CH3N | TIM3_CH4 | TIM8_CH3N | - | - | | - | - | - | OTG_HS_ULPI_D2 | ETH_MII_RXD3 | - | - | - | EVENTOU |
| | PB2 | - | - | - | - | - | - | SAI1_SD_A | SPI3_MOSI/I2S3_SD | - | QUADSPI_CLK | | - | - | - | - | EVENTOU |
| | PB3 | JTDO/TRACESWO | TIM2_CH2 | - | - | - | SPI1_SCK/I2S1_CK | SPI3_SCK/I2S3_CK | - | SPI6_SCK | - | SDMMC2_D2 | CAN3_RX | UART7_RX | - | - | EVENTOU |
| | PB4 | NJTRST | - | TIM3_CH1 | - | - | SPI1_MISO | SPI3_MISO | SPI2_NSS/I2S2_WS | SPI6_MISO | - | SDMMC2_D3 | CAN3_TX | UART7_TX | - | - | EVENTOU |
| | PB5 | - | UART5_RX | TIM3_CH2 | - | I2C1_SMBA | SPI1_MOSI/I2S1_SD | SPI3_MOSI/I2S3_SD | - | SPI6_MOSI | CAN2_RX | OTG_HS_ULPI_D7 | ETH_PPS_OUT | FMC_SDCKE1 | - | - | EVENTOU |
| | PB6 | - | UART5_TX | TIM4_CH1 | - | I2C1_SCL | - | | USART1_TX | - | CAN2_TX | QUADSPI_BK1_NCS | I2C4_SCL | FMC_SDNE1 | - | - | EVENTOU |

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| | PB7 | - | - | TIM4_CH2 | - | I2C1_SDA | - | | USART1_RX | - | - | - | I2C4_SDA | FMC_NL | - | - | EVENTOU |
| | PB8 | - | I2C4_SCL | TIM4_CH3 | TIM10_CH1 | I2C1_SCL | - | | UART5_RX | - | CAN1_RX | SDMMC2_D4 | ETH_MII_TXD3 | SDMMC1_D4 | - | - | EVENTOU |
| | PB9 | - | I2C4_SDA | TIM4_CH4 | TIM11_CH1 | I2C1_SDA | SPI2_NSS/I2S2_WS | | UART5_TX | - | CAN1_TX | SDMMC2_D5 | I2C4_SMBA | SDMMC1_D5 | - | - | EVENTOU |
| | PB10 | - | TIM2_CH3 | - | - | I2C2_SCL | SPI2_SCK/I2S2_CK | | USART3_TX | - | QUADSPI_BK1_NCS | OTG_HS_ULPI_D3 | ETH_MII_RX_ER | - | - | - | EVENTOU |
| | PB11 | - | TIM2_CH4 | - | - | I2C2_SDA | - | | USART3_RX | - | - | OTG_HS_ULPI_D4 | ETH_MII_TX_EN/ETH_RMII_TX_EN | - | - | - | EVENTOU |
| | PB12 | - | TIM1_BKIN_COMP0_ | - | - | I2C2_SMBA | SPI2_NSS/I2S2_WS | | USART3_CK | UART5_RX | CAN2_RX | OTG_HS_ULPI_D5 | ETH_MII_TXD0/ETH_RMII_TXD0 | OTG_HS_ID | - | - | EVENTOUT |

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| | | | OUT | | | | | | | | | | | | | | |
| | PB13 | - | TIM1_CH1N | - | - | - | SPI2_SCK/I2S2_CK | | USART3_CTS | UART5_TX | CAN2_TX | OTG_HS_ULPI_D6 | ETH_MII_TXD1/ETH_RMII_TXD1 | - | - | - | EVENTOU |
| | PB14 | - | TIM1_CH2N | - | TIM8_CH2N | USART1_TX | SPI2_MISO | | USART3_RTS | UART4_RTS | TIM12_CH1 | SDMMC2_D0 | - | OTG_HS_DM | - | - | EVENTOU |
| | PB15 | RTC_REFIN | TIM1_CH3N | - | TIM8_CH3N | USART1_RX | SPI2_MOSI/I2S2_SD | | - | UART4_CTS | TIM12_CH2 | SDMMC2_D1 | - | OTG_HS_DP | - | - | EVENTOU |
| PC | PC0 | - | - | - | | - | - | | - | SAI2_FS_B | - | OTG_HS_ULPI_STP | - | FMC_SDNWE | - | - | EVENTOU |
| | PC1 | TRACED0 | - | - | | - | SPI2_MOSI/I2S2_SD | SAI1_SD_A | - | - | - | - | ETH_MDC | MDIOS_MDC | - | - | EVENTOU |

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| | PC2 | - | - | - | | - | SPI2_MISO | | - | - | - | OTG_HS_ULPI_DIR | ETH_MII_TXD2 | FMC_SDNE0 | - | - | EVENTOU |
| | PC3 | - | - | - | | - | SPI2_MOSI/I2S2_SD | - | - | - | - | OTG_HS_ULPI_NXT | ETH_MII_TX_CLK | FMC_SDCKE0 | - | - | EVENTOU |
| | PC4 | - | - | - | | - | I2S1_MCK | - | - | - | - | - | ETH_MII_RXD0/ETH_RMII_RXD0 | FMC_SDNE0 | - | - | EVENTOU |
| | PC5 | - | - | - | | - | - | - | - | - | - | - | ETH_MII_RXD1/ETH_RMII_RXD1 | FMC_SDCKE0 | COMP0_O | - | EVENTOU |
| | PC6 | - | - | TIM3_CH1 | TIM8_CH1 | - | I2S2_MCK | - | - | USART6_TX | FMC_NWAIT | SDMMC2_D6 | - | SDMMC1_D6 | - | - | EVENTOU |
| | PC7 | - | - | TIM3_CH2 | TIM8_CH2 | - | - | I2S3_MCK | - | USART6_RX | FMC_NE1 | SDMMC2_D7 | - | SDMMC1_D7 | - | - | EVENTOU |

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| | PC8 | TRACED1 | - | TIM3_CH3 | TIM8_CH3 | - | - | - | UART5_RTS | USART6_CK | FMC_NE2/FMC_NCE | - | - | SDMMC1_D0 | - | - | EVENTOU |
| | PC9 | MCO2 | - | TIM3_CH4 | TIM8_CH4 | I2C3_SDA | I2S_CKIN | - | UART5_CTS | - | QUADSPI_BK1_IO0 | - | - | SDMMC1_D1 | - | - | EVENTOU |
| | PC10 | - | - | - | - | - | - | SPI3_SCK/I2S3_CK | USART3_TX | UART4_TX | QUADSPI_BK1_IO1 | - | - | SDMMC1_D2 | - | - | EVENTOU |
| | PC11 | - | - | - | - | - | - | SPI3_MISO | USART3_RX | UART4_RX | QUADSPI_BK2_NCS | - | - | SDMMC1_D3 | - | - | EVENTOU |
| | PC12 | TRACED3 | - | - | - | - | - | SPI3_MOSI/I2S3_SD | USART3_CK | UART5_TX | - | - | - | SDMMC1_CK | - | - | EVENTOU |
| | PC13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |

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| | PC14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PC15 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| PD | PD0 | - | - | - | - | - | - | - | UART4_RX | CAN1_RX | - | - | FMC_D2 | - | - | EVENTOU |
| | PD1 | - | - | - | - | - | - | - | UART4_TX | CAN1_TX | - | - | FMC_D3 | - | - | EVENTOU |
| | PD2 | TRACED2 | - | TIM3_ETR | - | - | - | - | UART5_RX | - | - | - | SDMMC1_CMD | - | - | EVENTOU |
| | PD3 | - | - | - | - | - | SPI2_SCK/I2S2_CK | - | USART2_CTS | - | - | - | - | FMC_CLK | - | - | EVENTOU |

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| | PD4 | - | - | - | - | - | - | USART2_RTS | - | - | - | - | FMC_NOE | - | - | EVENTOU |
| | PD5 | - | - | - | - | - | - | USART2_TX | - | - | - | - | FMC_NWE | - | - | EVENTOU |
| | PD6 | - | - | - | - | SPI3_MOSI/I2S3_SD | SAI1_SD_A | USART2_RX | - | - | - | SDMMC2_CK | FMC_NWAIT | - | - | EVENTOU |
| | PD7 | - | - | - | - | SPI1_MOSI/I2S1_SD | - | USART2_CK | - | - | - | SDMMC2_CMD | FMC_NE1 | - | - | EVENTOU |
| | PD8 | - | - | - | - | - | - | USART3_TX | - | - | - | - | FMC_D13 | - | - | EVENTOU |
| | PD9 | - | - | - | - | - | - | USART3_RX | - | - | - | - | FMC_D14 | - | - | EVENTOU |

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| | PD10 | - | - | - | - | - | - | - | USART3_CK | - | - | - | - | FMC_D15 | - | - | EVENTOU |
| | PD11 | - | - | - | - | I2C4_SMBA | - | - | USART3_CTS | - | QUADSPI_BK1_IO0 | SAI2_SD_A | - | FMC_A16/FMC_CLE | - | - | EVENTOU |
| | PD12 | - | - | TIM4_CH1 | LPTIM1_IN1 | I2C4_SCL | - | - | USART3_RTS | - | QUADSPI_BK1_IO1 | SAI2_FS_A | - | FMC_A17/FMC_ALE | - | - | EVENTOU |
| | PD13 | - | - | TIM4_CH2 | LPTIM1_OUT | I2C4_SDA | - | - | - | - | QUADSPI_BK1_IO3 | SAI2_SCK_A | - | FMC_A18 | - | - | EVENTOU |
| | PD14 | - | - | TIM4_CH3 | - | - | - | - | - | UART8_CTS | - | - | - | FMC_D0 | - | - | EVENTOU |
| | PD15 | - | - | TIM4_CH4 | - | - | - | - | - | UART8_RTS | - | - | - | FMC_D1 | - | - | EVENTOU |

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| PE | PE0 | - | - | TIM4_ETR | LPTIM1_ETR | - | - | - | - | UART8_RX | - | SAI2_MCLK_A | - | FMC_NBL0 | - | - | EVENTOU |
| | PE1 | - | - | - | LPTIM1_IN2 | - | - | - | - | UART8_TX | - | - | - | FMC_NBL1 | - | - | EVENTOU |
| | PE2 | TRACECLK | - | - | - | - | SPI4_SCK | SAI1_MCLK_A | - | - | QUADSPI_BK1_IO2 | - | ETH_MII_TXD3 | FMC_A23 | - | - | EVENTOU |
| | PE3 | TRACED0 | - | - | - | - | - | SAI1_SD_B | - | - | - | - | - | FMC_A19 | - | - | EVENTOU |
| | PE4 | TRACED1 | - | - | - | - | SPI4_NSS | SAI1_FS_A | - | - | - | - | - | FMC_A20 | - | - | EVENTOU |
| | PE5 | TRACED2 | - | - | TIM9_CH1 | - | SPI4_MISO | SAI1_SCK_A | - | - | - | - | - | FMC_A21 | - | - | EVENTOU |

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| | PE6 | TRACED3 | TIM1_BKIN2_COMP1_OUT | - | TIM9_CH2 | - | SPI4_MOSI | SAI1_SD_A | - | - | - | SAI2_MCLK_B | - | FMC_A22 | - | - | EVENTOUT |
| | PE7 | - | TIM1_ETR | - | - | - | - | - | - | UART7_RX | - | QUADSPI_BK2_IO0 | - | FMC_D4 | - | - | EVENTOU |
| | PE8 | - | TIM1_CH1N | - | - | - | - | - | - | UART7_TX | - | QUADSPI_BK2_IO1 | - | FMC_D5 | COMP2_O | - | EVENTOU |
| | PE9 | - | TIM1_CH1 | - | - | - | - | - | - | UART7_RTS | - | QUADSPI_BK2_IO2 | - | FMC_D6 | - | - | EVENTOU |
| | PE10 | - | TIM1_CH2N | - | - | - | - | - | - | UART7_CTS | - | QUADSPI_BK2_IO3 | - | FMC_D7 | - | - | EVENTOU |

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| | PE11 | - | TIM1_CH2 | - | - | - | SPI4_NSS | - | - | - | - | SAI2_SD_B | - | FMC_D8 | - | EVENTOU |
| | PE12 | - | TIM1_CH3N | - | - | - | SPI4_SCK | - | - | - | - | SAI2_SCK_B | - | FMC_D9 | COMP1_O | EVENTOU |
| | PE13 | - | TIM1_CH3 | - | - | - | SPI4_MISO | - | - | - | - | SAI2_FS_B | - | FMC_D10 | COMP3_O | EVENTOU |
| | PE14 | - | TIM1_CH4 | - | - | - | SPI4_MOSI | - | - | - | - | SAI2_MCLK_B | - | FMC_D11 | - | EVENTOU |
| | PE15 | - | TIM1_BKIN_COMP0_OUT | - | - | - | - | - | - | - | - | - | - | FMC_D12 | - | EVENTOUT |

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| PF | PF0 | - | - | - | - | I2C2_SDA | - | - | - | - | - | - | - | FMC_A0 | - | - | EVENTOU |
| | PF1 | - | - | - | - | I2C2_SCL | - | - | - | - | - | - | - | FMC_A1 | - | - | EVENTOU |
| | PF2 | - | - | - | - | I2C2_SMBA | - | - | - | - | - | - | - | FMC_A2 | - | - | EVENTOU |
| | PF3 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A3 | - | - | EVENTOU |
| | PF4 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A4 | - | - | EVENTOU |
| | PF5 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A5 | - | - | EVENTOU |

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| | PF6 | - | - | - | TIM10_CH1 | - | SPI5_NSS | SAI1_SD_B | - | UART7_RX | QUADSPI_BK1_IO3 | - | - | - | - | - | EVENTOU |
| | PF7 | - | - | - | TIM11_CH1 | - | SPI5_SCK | SAI1_MCLK_B | - | UART7_TX | QUADSPI_BK1_IO2 | - | - | - | - | - | EVENTOU |
| | PF8 | - | - | - | - | - | SPI5_MISO | SAI1_SCK_B | - | UART7_RTS | TIM13_CH1 | QUADSPI_BK1_IO0 | - | - | - | - | EVENTOU |
| | PF9 | - | - | - | - | - | SPI5_MOSI | SAI1_FS_B | - | UART7_CTS | TIM14_CH1 | QUADSPI_BK1_IO1 | - | - | - | - | EVENTOU |
| | PF10 | - | - | - | - | - | - | - | - | - | QUADSPI_CLK | - | - | - | - | - | EVENTOU |
| | PF11 | - | - | - | - | - | SPI5_MOSI | - | - | - | - | SAI2_SD_B | - | FMC_SDNRAS | - | - | EVENTOU |

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| | PF12 | - | - | - | - | - | - | - | - | - | - | - | FMC_A6 | - | - | EVENTOU |
| | PF13 | - | - | - | - | I2C4_SMBA | - | - | - | - | - | - | FMC_A7 | - | - | EVENTOU |
| | PF14 | - | - | - | - | I2C4_SCL | - | - | - | - | - | - | FMC_A8 | - | - | EVENTOU |
| | PF15 | - | - | - | - | I2C4_SDA | - | - | - | - | - | - | FMC_A9 | - | - | EVENTOU |
| PG | PG0 | - | - | - | - | - | - | - | - | - | - | - | FMC_A10 | - | - | EVENTOU |
| | PG1 | - | - | - | - | - | - | - | - | - | - | - | FMC_A11 | - | - | EVENTOU |

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| | PG2 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A12 | - | - | EVENTOU |
| | PG3 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A13 | - | - | EVENTOU |
| | PG4 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A14/ FMC_BA0 | - | - | EVENTOU |
| | PG5 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A15/ FMC_BA1 | - | - | EVENTOU |
| | PG6 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_NE3 | - | - | EVENTOU |
| | PG7 | - | - | - | - | - | SAI1_MC LK_A | - | USART6_ CK | - | - | - | - | FMC_INT | - | - | EVENTOU |

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| | PG8 | - | - | - | - | - | SPI6_NSS | - | - | USART6_RTS | - | - | ETH_PPS_OUT | FMC_SDCLK | - | - | EVENTOU |
| | PG9 | - | - | - | - | - | SPI1_MISO | - | - | USART6_RX | QUADSPI_BK2_IO2 | SAI2_FS_B | SDMMC2_D0 | FMC_NE2/FMC_NCE | - | - | EVENTOU |
| | PG10 | - | - | - | - | - | SPI1_NSS/I2S1_WS | - | - | - | - | SAI2_SD_B | SDMMC2_D1 | FMC_NE3 | - | - | EVENTOU |
| | PG11 | - | - | - | - | - | SPI1_SCK/I2S1_CK | - | - | - | - | SDMMC2_D2 | ETH_MII_TX_EN/ETH_RMII_TX_EN | - | - | - | EVENTOU |
| | PG12 | - | - | - | LPTIM1_IN1 | - | SPI6_MISO | - | | USART6_RTS | - | - | SDMMC2_D3 | FMC_NE4 | - | - | EVENTOU |
| | PG13 | TRACED0 | - | - | LPTIM1_OUT | - | SPI6_SCK | - | - | USART6_CTS | - | - | ETH_MII_TXD0/ETH_RMII_TXD0 | FMC_A24 | - | - | EVENTOU |

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| | PG14 | TRACED1 | - | - | LPTIM1_ETR | - | SPI6_MOSI | - | - | USART6_TX | QUADSPI_BK2_IO3 | - | ETH_MII_TXD1/ETH_RMII_TXD1 | FMC_A25 | - | - | EVENTOU |
| | PG15 | - | - | - | - | - | - | - | - | USART6_CTS | - | - | - | FMC_SDNCAS | - | - | EVENTOU |
| PH | PH0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PH1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PH2 | - | - | - | LPTIM1_IN2 | - | - | - | - | - | QUADSPI_BK2_IO0 | SAI2_SCK_B | ETH_MII_CRS | FMC_SDCKE0 | - | - | EVENTOU |
| | PH3 | - | - | - | - | - | - | - | - | - | QUADSPI_BK2_IO1 | SAI2_MCLK_B | ETH_MII_COL | FMC_SDNE0 | - | - | EVENTOU |

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| | PH4 | - | - | - | - | I2C2_SCL | - | - | - | - | - | OTG_HS_ULPI_NXT | - | - | - | EVENTOU |
| | PH5 | - | - | - | - | I2C2_SDA | SPI5_NSS | - | - | - | - | - | - | FMC_SDNWE | - | EVENTOU |
| | PH6 | - | - | - | - | I2C2_SMBA | SPI5_SCK | - | - | - | TIM12_CH1 | - | ETH_MII_RXD2 | FMC_SDNE1 | - | EVENTOU |
| | PH7 | - | - | - | - | I2C3_SCL | SPI5_MISO | - | - | - | - | - | ETH_MII_RXD3 | FMC_SDCKE1 | - | EVENTOU |
| | PH8 | - | - | - | - | I2C3_SDA | - | - | - | - | - | - | - | FMC_D16 | - | EVENTOU |
| | PH9 | - | - | - | - | I2C3_SMBA | - | - | - | - | TIM12_CH2 | - | - | FMC_D17 | - | EVENTOU |

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| | PH10 | - | - | TIM5_CH1 | - | I2C4_SMBA | - | - | - | - | - | - | - | FMC_D18 | - | - | EVENTOU |
| | PH11 | - | - | TIM5_CH2 | - | I2C4_SCL | - | - | - | - | - | - | - | FMC_D19 | - | - | EVENTOU |
| | PH12 | - | - | TIM5_CH3 | - | I2C4_SDA | - | - | - | - | - | - | - | FMC_D20 | - | - | EVENTOU |
| | PH13 | - | - | - | TIM8_CH1N | - | - | - | - | UART4_TX | CAN1_TX | - | - | FMC_D21 | - | - | EVENTOU |
| | PH14 | - | - | - | TIM8_CH2N | - | - | - | - | UART4_RX | CAN1_RX | - | - | FMC_D22 | - | - | EVENTOU |
| | PH15 | - | - | - | TIM8_CH3N | - | - | - | - | - | - | - | - | FMC_D23 | - | - | EVENTOU |

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| PI | PI0 | - | - | TIM5_CH4 | - | - | SPI2_NSS/I2S2_WS | - | - | - | CAN4_TX | - | - | FMC_D24 | - | - | EVENTOU |
| | PI1 | - | - | - | TIM8_BKIN2_COMP | - | SPI2_SCK/I2S2_CK | - | - | - | CAN4_RX | - | - | FMC_D25 | - | - | EVENTOU |
| | PI2 | - | - | - | TIM8_CH4 | - | SPI2_MISO | - | - | - | - | - | - | FMC_D26 | - | - | EVENTOU |
| | PI3 | - | - | - | TIM8_ETR | - | SPI2_MOSI/I2S2_SD | - | - | - | - | - | - | FMC_D27 | - | - | EVENTOU |
| | PI4 | - | - | - | TIM8_BKIN_COMP2 | - | - | - | - | - | CAN5_TX | SAI2_MCLK_A | - | FMC_NBL2 | - | - | EVENTOU |
| | PI5 | - | - | - | TIM8_CH1 | - | - | - | - | - | CAN5_RX | SAI2_SCK_A | - | FMC_NBL3 | - | - | EVENTOU |

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PI6 | - | - | - | TIM8_CH2 | - | - | - | - | - | - | SAI2_SD_A | - | FMC_D28 | - | - | EVENTOU |
| | PI7 | - | - | - | TIM8_CH3 | - | - | - | - | - | - | SAI2_FS_A | - | FMC_D29 | - | - | EVENTOU |
| | PI8 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PI9 | - | - | - | - | - | - | - | - | UART4_RX | CAN1_RX | - | - | FMC_D30 | - | - | EVENTOU |
| | PI10 | - | - | - | - | - | - | - | - | - | - | - | ETH_MII_RX_ER | FMC_D31 | - | - | EVENTOU |
| | PI11 | - | - | - | - | - | - | - | - | - | - | OTG_HS_ULPI_DIR | - | - | - | - | EVENTOU |

| | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PI12 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PI13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PI14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PI15 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| PJ | PJ0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PJ1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |

| | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PJ2 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PJ3 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PJ4 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PJ5 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PJ6 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PJ7 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |

| | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PJ8 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PJ9 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PJ10 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PJ11 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PJ12 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PJ13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |

| | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PJ14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PJ15 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| PK | PK0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PK1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PK2 | | | | | | | | | | | | | | | - | EVENTOU |
| | PK3 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PK4 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PK5 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PK6 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |
| | PK7 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOU |

# VIII. Functional Description

## 8.1. CPU

BST32F 4xx integrates a 32-bit RISC processor with an operating frequency of 180MHz, supports single and double precision floating point operations, and has excellent computing performance and low interrupt latency.

- Built-in 16KB instruction cache and 16KB data cache
- 64-bit ITCM interface
- Two 32-bit DTCM interfaces
- Dedicated low-latency peripheral interface

## 8.2. Memory Map

BST32F 4xx Technical Reference Manual for detailed information on the memory map and address boundaries of all peripherals.

## 8.3. Memory Protection Unit

The memory protection unit (MPU) is used to manage the CPU's access to the entire 4G address space, improving system security by preventing unauthorized access.

The MPU is usually managed by an RTOS (Real-Time Operating System), which can detect when a program accesses a memory location that is prohibited by the MPU. In an RTOS environment, the kernel can dynamically update the settings of the MPU area based on the executed process.

## 8.4. Embedded FLASH

BST32F 4xx products have built-in Flash memory up to 2MB for storing programs and data, with the following features:

- Single/dual bank operation mode, support read and write synchronization;

- Level 3 Read Protection (RDP):
  - level 0: no read protection;
  - level 1: no access to the flash memory (read, erase, write), backup SRAM is executed during debug functions, when booting from RAM or system memory bootloader;
  - level 2: Debug or chip read operations are prohibited.
- Write Protect (WRP): The protected area can be prevented from being erased and written.
- Dedicated code read protection.

### 8.5. CRC (Cyclic Redundancy Check) calculation unit

The CRC (Cyclic Redundancy Check) calculation unit generates a CRC code from a 32-bit data word using a polynomial generator of configurable value and size.

In many applications, CRC is often used to verify the integrity of data transmission or storage.

### 8.6. On-chip SRAM

All products have built-in:

- 512KB System SRAM:
  - SRAMH bus includes SRAM1: 368KB, SRAM2: 16KB
  - DTCM-RAM: 128KB
- ITCM-RAM 16KB:
  - ITCM-RAM is located in the TCM interface and is only retained when the CPU is executing/instructions are useful for critical real-time programs

DTCM-RAM can be accessed by DMA, and ITCM-RAM only supports CPU access and 0 wait CPU clock.

- 4KB backup SRAM

Supports CPU access only, supports write protection, and can maintain data in Standby or VBAT mode.

### 8.7. Direct Memory Access Controller (DMA)

The product has 2 general DMA controllers, each controller supports 8 data streams, each data stream can have up to 8 channels. Each data stream can manage the transfer from memory to memory, peripheral to memory, memory to peripheral, built-in dedicated FIFO for connecting peripherals, support burst transfer, support circular buffer, double buffer, no program code control is required when using it.

Each data stream can be configured by software hardware DMA request or software trigger, and the amount of data transferred between the data source and the data destination is unlimited.

DMA-capable peripherals include: SPI, I2C, USART, general-purpose, basic and advanced control timers TIMx, DAC, SDIO, ADC

### 8.8. Flexible Memory Controller ( FMC)

The Flexible Memory Controller (FMC) includes three memory controllers:

- NOR/PSRAM Memory Controller
- NAND memory controller
- Synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) Controller

The FMC controller mainly supports the following functions:

- Static memory mapped device interface:

- Static Random Access Memory (SRAM)
- NOR Flash memory /OneNAND flash memory
- NOR Flash memory can support 2 56M bytes, that is, 2 Gb storage particle size
- PSRAM (4 memory sticks)
- NAND Flash, up to 8KB data can be checked with ECC hardware
- Synchronous DRAM memory interface (SRAM/Mobile LPSDR SDRAM)
- 8, 16, 32-bit data bus width
- Each memory has independent chip select control
- Each memory can be configured independently
- Write FIFO
- Read FIFO for SDRAM controller
- The maximum synchronous access frequency of FMC_CLK/FMC_SDCLK is HCLK/2

### 8.9. Nested Vectored Interrupt Controller (NVIC)

The product has a built-in nested vectored interrupt controller that can manage 16 priority levels and handles maskable interrupt channels and 16 interrupt lines supported by the core.

This hardware block provides flexible interrupt management capabilities with minimal interrupt latency.

### 8.10. External Interrupt/Event Controller (EXTI)

The external interrupt (EXTI) is directly connected to the NVIC . EXTI contains 2 5 edge detectors for generating interrupt requests. Each interrupt line can be independently

configured with its trigger event (rising edge, falling edge, or both edges) and can be individually masked. Up to 16 of the external interrupt lines can be selected from GPIO .

### 8.11. Clock

At power-on reset, the core first uses the 16MHz internal HSI RC oscillator as the default clock, which is calibrated according to industrial standards to provide **2%** accuracy. Then, the user can select the RC oscillator or external 4-26 MHz clock source as the system clock through register configuration, and can monitor the clock status. When a clock failure is detected, it automatically switches to the internal RC oscillator and generates a software interrupt (if enabled).

The clock source can be multiplied to 180MHz by PLL inside the chip, and the PLL clock can also be monitored and interrupted.

### 8.12. Startup Mode

The boot mode can be selected through the BOOT pin and BOOT_ADDx, supporting a programming range of 0x0000 0000 to 0x3FFF FFFF, and can be selected from the following three modes:

- Boot from the chip's internal FLASH
- Boot from internal SRAM
- Booting from the boot code area

### 8.13. Power Solution

#### 8.13.1 Power supply solution

- VDD = 2.1～ 3.6V : The VDD pin is used to power the GPIO pins and internal modules such as the voltage regulator ( LDO) .
- V DDA = 2.1 to 3.6 V : Power the ADC and DAC through the V DDA pin . V DDA and VSSA must be at the same potential as V DD and V SS .

- V BAT = 2.0 ~ 3.6 V : The VBAT pin allows the VBAT domain of the device to be powered from an external battery, an external supercapacitor , or from VDD when no external battery or external supercapacitor is present. When no VDD is present, the VBAT pin (through an internal power switch) powers the RTC , external 32 kHz crystal ( LEXT), and the battery-backed register ( BPR)

### 8.13.2 Reset

This product integrates a power-on reset (POR) and a low voltage reset ( LVR) circuit, which is always in operation, allowing the device to operate when the power supply exceeds 2.1 V ; when V DD is lower than the set threshold, the device can be placed in a reset state without the need for an external reset circuit.

### 8.13.3 Power supply monitoring

Products that include the PDR_ON PIN enable the internal power monitor by keeping PDR_ON high, while products that do not include the PDR_ON PIN keep the power monitor enabled after power-on.

All products integrate a power-on reset (POR)/power-down reset (PDR) circuit and are coupled with a brown-out reset (BOR) circuit. At power-on, the POR/PDR is activated to ensure that the MCU's operating voltage is above 2.1v. When the 2.1v POR threshold level is reached, the register configuration is loaded, and the default BOR threshold is confirmed or modified according to the user's settings, or the BOR is turned off. Three BOR thresholds can be set through the corresponding registers. When V DD is lower than the specified threshold V POR/PDR or V BOR , the product will remain in reset mode without an external reset circuit.

The product also has an embedded programmable voltage detector (PVD), which can be turned off or enabled by the application program, which can be used to monitor the V DD

/V DDA supply. When V DD /V DDA is lower than the V PVD threshold and/or V DD /V DDA is higher than the V PVD threshold, an interrupt will be generated. Subsequently, the interrupt service routine will generate a warning message and/or put the MCU into a safe state.

**Products packaged with PDR_ON PIN support the following functions:**

- Internal Power-On Reset (POR)/Power-Down Reset (PDR) circuit can be disabled via PDR_ON PIN
- When PDR_ON is connected to $V_{SS}$, an external reset circuit must be used to hold the device in reset when $V_{DD} < 2.1v$, see Figure 3 -1. When $V_{DD}$ is below the threshold voltage ( see Figure 3 -1 Use PDR_ON to turn off the internal reset circuit (use external reset ) must be kept in reset state.

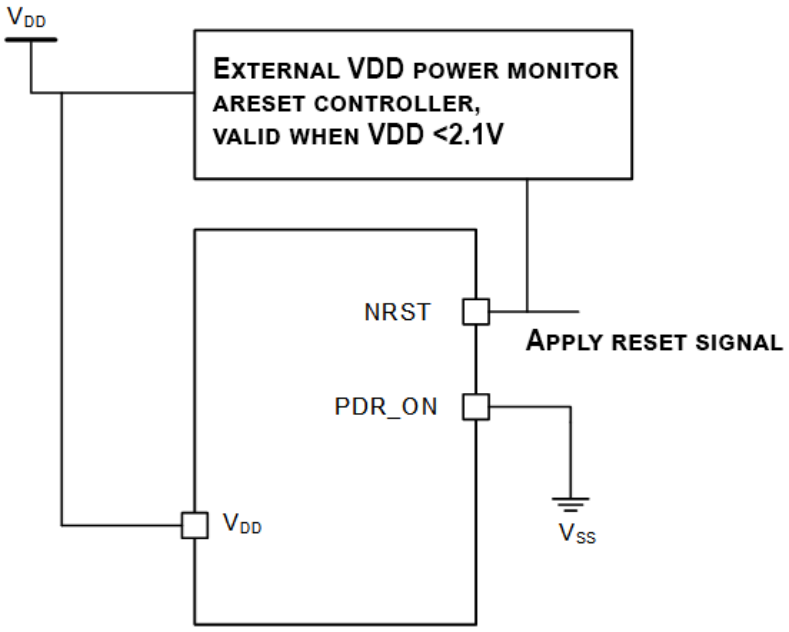


Figure 3 -1. Use PDR_ON to turn off the internal reset circuit and use external reset

### 8.13.4 Internal voltage regulator (LDO)

The internal LDO has three operating modes:

### 8.13.5. MR Mode

MR mode is used in normal mode (default mode), overdrive mode (enabled by software), or stop mode. Different voltage levels are provided to achieve the best balance between maximum frequency and dynamic power consumption. For a given voltage level, overdrive mode can operate at a higher frequency than normal mode.

During stop mode, MR has two configurations:

- MR works in normal mode (MR's default mode in stop mode)
- MR works in low load mode (reduced leakage current mode)

## 8.13.6. LPR mode

When entering stop mode, the LP regulator mode is configured by software. Similar to MR mode, there are two configurations of LPR during stop mode:

- LPR works in normal mode (default mode when LPR is ON)
- LPR works in low load mode (reduced leakage current mode)

### 8.13.7. Power-down

The power-down function can be activated only when entering the standby mode. At this time, the voltage regulator outputs high impedance, the core circuit is powered off, and zero power consumption is achieved. The register and SRAM contents are lost.

Table 3.1 -shows the operating modes that the voltage regulator can support in different operating modes of the chip.

Note:

- Two 2.2μF capacitors with an equivalent series resistance (ESR) < 2Ω should be connected to the VCAP_1 and VCAP_2 pins (or a 4.7μF capacitor with an equivalent series resistance (ESR) between 0.1-0.2Ω when only the VCAP_1 pin is provided (LQFP64 package)).

Table 3-1Regulator configuration mode and device operating mode

| VOLTAGE REGULATOR CONFIGURATION | OPERATION MODE | SLEEP MODE | STOP MODE | STANDBY MODE |
|---|---|---|---|---|
| Normal mode | MR | MR | MR or LPR | - |
| Overload Mode | MR | MR | - | - |
| Underdrive mode | - | - | MR or LPR | - |
| Power-down mode | - | - | - | Yes |

- "-" means the corresponding configuration is not available

### 8.13.7 Low Power Mode

The product supports three low-power modes to achieve the best balance between low power consumption, short startup time and available wake-up sources:

- Sleep Mode

  In sleep mode, only the CPU stops working, all peripherals continue to operate and can be interrupted/event;

  Wake up the CPU.

- Stop Mode

- The shutdown mode can achieve the lowest power consumption while maintaining the contents of SRAM and registers;
- All clocks will stop, including PLL, HSI RC and HSE;
- In stop mode, the regulator can operate in MR or LPR mode and be configured as shown in Table 3:
  - Normal mode (default mode when MR or LPR is enabled);
  - Under-drive mode.

In Stop mode, the chip can be woken up by EXTI, which can be any of 16 external interrupt sources, PVD output, RTC alarm/wakeup/timestamp event, USB OTG FS/HS wakeup.

Table 3. 2

| VOLTAGE REGULATOR CONFIGURATION | MAIN REGULATOR (MR) | LOW POWER REGULATOR (LPR) |
|---|---|---|
| Normal mode | MR ON | LPR ON |
| Low load mode | MR in low load mode | LPR in low load mode |

- Standby mode

  The standby mode is designed to provide the user with the lowest power consumption, therefore, the internal voltage regulator is turned off and the 1.2V voltage domain

  The power supply will be stopped. The PLL, HSI RC and HSE crystal oscillators will also be turned off. After entering standby mode, the contents of the SRAM and registers will be lost except for the registers in the selected backup domain and backup SRAM.

The chip can exit standby mode by an external reset (NRST pin), an IWDG reset, a rising or falling edge on the WKUP pin (PA0, PA2, PC1, PC13, PI8, PI11), or an RTC alarm/wake-up/timestamp event.

### 8.13.8 $V_{BAT}$ Operation

When $V_{DD}$ is not powered, the chip can power the VBAT domain from an external battery or supercapacitor through the VBAT pin, including: RTC, backup registers, and backup SRAM can all be powered by VBAT .

Note:

- When the chip is powered from VBAT , external interrupts and RTC alarms/events do not exit it from VBAT operating mode.
- When the PDR_ON pin is connected to VSS (internal reset OFF), the VBAT function is no longer available and the VBAT pin should be connected to VDD.

## IX. Real-time clock (RTC), backup SRAM, backup register BKR

The real-time clock (RTC) is a counter that stores time information in BCD format. It records specific calendar times from 00 to 99. It supports both 12/24 hour time systems and automatically calculates the days 28, 29 (leap year), 30 and 31 according to the month and year.

The RTC and backup SRAM, backup registers (BPR) are powered by a switch that selects VDD power when VDD is valid, otherwise they are powered by the VBAT pin. The RTC and backup SRAM, registers will not be reset by system or power reset sources; they will not be reset when waking up from standby mode.

## X. Timer and Watchdog

The chip includes 2 advanced control timers, 10 general-purpose timers, 2 basic timers, and 2 watchdog timers. Table 3 compares the -features of the advanced control timers, general-purpose timers, and basic timers.

Table 3. Comparison of characteristics of -1timers

| TIMER TYPE | TIMER | COUNTER RESOLUTION | COUNTER TYPE | PRESCALER FACTOR | DMA REQUEST GENERATION | CAPTURE/COMPARE CHANNEL | COMPLEMENTARY OUTPUT | MAXIMUM INTERFACE CLOCK (MHZ) | MAXIMUM TIMER CLOCK (MHZ) |
|---|---|---|---|---|---|---|---|---|---|
| Advanced Control | TIM1 TIM8 | 16-bit | Increment, decrement, increment/decrement | Any integer between 1 and 65536 | have | 4 | have | 108 | 180 |
| General | TIM2 TIM5 | 32-bit | Increment, decrement, increment/decrement | Any integer between 1 and 65536 | have | 4 | none | 54 | 1 08 |
| | TIM3 TIM4 | 16-bit | Increment, decrement, increment/decrement | Any integer between 1 and 65536 | have | 4 | none | 54 | 108 |
| | TIM9 | 16-bit | Increment | Any integer between 1 and 65536 | none | 2 | none | 108 | 180 |
| | TIM10 TIM11 | 16-bit | Increment | Any integer between 1 and 65536 | none | 1 | none | 108 | 180 |

| TIMER TYPE | TIMER | COUNTER RESOLUTION | COUNTER TYPE | PRESCALER FACTOR | DMA REQUEST GENERATION | CAPTURE/COMPARE CHANNEL | COMPLEMENTARY OUTPUT | MAXIMUM INTERFACE CLOCK (MHZ) | MAXIMUM TIMER CLOCK (MHZ) |
|---|---|---|---|---|---|---|---|---|---|
| | TIM 12 | 16-bit | Increment | Any integer between 1 and 65536 | none | 2 | none | 54 | 108 |
| | TIM 13 TIM 14 | 16-bit | Increment | Any integer between 1 and 65536 | none | 1 | none | 54 | 108 |
| Basics | TIM 6 TIM 7 | 16-bit | Increment | Any integer between 1 and 65536 | have | 0 | none | 54 | 108 |

- Depending on the configuration of the TIMPRE bits in the RCC_DCKCFGR register, the maximum timer clock can be 108 MHz or 180 MHz.

### 10.1. Advanced control timer (TIM1, TIM8)

The advanced control timers (TIM1, TIM8) can be viewed as three-phase PWM generators multiplexed on six channels. They have complementary PWM outputs with programmable dead-time insertion and can also be used as complete general-purpose timers.

4 independent channels can be used for:

- Input Capture
- Output Compare
- PWM generation (edge or center-aligned mode)
- Single pulse mode output

If configured as a standard 16-bit timer, the functionality is the same as the generic TIMx timers. If configured as a 16-bit PWM generator, it has full modulation capability (0-100%).

Advanced control timers can work with TIMx timers through the timer link function to provide synchronization or event linking capabilities.

TIM1 and TIM8 support the generation of independent DMA requests.

### 10.2. General purpose timer (TIMx)

The chip has 10 built-in synchronous general-purpose timers ( see Table 3 -3 for the differences).

- TIM2, TIM3, TIM4, and TIM5

BST32F 4xx includes 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, TIM4. TIM2 and TIM5 timers are based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. TIM3 and TIM4 timers are based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. They all have 4 independent channels for input capture/output comparison, PWM, and single pulse mode output. In the largest package, up to 16 input capture/output comparison/PWM are available.

The TIM2, TIM3, TIM4, and TIM5 general-purpose timers can work together or with other general-purpose timers and the advanced control timers TIM1 and TIM8 through the timer chaining feature to achieve synchronization or event chaining.

Any general purpose timer can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 can generate independent DMA requests. They can process quadrature (incremental) encoder signals and can also process the digital outputs of 1 to 4 Hall effect sensors.

- TIM9, TIM10, TIM11, TIM12, TIM13, TIM14

These timers are based on a 16-bit auto-reload up-counter and a 16-bit prescaler. TIM10, TIM11, TIM13, TIM14 have one independent channel, while TIM9 and TIM12 have two independent channels for input capture/output compare, PWM, single pulse mode output. They can be synchronized with TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as a simple time base.

### 10.3. Basic timers TIM6 and TIM7

These timers are primarily used to generate DAC trigger signals and waveforms, but can also be used as a general-purpose 16-bit time base.

TIM6 and TIM7 support the generation of independent DMA requests.

### 10.4. Independent watchdog

The independent watchdog is based on a 12-bit down counter and an 8-bit prescaler. It is clocked by an independent 32 kHz internal RC, and since the internal RC is independent of the main clock, it can work in stop and standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free-running timer to provide timeout management for the application. It can be configured by hardware or software through the option byte.

### 10.5. Window Watchdog

The window watchdog is based on a 7-bit down counter that can be set to free-run. It can be used as a watchdog to reset the device if a problem occurs. It is driven by the main clock. There is an early warning interrupt function and the counter can be frozen in debug mode.

### 10.6. SysTick Timer

This timer is designed for use in real-time operating systems, but can also be used as a standard down counter. It has the following features:

- 24-bit down counter
- Automatic reload function
- When the counter reaches 0, a maskable system interrupt is generated
- Programmable clock source

## XI. Inter-Integrated Circuit Interface (I 2 C)

There are 4 I2Cs embedded in the device. Please refer to Table 3 -4 to understand their functional implementation.

The I2C bus interface handles the communication between the chip and the I2C bus, controlling the timing, protocol, and arbitration of the I2C bus.

The chip's I2C peripherals meet the following characteristics:

- Compatible with I2C bus specifications:

  Master-slave mode, allowing multiple hosts.

  - Standard mode (Sm) with a bit rate of up to 100 kb/s
  - Fast mode (Fm) with a maximum bit rate of 400 kb/s
  - Fast-mode+ (Fm+) with up to 1Mb/s bit rate and 20mA output drive IO
  - 7-bit and 10-bit addressing modes, allowing multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- Compatible with SMBUS 2.0 specification
- Hardware PEC (Packet Error Check) generation and acknowledgement with ACK control

  - Support Address Resolution Protocol (ARP)

- SMBus Alerts

- Compatible with Power System Management Bus Protocol Rev1.1
- Independent clock: You can select an independent clock source, which is the I2C communication speed and PCLK reprogrammable
- Programmable analog and digital noise filters
- 1-byte buffer with DMA support

Table 3 -1. I2C Implementation

| I ² C FEATURES (1) | I2C1 ~ I2C4 |
|---|---|
| Standard mode (up to 100 kbit/s) | X |
| Fast mode (up to 100 kbit/s) | X |
| Fast-mode+ with 20mA output drive I/O (up to 1Mbit/s) | X |
| Programmable analog and digital noise filters | X |
| SMBus/PMBus Hardware Support | X |
| Independent clock | X |

- X：Supported.

## XII. Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The device has a built-in USART, and its performance implementation can be found in Table 3 -5 .

The universal synchronous/asynchronous receiver/transmitter provides a flexible full-duplex data exchange mode and can exchange data with external devices that comply with the NRZ standard.

USART peripheral support:

- Full-duplex asynchronous communication
- Configurable 16- or 8-times oversampling provides flexibility in data and clock tolerances.
- Dual clock domains, convenient baud rate programming, independent of PCLK reprogramming.
- Automatic baud rate detection
- Programmable data word length (7/8/9 bits)
- Programmable MSB-first or LSB-first shift data order
- Programmable parity (odd, even or no parity)
- Configurable stop bits (1, 1.5 or 2 stop bits)
- Output clock in synchronous mode for synchronous communication
- Single-line half-duplex communication
- Individual signal polarity controls for transmit and receive
- Tx/Rx pin configurations are swappable
- Hardware flow control for modems and RS-485 transceivers
- Multiprocessor Communication
- LIN master mode synchronous break transmission function and LIN slave mode break detection function
- Support ModBus communication

Table 3 -1. USART Implementation

| Features (1) | USART1/2/ 3/6 | UART4 /5/7/8 |
|---|---|---|
| Single-line half-duplex communication | X | X |
| LIN Mode | X | X |

| Features (1) | USART1/2/ 3/6 | UART4 /5/7/8 |
|---|---|---|
| Dual clock domains | X | X |
| Receiver timeout interrupt | X | X |
| Modbus Communication | X | X |
| Automatic baud rate detection | X | X |
| Drive Enable | X | X |
| Synchronous Mode | X | - |

X = Support.

## XIII. Serial Peripheral Interface (SPI)

The chip has 6 SPIs, supporting master-slave mode, full-duplex and simplex communication modes with a communication rate of up to 25Mbit/s. The 3-bit prescaler can generate 8 master mode frequencies, the frame can be configured to 4-16 bits, and all SPIs can use the DMA controller

- When SPI acts as a slave and only receives, it can operate at a frequency of 54M.
- When SPI is a slave receiving and transmitting, it can work at 37M
- When SPI is a slave device that only transmits, it can operate at a frequency of 37M.
- SPI is used as the host. If it only transmits and does not care whether the received data is correct, it can work at 40M.
- SPI is used as the host. If it needs to receive while transmitting, and ensure that the received and transmitted data are correct, the maximum operating frequency is 30M.

### 13.1. Secure Digital Input/Output Interface (SDIO)

The product provides an SD/SDIO/MMC host interface with a data transfer rate of up to 24MHz, compliant with SD Memory Card Specification Version 2.0.

Supports SDMMC cards, but only supports one SD/SDMMC/MMC4.2 card at a time, but supports multiple MMC4.1 or earlier version cards.

### 13.2. Controller Area Network (CAN)

Supports up to 3 CANs compatible with 2.0A and B (active) specifications, with a bit rate of up to 1 Mbit/s. They can receive and send standard frames with 11-bit identifiers and extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOs, with 3 levels and 28 shared adjustable filter groups (even if only one CAN is used, all resources can be used), CAN1, CAN2 are equipped with 256 bytes of SRAM, and CAN3 is equipped with 512 bytes of SRAM.

### 13.3. Management Data Input Output Interface (MDIO) Slave Mode

The MDIO bus is useful if the master chip in the system needs to manage (configure and obtain status data) one or more slave chips. The bus protocol uses only two signals:

- MDC: Management Data Clock
- MDIO: Data line that carries the opcode (write or read), slave (port) address, MDIOS register address, and data

In each transaction, the master reads the contents of the MDIOS register of one of the slaves or writes data to the MDIOS register of one of the slaves.

The MDIOS peripheral acts as a slave interface to the MDIO bus, and the MDIO master can use the MDC/MDIO line to write and read 16-bit MDIOS registers stored in the 32 MDIOS. These MDIOS registers are managed by firmware, allowing the MDIO master to configure the application running on the HWD32 and obtain status information from it.

MDIOS can operate in Stop mode and can optionally wake up the HWD32 if the MDIO master reads or writes to one of the MDIOS registers.

### 13.4. Ethernet MAC interface compatible with IEEE 1588 standard (Ethernet)

The chip integrates a media access controller (MAC) that complies with the IEEE - 802.3-2002 standard for Ethernet LAN communication through a standard media independent interface (MII) or a simplified media independent interface (RMII) . The microcontroller requires an external device interface device (PHY) to connect to the physical LAN bus (twisted pair, optical fiber, etc). The PHY uses a 17-wire MII interface or a 9-wire RMII interface to connect this device, and can use the 25 MHz from the microcontroller to provide a clock.

The main features are as follows:

- Support 10M bit/ s and 100Mbit /s rates
- Dedicated DMA controller for high-speed transfer between SRAM and descriptors
- Support tagged MAC frames (support V LAN)
- Supports close duplex (CSMA /CD) and full duplex mode
- Support MAC control sublayer
- Support 32 CRC generation and deletion
- Supports address filtering modes under physical and multicast addresses (multicast and group addresses)
- Each sent and received frame supports 32-bit status code
- Internal FIFO for buffering transmission and reception. The capacity of transmission FIFO and reception FIFO is 2 KB
- When the system time is greater than the target time, an interrupt can be triggered

### 13.5. Universal Serial Bus on-the-go full speed (OTG_FS)

The chip has a built-in USB OTG full-speed device/host/OTG peripheral with an integrated transceiver. The USB OTG FS peripheral is compatible with the USB 2.0 specification and the OTG 2.0 specification, has software-configurable endpoint settings, and supports suspend/resume functions. The USB OTG controller requires a dedicated 48MHz clock generated by a PLL connected to the HSE oscillator. When operating in OTG/host mode, a power switch is required when the bus is connected to a device.

The main features are:

- Combined Rx and Tx FIFO size of 4KB with dynamic FIFO size
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
- 1 bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- 12 host channels, support periodic OUT
- Software configurable operation mode: OTG1.3 and OTG2.0
- Supports USB 2.0 LPM (Link Power Management)
- Support built-in FS OTG PHY
- Built-in HNP/SNP/IP (does not require any external resistors)
- Supports charging port detection as described in Battery Charging Specification Version 1.2

### 13.6. Universal Serial Bus on-the-go High Speed (OTG_HS)

The chip has a built-in peripheral that supports USB OTG high-speed device (up to 480 Mb/s)/host/OTG, supporting full-speed and high-speed operation. The integrated transceiver is used for full-speed operation (12 MB/s), and the UTMI pin-less interface (ULPI) is used for high-speed operation (480 MB/s). When using USB OTG HS in HS mode, an external PHY device is required to connect to ULPI.

The USB OTG HS peripheral is compatible with the USB 2.0 specification and the OTG 2.0 specification. It has software configurable endpoint settings and supports suspend/resume functionality. The USB OTG controller requires a dedicated 48 MHz clock generated by a PLL connected to the HSE oscillator.

When working in OTG/host mode, the bus needs a power switch when connecting to the device

The main features are:

- Combined Rx and Tx FIFO size of 4KB with dynamic FIFO size.
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
- 8 bidirectional endpoints
- 16 host channels, support periodic OUT
- Software configurable operation mode: OTG1.3 and OTG2.0
- Supports USB 2.0 LPM (Link Power Management)
- In SDR mode, external HS or HS OTG supports ULPI, and OTG PHY is connected to the ULPI port of the chip through 12 signal lines, and a 60 MHz output clock can be used.
- Built-in USB DMA
- Built-in HNP/SNP/IP (does not require any external resistors)

### 13.7. Cryptographic Processor (CRYP)

With the help of encryption processor (CRYP), can be used DES, Triple-DES (3DES) , or AES algorithms are used to encrypt data and Decryption. The cryptographic processor is fully compliant with the following standards:

- Encryption Standard (DES) and Triple DES (TDES) as defined by the Federal Information Processing Standards Publication ( FIPS PUB 46-3 , October 1999) and the American National Standards Institute (ANSI X9.52)
- Encryption Standard (AES) as specified in the Federal Information Processing Standards Publication ( FIPS PUB 197 , November 2001)

Supports multiple key sizes and chaining modes:

- AES link mode ECB/CBC/OFB/CTR , support 128 , 192 or 256 bits Key size
- DES/TDES link modes ECB and CBC , support for standard 56 -bit keys (each with 8 -bit parity)

### 13.8. Hash Processor (HASH)

The hash processor is fully compatible with the secure hash algorithm (SHA-1, SHA-224 and SHA-256), MD5 (Message Digest Algorithm 5) hash algorithms and suitable for a variety of applications HMAC (Keyed-Hash Message Authentication Code) hashing algorithm. HMAC The algorithm uses a hash function to authenticate the message. The algorithm requires two calls SHA-1, SHA-224, SHA-256 or MD5 hash function. For a message as long as $(264 - 1)$ bits, the hash processor calculates the message digest (SHA-1 The algorithm is 160 bits, and the SHA-256 algorithm is 256 bits, SHA-224 algorithm is 224 The MD5 algorithm is 128 bits).

### 13.9. General Purpose Input/Output (GPIOs)

Each GPIO pin can be configured by software as an output (push-pull or open-drain, with or without pull-up/pull-down), input (floating, with or without pull-up/pull-down), or peripheral multiplexing function. Most GPIO pins have digital or analog multiplexing functions. All GPIOs have high current capabilities and have speed selection to better manage internal noise, power consumption, and electromagnetic radiation.

If desired, the I/O configuration can be locked after a specific sequence to avoid accidental writes to the I/O registers.

Except for DAC and USB multiplexed I/O, other I/Os support 5v-input tolerant.

### 13.10. Analog-to-Digital Converters (ADCs)

There are three built-in 12-bit analog-to-digital converters (ADCs), each of which can share up to 16 external channels and perform conversions in single-shot or scan mode. In scan mode, automatic conversions are performed on a selected group of analog inputs.

Other logic functions built into the ADC interface allow:

- Synchronous Sample and Hold
- Interleaved

The ADC can use the DMA controller to very accurately monitor the conversion voltage of one, multiple or all selected channels using the analog watchdog function, and generate an interrupt when the conversion voltage exceeds the programmed threshold.

To synchronize the A/D conversion and the timer, the ADC can be triggered by any of the timers TIM1, TIM2, TIM3, TIM4, TIM5, and TIM8.

### 13.11. Temperature Sensor

The temperature sensor must produce a voltage that varies linearly with temperature. The conversion range is 2.0 V to 3.6 V. The temperature sensor is internally connected to VBAT，the same input channel of ADC1_IN18, which is used to convert the sensor output voltage to a digital value. When both the temperature sensor and VBAT conversion are enabled，only the VBAT conversion is performed.

Due to different processes, the offset of the temperature sensor varies from chip to chip, so the internal temperature sensor is mainly suitable for applications that detect

temperature changes rather than applications that detect absolute temperature. If you need to read the exact temperature, you should use an external temperature sensor.

The on-chip temperature sensor can obtain the temperature inside the chip. After the temperature measurement is started using software or hardware trigger, the test result needs to be sampled through ADC1_IN18 and the temperature value is calculated using the formula.

### 13.12. Digital-to-Analog Converter (DAC)

Two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

The DAC supports the following functions:

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- In 12-bit mode, data is left-aligned or right-aligned
- Synchronous update function
- Generate noise waves
- Generate a triangle wave
- DAC dual channels convert individually or simultaneously
- Each channel has DMA function
- Conversion by external trigger signal
- Input reference voltage V REF+

The chip uses 8 DAC trigger inputs, and the DAC channels are triggered via timer update outputs, which are also connected to different DMA data streams.

### 13.13. Serial Wire JTAG Debug Port (SWJ-DP)

The built-in SWJ-DP interface is a combination of JTAG and Serial Wire Debug ports, enabling either a Serial Wire Debug probe or a JTAG probe to be connected to the target.

Debugging is performed using only 2 pins instead of 5 required by JTAG (JTAG pins can be reused as GPIOs with multiplexed functionality): JTAG TMS and TCK pins are shared with SWDIO and SWCLK respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

## XIV. Electrical Characteristics

### 14.1. Parameter conditions

All voltages are referenced to $V_{SS}$.

#### 14.1.1. Minimum and Maximum Values

All devices are tested during production for minimum and maximum values at ambient temperatures of $TA = 25°C$ and $TA_{max}$ (depending on the selected device temperature range).

#### 14.1.2. Typical Value

Typical data are tested under the conditions of $T_A$ = 25℃, $VDD = 3.3V$ .

### 14.2. Absolute Maximum Ratings

The chip cannot be operated under any conditions exceeding this value . If it is exceeded, it may cause permanent damage to the chip. And long-term operation under the maximum rated value may affect the reliability of the chip.

#### 14.2.1. Limit voltage characteristics

Table 4 -1Limit voltage list

| SYMBOL | RATING | MINIMUM | MAXIMUM | UNIT |
|---|---|---|---|---|
| VDD | External main power supply (including $V_{DDA}$ ,$V_{DD}$ ,$V_{BAT}$) | -0.3 | 4.0 | V |
| $V_{IN}$ | Input voltage on FT pin | $V_{SS}$ -0.3 | $V_{SS}$ + 4 | |
| | Any other input voltage on the pin | $V_{SS}$ -0.3 | 4.0 | |
| | Input voltage on BOOT pin | $V_{SS}$ | 4.0 | |
| $V_{ESD(HBM)}$ | Electrostatic Discharge Voltage (Human Body Model) | +25°C 2000V | | |

### 14.2.2. Limiting current characteristics

Table 4 -2Limiting current characteristics

| SYMBOL | RATING | MAXIMUM | UNIT |
|---|---|---|---|
| $\Sigma I_{VDD}$ | flowing into all $V_{DD}$ supply rails (sourcing current) (1) | 300 | mA |
| $\Sigma I_{VSS}$ | Total current drawn from all $V_{SS}$ ground rails (sinking current) (1) | -300 | |
| $I_{VDD}$ | flowing into each $VDD\_x_{supply}$ line (source current) (1) | 25 | |
| $I_{VSS}$ | Maximum current that can flow from each $VSS\_x$ ground line (sink current) (1) | -25 | |
| $I_{IO}$ | Current sinking for any I/O and control pin output | 20 | |
| | Any I/O and control pin can source current | -20 | |
| $\Sigma I_{IO}$ | Total current sunk by all I/O and control pins | 100 | |
| | Total current sunk by all USB I/O outputs | 20 | |
| | Total current sourced by all I/O and control pins | -100 | |
| $I_{INJ(PIN)}$ | Injection current on FT, RST and B pins | -5/+0 | |
| | Injection current on TTa pin | ±5 | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (all I/O and control pins) | ±25 | |

- All power and ground pins must remain connected to the external power supply at all times .

# XV. Working Parameters

## 15.1. Extreme temperature characteristics

- Storage temperature range ( TSTG): -65 °C to + 150°C
- Maximum Junction Temperature (TJ): 1 50°C

## 15.2. Recommended operating conditions

Table 4 -1Recommended working conditions

| SYMBOL | PARAMETER | CONDITION | | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|---|
| fHCLK | Internal AHB clock frequency | Power settings: VOS[1:0]=0x01 in PWR_CR register, voltage regulator ON, over -drive OFF | | 0 | - | 144 | MHz |
| | | Power setting: VOS[1:0]=0x10 in PWR_CR register, voltage regulator ON | Overload OFF | 0 | - | 168 | |
| | | | Overload ON | | - | 180 | |
| | | Power setting: VOS[1:0]=0x11 in PWR_CR register, voltage regulator ON | Overload OFF | 0 | - | 180 | |
| | | | Overload ON | | - | 180 | |
| VDD | Standard operating voltage | - | | 2.1 | - | 3.6 | V |
| $V_{DDA}$ | Analog operating voltage | - | | 2.1 | - | 3.6 | |
| $V_{BAT}$ | Backup working voltage | | | 2.0 | - | 3.6 | |
| $V_{IN}$ | Input voltage on RST and FT pins | 2.0V≤VDD≤3.6V | | -0.3 | - | 5.5 | |
| | | VDD≤2V | | -0.3 | - | 5.2 | |
| | Input voltage on TTa pin | - | | -0.3 | - | $V_{DDA}$ | |

### 15.3. VCAP1/VCAP2 external capacitor

The internal voltage regulator requires external capacitors connected through the VCAP1/VCAP2 pins to achieve voltage regulation. The external capacitors are specified as CEXT must be limited to ensure that the drive current does not exceed the absolute maximum ratings specified in Table 4-2.

#### 15.3.1. Output voltage

Table 4 -2Output voltage characteristics

| SYMBOL | PARAMETER | CONDITION (UNLESS OTHERWISE SPECIFIED, -40℃ ≤ T A ≤ 125℃) | MINIMUM | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| V OL | Output low level | I IO = 4 mA 2.1 V ≤ V DD ≤ 3.6 V | - | 0.3V DD | V |
| V O H | Output high level | I IO = 4 mA, except PC13, PC14, PC15 2.1 V ≤ V DD ≤ 3.6 V | 0.7V DD | | |
| V O H | Output high level | I IO = 4 mA, PC13, PC14, PC15 2.1 V ≤ V DD ≤ 3.6 V | 0.7V DD | | V |

#### 15.3.2. Input/Output AC Characteristics

The speed is configured by the OSPEEDRy[ 1:0] bits . For a description of the GPIOx SPEEDR GPIO port output speed register, refer to the BST32F 4 xx Technical Reference Manual. If the maximum GPIO frequency exceeds 50MHz, a compensation unit should be used.

The input/output AC characteristics are given in Table 4 -20.

Table 4 -3. GPIO AC Characteristics (1)

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| tEXTIpw | EXTI Pulse width of the external signal detected by the controller | - | | 10 | | ns |

- Guaranteed by design, not tested in production.

## 15.4. NRST Pin Characteristics

The NRST pin input driver is CMOS technology. It is connected to a permanent pull-up resistor $R_{PU}$ ( see Table 4 -21).

Table 4 -4. NRST Pin Characteristics

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| R PU | Weak pull-up equivalent resistor (1) | V IN =V SS | 30 | 40 | 5 0 | kΩ |
| T NRST_OUT | The duration of the reset pulse generated | Internal reset source | 20 | - | | μs |

## 15.5. TIM counter characteristics

Table 4 -5. TIMx features (1)

| SYMBOL | PARAMETER | CONDITION | MINIMUM | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| t res(TIM) | Timer resolution time | | 1 | - | t TIMxCLK |
| f EXT | Timer external clock frequency on CH1 to CH4 | fTIMCLK = 180MHz | 0 | fTTIMxCLK / 2 | MHz |
| Res TIM | Timer resolution | | - | 16/32 | bit |

- Guaranteed by design, not tested in production.

### 15.6. 12-bit ADC Features

Table 4 -6. ADC Characteristics

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| V DDA | powered by | -40℃ ≤ TA ≤ 125℃ | 2.1 | - | 3.6 | V |
| V REF+ | Positive reference voltage | | 2.1 | - | V DDA | V |
| V AIN | Conversion voltage range (1) | - | | | V REF+ | V |
| R AIN | External input impedance (1) | - | | | 50 | kΩ |

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| f | Sampling frequency (f ADC = 22.5 MHz) | 12-bit resolution<br>Single ADC | | | 1.5 | Msps |

Table 4 -7. ADC static accuracy at fADC = 22.5 MHz

| SYMBOL | PARAMETER | TEST CONDITIONS | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| EO (2) | Offset Error | -40℃ ≤ T A ≤ 125℃<br>V DDA =V REF+ =3.3V | | ±4 | LSB |
| EG (3) | Gain Error | | | ±4 | |
| DNL | Differential linearity error | | | ± 3 | |
| INL | Integral linearity error | | | ± 3 | |

Table 4 -8. ADC dynamic accuracy at f ADC = 22.5 MHz

| SYMBOL | PARAMETER | TEST CONDITIONS | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| ENOB (1) | Significant digits | V DDA =V REF+ =3.3V<br>frequency = 20KHz<br>-40℃ ≤ T A ≤ 125℃ | 10.6 | 10. 8 | | bits |
| SINAD (1) | Signal to Noise and Distortion Ratio | | 64 | 6 7 | | dB |
| SNR | Signal-to-Noise Ratio | | 6 0 | | | |
| THD | Total harmonic frequency | | | -60 | | |

- Guaranteed by characterization results, not production tested.
- EO = Offset Error: The deviation between the first actual transition and the first ideal transition.
- EG = Gain Error: The deviation between the last ideal transition and the last actual transition.

### 15.7. DAC Electrical Characteristics

Table 4 -9DAC characteristics

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| V DDA | Analog supply voltage | -40℃ ≤ T A ≤ 125℃ | 2.1 | - | 3.6 | V |
| V REF+ | Reference supply voltage | | 2.1 | - | 3.6 | V |
| R LOAD ( 1) | resistance when the buffer is turned on | - | 5 | - | | kΩ |
| R O ( 1) | Output impedance when buffer is off | - | | - | 1 5 | kΩ |
| C LOAD ( 1) | Capacitive load | - | | - | 50 | pF |
| I VREF+ ( 2) | DAC current consumption in standby mode , No load, code=0X800 | - | | 170 | 240 | μA |
| I DDA ( 2) | DAC current consumption in quiescent mode (3) No load, code=OXF1C | - | | | 840 | μA |
| DNL ( 1) | Differential Linear Distortion | -40℃ ≤ T A ≤ 125℃, VDD = VDDA = 3.3V | -4 | - | 4 | LSB |
| INL ( 2) | Integral Nonlinearity | | -5 | - | 5 | LSB |
| OE | Offset Error No load, code=0X800 | | -10 | - | 10 | mV |
| GE | Gain Error | | - 1.5 | - | 1.5 | % |
| PSRR | Power Supply Rejection Ratio | | - 40 | - | - 40 | dB |

Guaranteed by design, not tested in production.

- Guaranteed by characterization results, not production tested.

### 15.8. Temperature Sensor Characteristics

Table 4 -10Temperature sensor characteristics

| SYMBOL | PARAMETER | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| T L (1) | VSENSE Linearity with Respect to Temperature | | ±1 | | ℃ |
| V 25 (1) | Voltage at 25℃ | | 0.76 | | V |
| t START (2) | Startup time | | 6 | | μs |

- Guaranteed by characteristic analysis results.
- Guaranteed by design.

## XVI. Communication interface

### 16.1. $^{2}$C Interface Characteristics

- I2C bus interface supports standard mode (up to 100 kHz) , fast mode (up to 400 kHz), and overspeed mode (up to 1 MHz)
- The I/O pins mapped to SDA and SCL are not "real" open-drain pins . When configured as open-drain pins, the PMOS connected between the I/O pin and $V_{DD}$ is disabled but still exists.
- Overdrive mode does not support 20mA output drive
- All $^{I2C}$ SDA and SCL I/Os have an internal analog filter. The analog filter characteristics can be found in the following table:

Table 4 -1I 2 C analog filter characteristics (1)

| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNIT |
|---|---|---|---|---|
| FWf | The maximum peak pulse width is limited by the analog filter | 50 | 260 | ns |

- Guaranteed by characterization results, not production tested.

### 16.2. SPI Interface Characteristics

Table 4 -2SPI electrical characteristics (1)

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| f SCK 1/t c(SCK) | SPI clock frequency | Main Mode 2.7≤V DD ≤3.6 | - | - | | MHz |
| | | Slave Mode 2.7 ≤V DD ≤3.6 | - | - | | |
| t su ( N SS) | NSS establishment time | Slave mode, SPI prescaler = 2 | 4xT p cl k | - | - | ns |
| t h ( N SS) | NSS hold time | Slave mode, SPI prescaler = 2 | 2xT p cl k | - | - | |
| t w (SCKH) t w(SCKL) | SCK high and low time | Main Mode | T p cl k -1 | T p cl k | T p cl k +1 | |
| t su (MI) | Data input setup time | Main Mode | | - | | ns |
| t su (SI) | | Slave Mode | | - | | |
| t h (MI) | Data input hold time | Main Mode | | - | | |
| t h (SI) | | Slave Mode | | - | | |
| t v (SO) | Data output valid time | Slave mode 2.7≤V DD ≤3.6V | | 6.5 | | |
| tv (MO) | | Main mode 2.7 ≤ V DD ≤ 3.6 V | | 2 | | |

- Guaranteed by characterization results, not production tested.

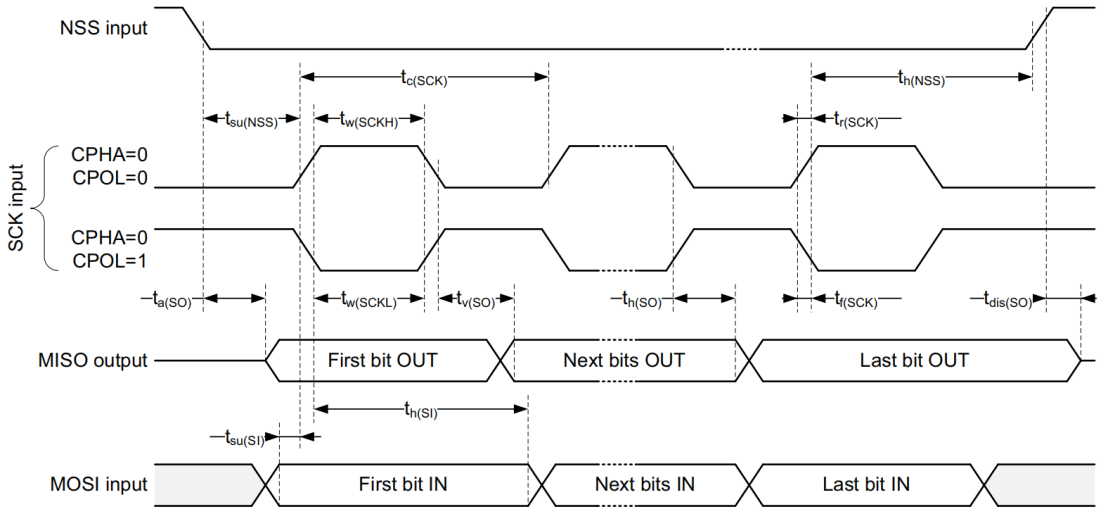


Figure 4-1SPI timing diagram - slave mode, CPHA=0

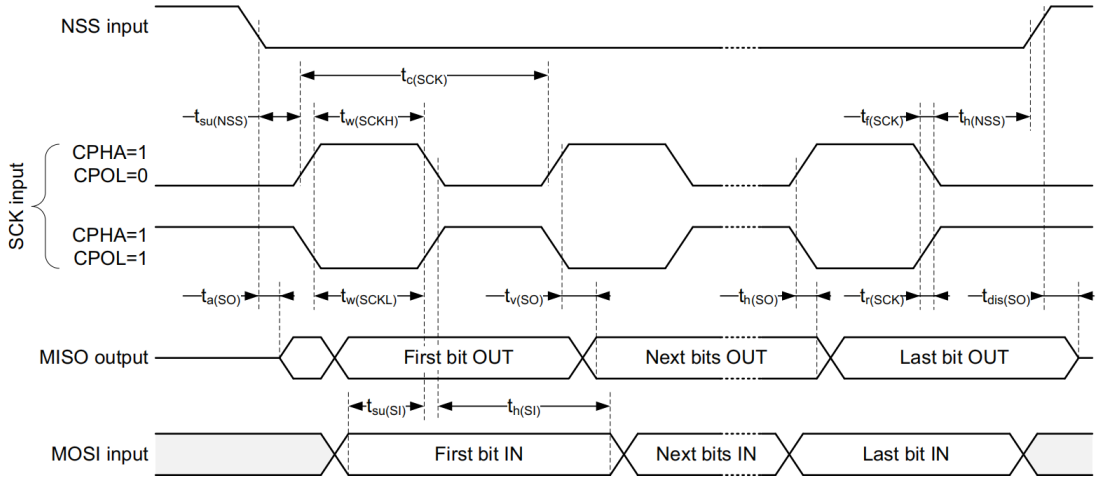


Figure 4-2SPI timing diagram - slave mode, CPHA=1

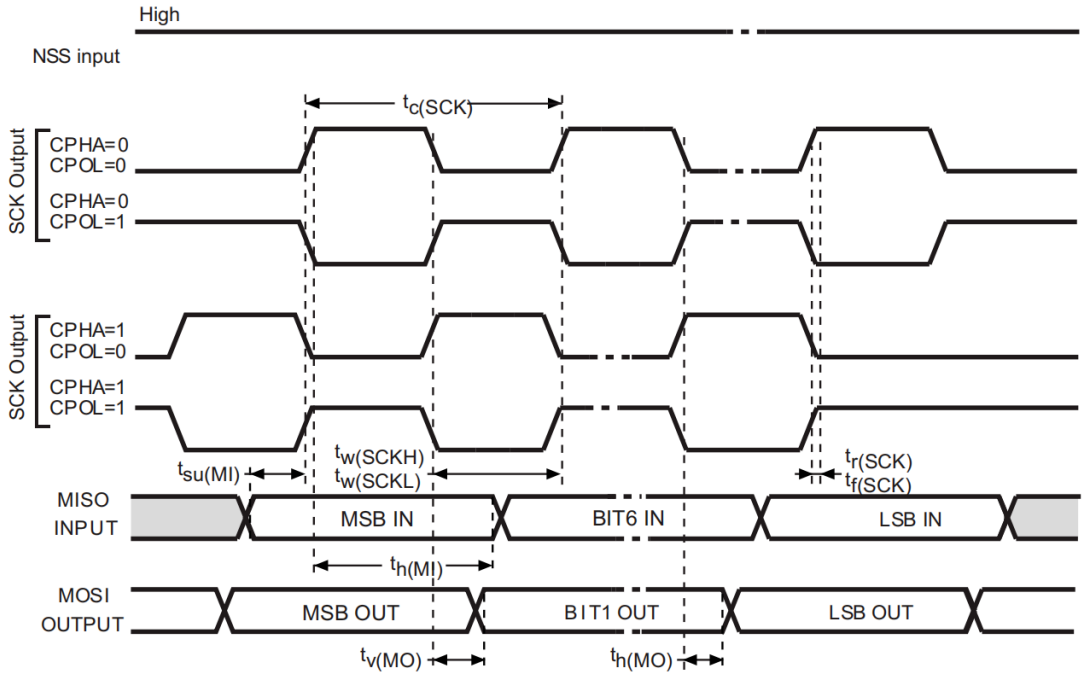


Figure 4-3SPI timing diagram - master mode

## 16.3. USB OTG Full Speed (FS) Features

This interface is available on both USB OTG HS and USB OTG FS controllers.

Table 4 -3 USB OTG Full Speed DC Electrical Characteristics

| SYMBOL | | PARAMETER | CONDITION | MINIMUM (1) | TYPICAL VALUE | MAXIMUM (1) | UNIT |
|---|---|---|---|---|---|---|---|
| Input Level | VDD | USB OTG FS operating voltage | - | 3.0 | - | 3.6 | V |
| | $V_{DI}$ (2) | Differential Input Sensitivity | I(USB_FS / HS_D + , USB_FS/HS_D- ) | 0.2 | - | | V |
| | $V_{CM}$ (2) | Differential common mode range | Includes $V_{DI}$ range | 0.8 | - | 2.5 | |
| | $V_{SE}$ (2) | Single-ended receive threshold | - | 1.3 | - | 2.0 | |
| Output Level | $V_{OL}$ | Static output low level | 1. 24 kΩ R L connected to 3.6 V (3) | | - | 0.3 | V |

| SYMBOL | | PARAMETER | CONDITION | MINIMUM (1) | TYPICAL VALUE | MAXIMUM (1) | UNIT |
|---|---|---|---|---|---|---|---|
| | V | Static output high level | 15kΩ $R_L$ to $V_{SS}$ (3) | 2.4 | - | 3.6 | |
| R | | PA11, PA12 ,PB14,PB15 (USB_FS /HS _D +/D-) pull-down resistor | $V_{IN}$ =$V_{DD}$ | 17 | - | 24 | kΩ |
| $R_{PU}$ | | PA12 (USB_FS /HS _D +) pull-up resistor | $V_{IN}$ =$V_{SS}$ , idle state | 1.5 | - | 2.1 | |

- All voltages are based on the equipment ground.
- Guaranteed by design, not tested in production.
- RL is the load connected to the USB OTG full-speed driver.

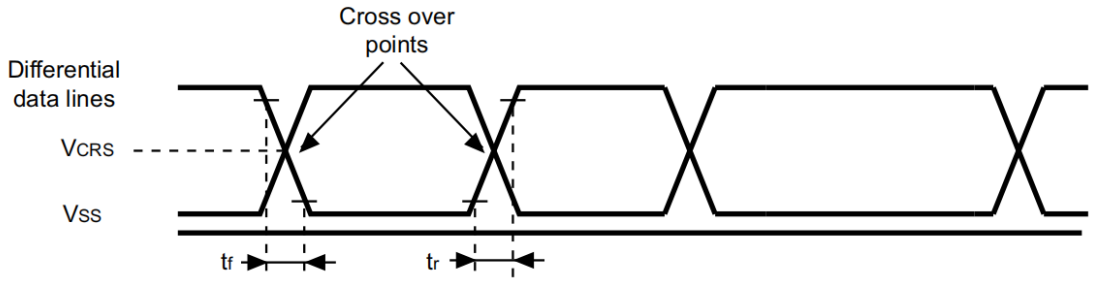


Figure 4 -4USB OTG full-speed timing: data signal rise and fall time definition

Table 4 -4USB OTG full-speed electrical characteristics (1)

| DRIVER CHARACTERISTICS | | | | | |
|---|---|---|---|---|---|
| SYMBOL | PARAMETER | CONDITION | MINIMUM | MAXIMUM | UNIT |
| t r | Rise time (2) | CL = 50pF | 4 | 20 | ns |
| t f | Fall time (2) | CL = 50pF | 4 | 20 | ns |
| t rfm | Rise/Fall Time Matching | t r /t f | 90 | 110 | % |
| V CRS | Output signal crossover voltage | - | 1.3 | 2.0 | V |
| Z DRV | Output drive impedance (3) | Drive high or low | 28 | 44 | Ω |

- Guaranteed by design, not tested in production.
- Measured between 10% and 90% of the data signal

### 16.4. USB High Speed (HS) features (via ULPI)

Table 4 -5USB HS DC electrical characteristics

| SYMBOL | | PARAMETER | MINIMUM (1) | MAXIMUM (1) | UNIT |
|---|---|---|---|---|---|
| Input Level | VDD | USB OTG HS operating voltage | 2.1 | 3. 6 | V |

- All voltages are referenced to the equipment end ground.

Table 4-6Dynamic characteristics: USB ULPI (1)

| SYMBOL | PARAMETER | CONDITION | MINIMUM | TYPICAL VALUE | MAXIMUM | UNIT |
|---|---|---|---|---|---|---|
| t SC | Control signal setup time (ULPI_DIR,ULPI_NXT) | 2.7V< VDD <3.6V C L =20pF OSPEEDRy[1:0]=11 | 2 | - | | ns |
| HC | Control signal holding time (ULPI_DIR,ULPI_NXT) | | 1.5 | - | | |
| SD | Data within the creation time | | 3 | - | | |
| t HD | Data within retention time | | 2.2 | - | | |
| t DC /t DD | Data/Control Output Delay | | | 6.5 | 8 | |

- Guaranteed by characterization results, not production tested.

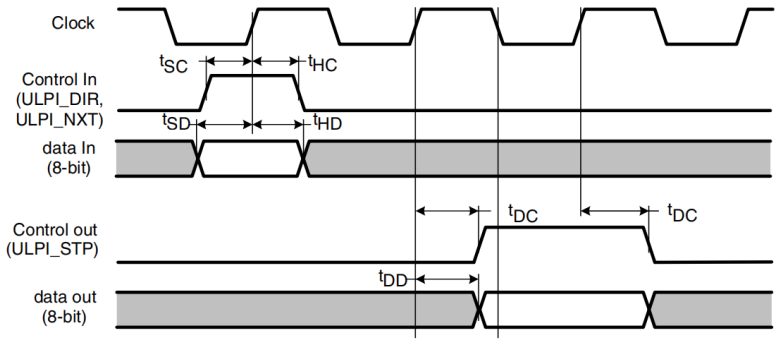


Figure 4-5ULPI timing diagram

# XVII. Package size

## 17.1. LQFP176 package

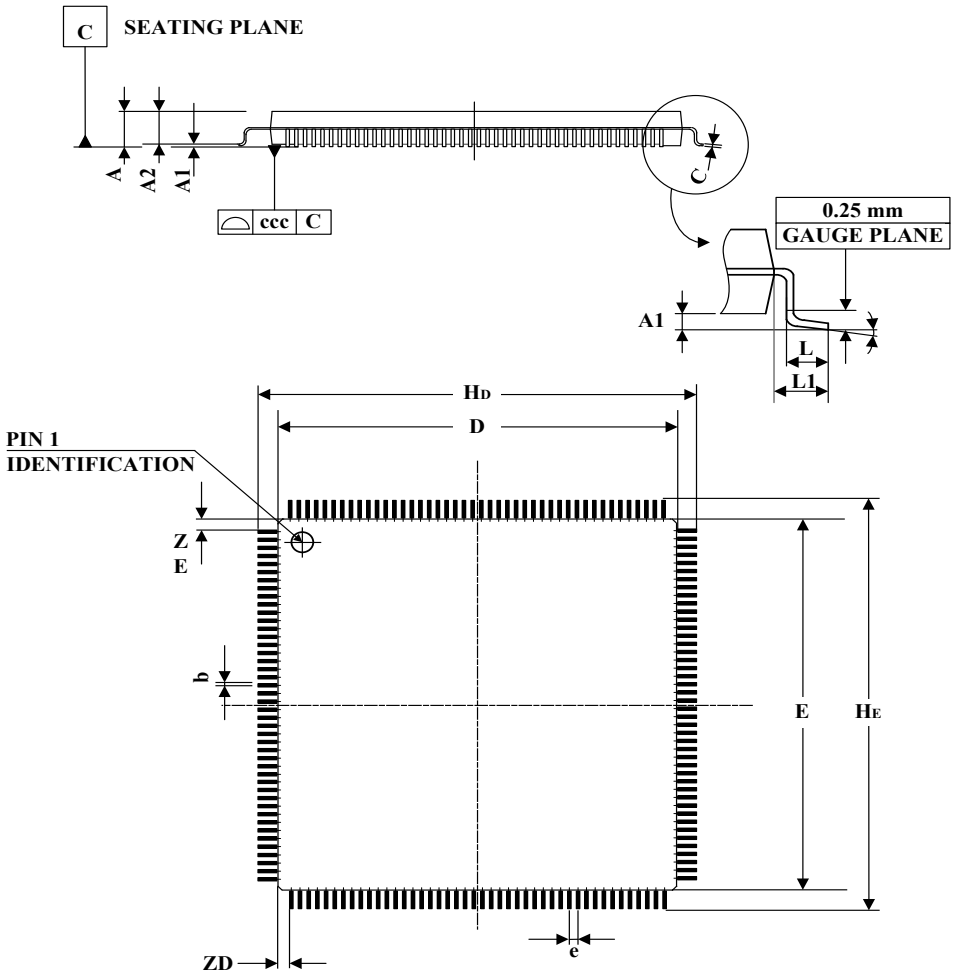


Figure 5-1. BST32F 4 07 L QFP 176 package diagram

Table 5-1Package size description

Unit is mm

| Dimension symbols | Numeric | | |
|---|---|---|---|
| | Minimum | Nominal | maximum |
| A | — | — | 1.60 |
| A 1 | 0.05 | — | 0.15 |
| A2 | 1.350 | — | 1.45 |

| Dimension symbols | Numeric | | |
|---|---|---|---|
| | Minimum | Nominal | maximum |
| b | 0.17 | — | 0.27 |
| c | 0.090 | — | 0.200 |
| D | 2 3.900 | — | 2 4.100 |
| E | 2 3.900 | — | 2 4.100 |
| e | — | 0.500 | — |
| HD | 2 5.800 | — | 26.200 |
| H E | 2 5.800 | — | 26.200 |
| L | 0.45 | — | 0.75 |
| L 1 | — | 1.000 | — |
| Z D | — | 1.250 | — |
| Z E | — | 1.250 | — |
| ccc | — | — | 0.08 |
| k | 0° | — | 7° |

## 17.2. LQFP144 package

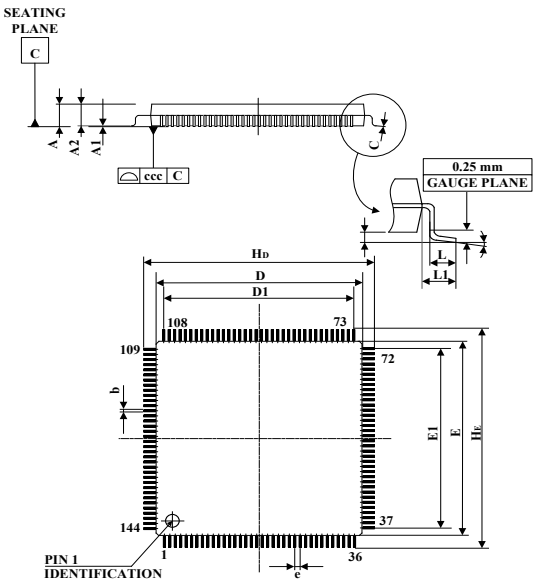


Figure 5-2. BST32F 4 07 L QFP144 package diagram

Table 5 -2Package size description

Unit is mm

| DIMENSION SYMBOLS | VALUE (MM) | | |
|---|---|---|---|
| | MINIMUM | TYPICAL | MAXIMUM |
| A | — | — | 1.700 |
| A 1 | 0.050 | — | 0.150 |
| A2 | 1.300 | 1.400 | 1.500 |
| b | 0.120 | 0.220 | 0.320 |
| c | 0.090 | — | 0.200 |
| HD | 2 1.700 | 22.000 | 22.300 |
| D | 19.700 | 2 0.000 | 20.300 |
| D1 | — | 17.500 | — |
| H E | 21.700 | 22.000 | 22.300 |
| E1 | — | 17.500 | — |
| E | 19.700 | 20.000 | 20.300 |
| e | | 0.500 | — |
| L | 0 .45 0 | 0.600 | 0.750 |
| L 1 | — | 1.000 | — |
| ccc | — | — | 0 .08 0 |
| k | 0° | 3.5 ° | 7° |

### 17.3. LQFP100 package

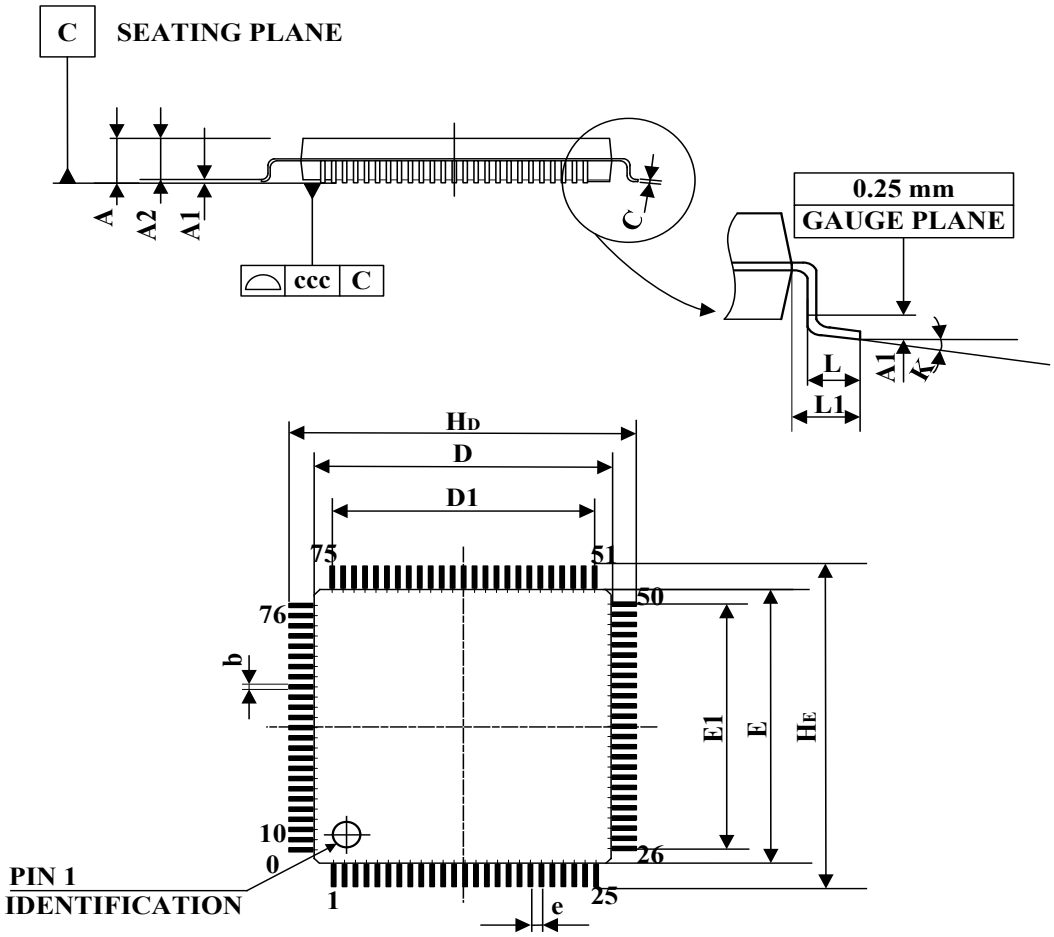


Figure 5-3. BST32F 4 L QFP100 package diagram

Table 5-3Package size description

Unit is mm

| DIMENSION SYMBOLS | VALUE (MM) | | |
|---|---|---|---|
| | MINIMUM | TYPICAL | MAXIMUM |
| A | — | — | 1.70 |
| A 1 | 0.05 | — | 0.15 |
| A2 | 1.250 | 1.400 | 1.55 |
| b | 0.120 | 0.220 | 0.320 |

| DIMENSION SYMBOLS | VALUE (MM) | | |
|---|---|---|---|
| | MINIMUM | TYPICAL | MAXIMUM |
| c | 0.040 | — | 0.250 |
| HD | 15.700 | 16.000 | 16.300 |
| D | 13.700 | 14.000 | 14.300 |
| D1 | — | 12.000 | — |
| H E | 15.700 | 16.000 | 16.300 |
| E | 13.700 | 14.000 | 14.300 |
| E1 | — | 12.000 | — |
| e | — | 0.500 | — |
| L | 0.45 | 0.600 | 0.750 |
| L 1 | — | 1.000 | — |
| ccc | — | — | 0.08 |
| k | 0° | 3.5 ° | 7° |

## 17.4. PBGA 1 76 package

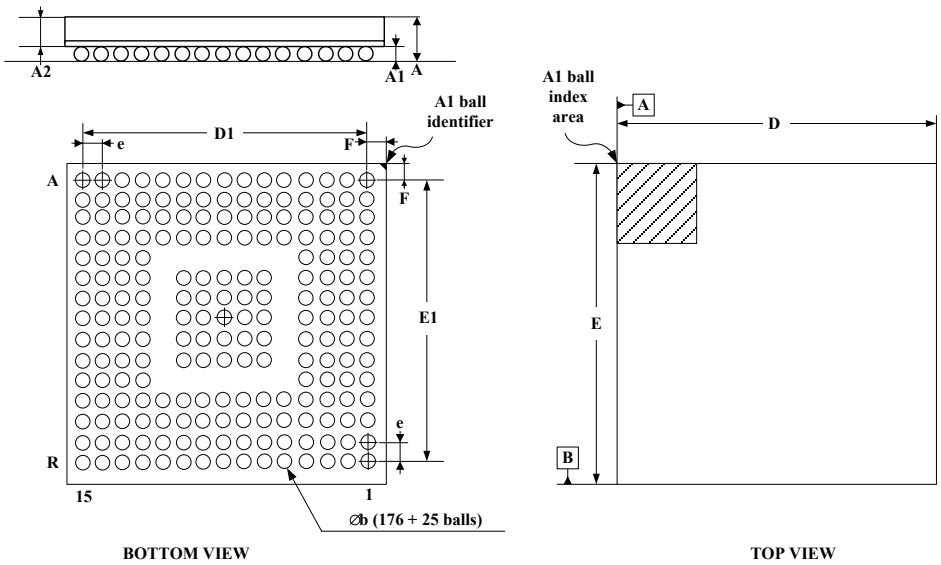


Figure 5-4. BST32F 4 07 PBGA176 package diagram

Table 5 -4Package size description

Unit is mm

| DIMENSION SYMBOLS | NUMERIC | | |
|---|---|---|---|
| | MINIMUM | TYPICAL | MAXIMUM |
| A | 1. 0 0 | — | 1.55 |
| A1 | — | — | 0.45 |
| A2 | — | — | 1.10 |
| b | | 0.40 | |
| D | 9. 80 0 | — | 10. 20 0 |
| D1 | | 9.100 | |
| E | 9. 8 0 0 | — | 10. 20 0 |
| E1 | | 9.1 | |
| e | — | 0.650 | — |

## XVIII. Ordering Information

Table 6-1Product ordering information

| PRODUCT MODEL | PACKAGE | MOQ | MPQ | PACKAGE | OPERATING TEMPERATURE | GRADE |
|---|---|---|---|---|---|---|
| BST32F 407LQFP176I | LQFP176 | 1 | 1 | tray | - 40 °～85° | industry |
| BST32F 407PBGA176I | PBGA176+25 | 1 | 1 | tray | - 40 °～85° | industry |
| BST32F 407LQFP 144 I | LQFP 144 | 1 | 1 | tray | - 40 °～85° | industry |
| BST32F 407LQFP1 00 I | LQFP1 00 | 1 | 1 | tray | - 40 °～85° | industry |
| BST32F 407LQFP 176 E | LQFP176 | 1 | 1 | tray | -55 ° ～ 125 ° | Military Temperature |
| BST32F 407PBGA 176 E | PBGA176+25 | 1 | 1 | tray | -55 ° ～ 125 ° | Military Temperature |
| BST32F 407LQFP 144 E | LQFP 144 | 1 | 1 | tray | -55 ° ～ 125 ° | Military Temperature |
| BST32F 407LQFP 100 E | LQFP1 00 | 1 | 1 | tray | -55 ° ～ 125 ° | Military Temperature |

| PRODUCT MODEL | PACKAGE | MOQ | MPQ | PACKAGE | OPERATING TEMPERATURE | GRADE |
|---|---|---|---|---|---|---|
| BST32F 407LQFP 176 M3 | LQFP176 | 1 | 1 | tray | -55 ° ～ 125 ° | N1 |
| BST32F 407PBGA 176 M3 | PBGA176+25 | 1 | 1 | tray | -55 ° ～ 125 ° | N1 |
| BST32F 407LQFP 144 M3 | LQFP 144 | 1 | 1 | tray | -55 ° ～ 125 ° | N1 |
| BST32F 407LQFP 100 M3 | LQFP1 00 | 1 | 1 | tray | -55 ° ～ 125 ° | N1 |
| BST32F 407CQFP 176 M1 | LQFP176 | 1 | 1 | tray | - 55 °～150° | B |
| BST32F 407CQFP 144 M1 | LQFP 144 | 1 | 1 | tray | - 55 °～150° | B |
| Additional notes:<br>For product quality grade description, please contact your local sales<br>For ceramic seal series products, please contact local sales for confirmation<br>For more F4 series products, please contact your local sales representative | | | | | | |

## XIX. Revision History

| SERIAL NUMBER | EDITION | CHANGE DESCRIPTION | CHANGE PERSON | CHANGE DATE | REMARK |
|---|---|---|---|---|---|
| 1 | V1.0 | Official version | HW | 2023.4 | |
| 2 | V1.1 | Supplement I2C4 pin multiplexing function | HW | 2023.5 | |
| 3 | V1.2 | Modify order model | HW | 2023.6 | |
| 4 | V1.21 | BGA pin labeling modification<br>LQFP series package size error correction | HW | 2023.6 | |
| 5 | V1.22 | Supplement USART1 pin multiplexing function | HW | 2023.8 | |
| 6 | V1.3 | Packaging parameter correction | HW | 2023.11 | |
| 7 | V1.31 | Modify BGA package size | HW | 2023.12 | |