BST32F1 Series
Datasheet v1.2

32-bit Cortex™-M3 core 72MHz main frequency, 512K FLASH, 128KB SRAM, 4KB backup SRAM storage, integrated USB OTG FS (built-in PHY), 10/100M Ethernet, 1 FSMC, 2 CAN, 5 USARTs, 3 SPIs, 2 I2Cs , 3 12-bit ADCs, 2 12-bit DACs, 2 advanced timers, 2 basic timers, 10 general timers, 1 window watchdog timer, 1 independent watchdog timer.

Product Features

Core: ARM 32-bit Cortex-M3 CPU, operating frequency 72MHz, performance of 1.25DMIPS/MHz at 0 wait state memory access Storage
512K FLASH
128Kbyte SRAM
4Kbyte backup SRAM Power management and reset
- VDD: 2.2v - 5.5v
- VBAT: 2.0v - 5.5v
USB 2.0 FS, built-in PHY
10/100 Ethernet MAC with dedicated DMA support and SRAM (4KB): IEEE 1588 hardware support
Storage interface: -
Variable storage controller (FSMC), including sram, nor flash, nand flash and psram
High performance simulation
3 12-bit, 1M ADC, up to 18CH - 2 12-bit DAC -

Built-in temperature sensor Algorithm modulePOR, PDR, PVD, BOR -

Support external pin reset, software reset, low power management reset, independent/window watchdog timer reset
 Low power consumption

Sleep, Stop and Standby modes
VBAT is used for RTC and backup registers ÿ Clock
- HSE (4-16MHz), LSE (32.769K)
HSI (8MHz), LSI (40KHz) ÿ Timer:
10 16-bit general
timers, 2 advanced timers (support motor PWM complementary output), 2 basic timers, 2 watchdog
timers
Communication interface

3 USARTs and 2 UARTs - 3 SPIs - 2 I2Cs ,
supporting SMBUS protocol - 2 CAN 2.0A/ B

CRC, RNG, HASH, CRYP

GPIO: Up to 112 GPIO ÿ Debug Mode - Serial debug SWD & JTAG interface.

- Cortex-M3 embedded trace macrocell

Power consumption: Current <300mA in operating mode

ESD: HBM2000V

Packaging:
LQFP48, LQFP64, LQFP100
LQFP144, BGA100
Quality grade:
Industrial grade (operating temperature -40℃~85℃)
Military grade (operating temperature -55℃ ~125℃)
N1 level (operating temperature -55℃ ~125℃)
Class B (operating temperature -55℃ ~125℃) Package compatibility: STM32F10X series

Product Introduction

The BST32F1 series is based on a high-performance 32-bit core with an operating voltage of 2.2V to 5.5V.
VBAT (battery powered) power supply function, embedded 512KB Flash, 128KB SRAM, 4KB backup
SRAM storage; 2 DMA; the circuit clock includes an external crystal oscillator 32.768KHz and 4MHzÿ16MHz, there are 8MHz and 40KHz RC oscillators on the chip; the highest output of the on-chip clock
72MHz.

The BST32F1 series has a large number of peripheral interfaces, including 2 I2C buses, 3 SPI interfaces, 1
USB OTG FS, 2 CAN, 3 USART and 2 UART, 1 EMAC interface,
3 12-bit ADCs and 2 12-bit DACs, as well as 2 advanced timers, 2 basic timers,
10 general-purpose timers, 1 window watchdog timer, 1 independent watchdog timer.

The low power modes supported by the BST32F1 series include sleep mode, stop mode, and standby mode. VBAT is used for RTC, backup registers, 4KB backup SRAM power supply, supports SWD&JTAG
Debug interface.

BST32F1 series provides LQFP48, LQFP64, LQFP100, LQFP144, BGA100

Package, package pin compatible with STM32F1 series

Model naming rules

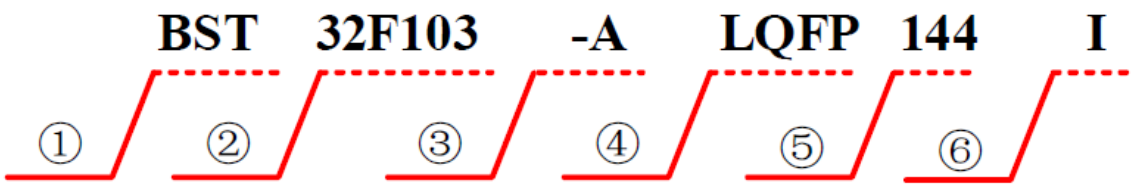


Figure 1-1 Model naming rules
32F103 represents the product model
Version ID: None means it is the first version of the product series
Packaging
Number of PIN pins
Grade: Commercial Grade C, Industrial Grade I, Wide Temperature W, Military Temperature E, Military Grade M

Model function comparison table

PIN		48PIN	64PIN	100PIn	144PIN
CPU maximum operating frequency and		72M			
operating voltage		2.2v~5.5v			
Operating temperature		-55℃~125℃(military temperature/N1/B) -40℃~85℃(Industrial)			
GPIO		35	49	80	112
Flash(KB)		512			
SRAM(KB)	System	128			
	Backup	4			
FSMC		Not supported		Support	
10/100M Ethernet		Not supported	Support		
Timer	General Timer	10			
	Advanced	2			
	Timer Basic Timer	2			
Communication interface	SPI	3			
	I2C	2			
	USART/UART	3×USARTs		3/2	
	USB OTG FS	1			
	CAN	2			
Simulate IP	12-bit ADC	2×ADCs	3 × ADCs, up to 18 channels, support interleaved		
	12-bit DAC	2			
Debug		SWD/JTAG			
Encapsulation		LQFP48	LQFP64	LQFP100 BGA100	LQFP144

Functional Block Diagram

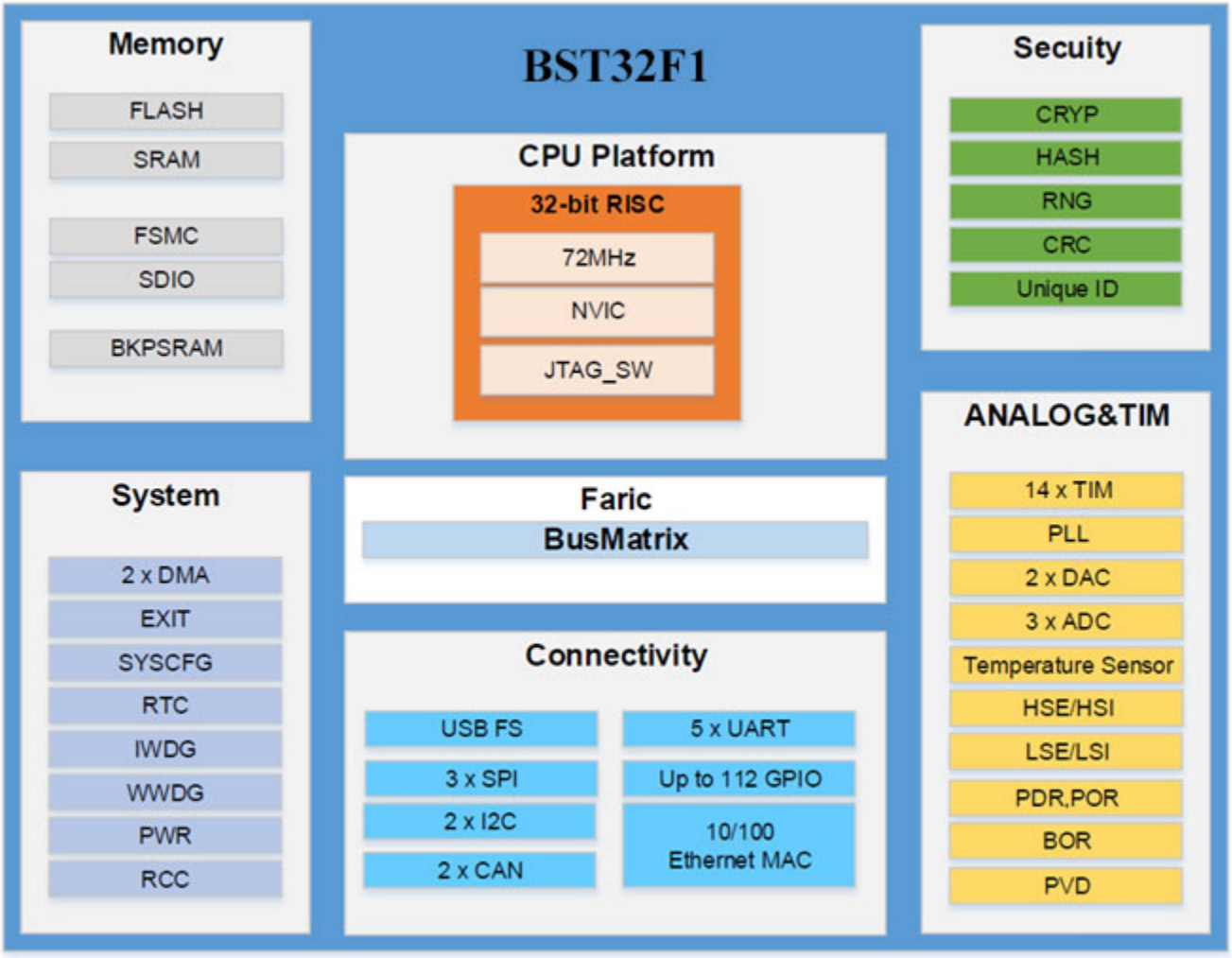


Figure 1-1 Functional block diagram

Product Pin Information

Package Pin Diagram

LQFP48 package

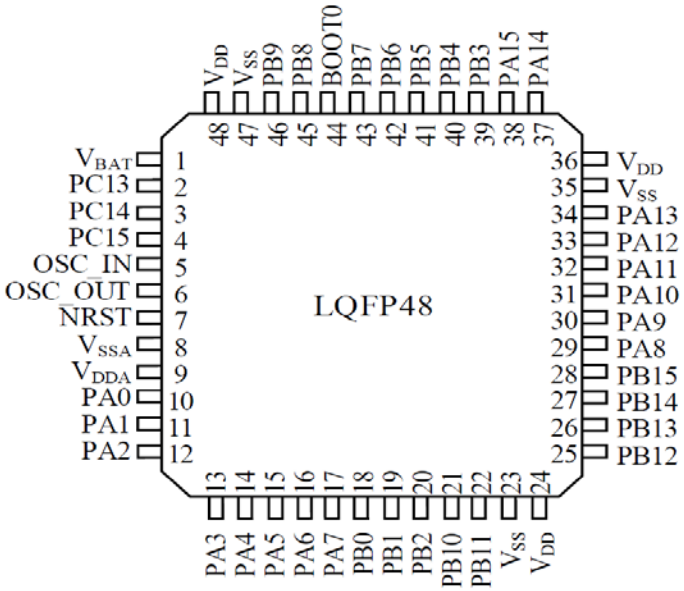


Figure 2-1 BST32F1 series LQFP48 pin arrangement and pin definition

LQFP64 package

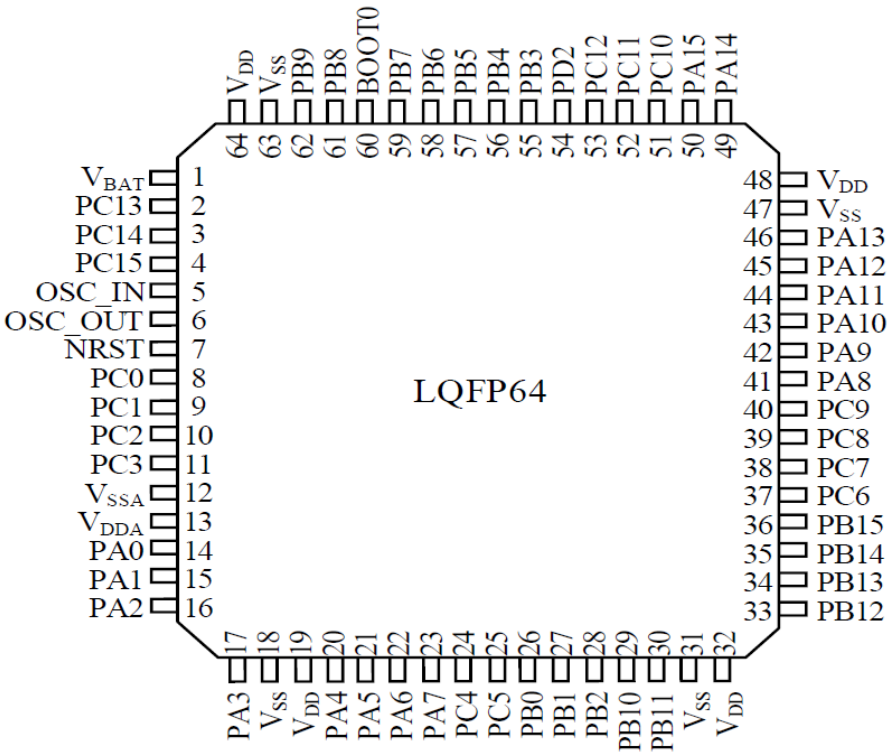


Figure 2-2 BST32F1 series LQFP64 pin arrangement and pin definition

LQFP100 package

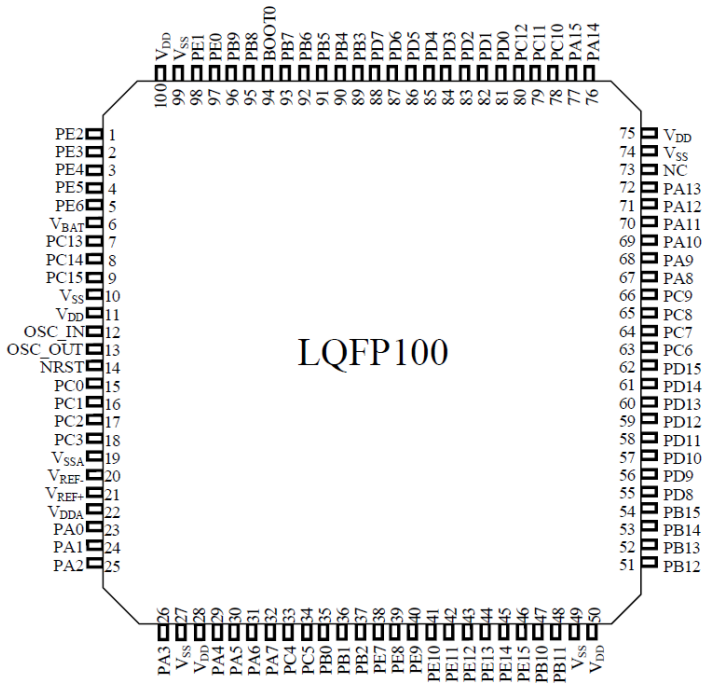


Figure 2-3 BST32F1 series LQFP100 pin arrangement and pin definition

PBGA100 package

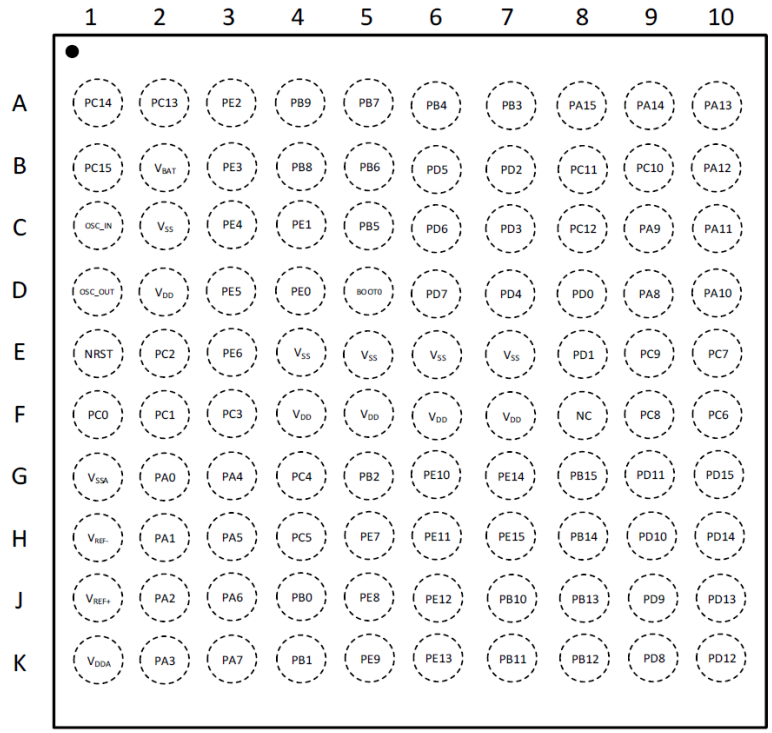


Figure 2-4 BST32F1 series PBGA100 pin arrangement and pin definition

LQFP144 package

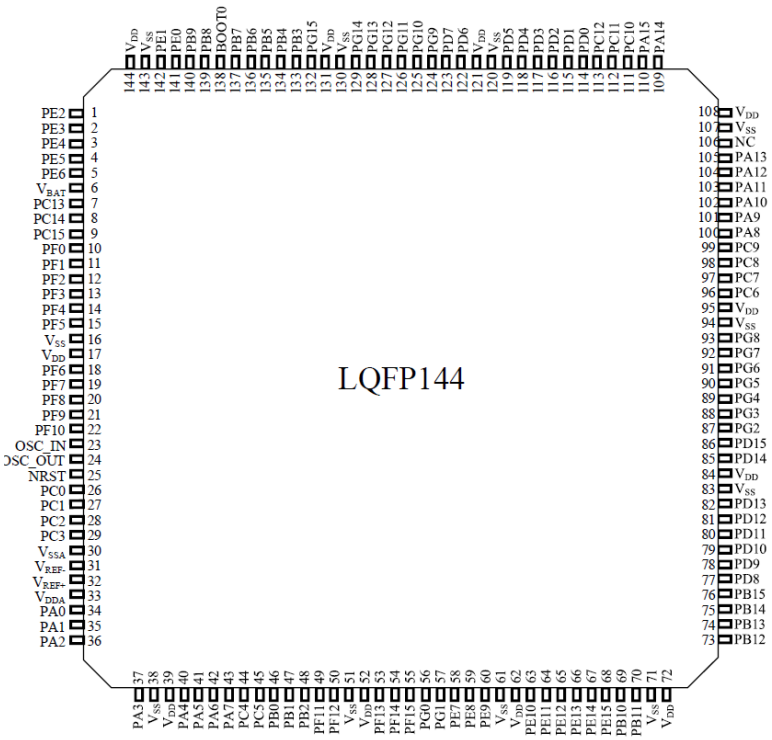


Figure 2-5 BST32F1 series LQFP144 pin arrangement

Pin function allocation table
Pin Function Definition

LQFP 48	LQFP 64	LQFP 100	BGA100	LQFP 144	Default after reset	Pinout type	I/O type	Digital functions	Simulation function
-	-	1	A3	1	PE2	I/O	FT	TRACECK、FSMC_A23、EVENTOUT	-
-	-	2	B3	2	PE3	I/O	FT	TRACED0、FSMC_A19、EVENTOUT	-
-	-	3	C3	3	PE4	I/O	FT	TRACED1、FSMC_A20、EVENTOUT	-
-	-	4	D3	4	PE5	I/O	FT	TRACED2、TIM9_CH1、FSMC_A21、EVENTOUT	-
-	-	5	E3	5	PE6	I/O	FT	TRACED3、TIM9_CH2、FSMC_A22、EVENTOUT	-
1	1	6	B2	6	VBAT	S	-	-	-
2	2	7	A2	7	PC13_WKUP 2	I/O	-	EVENTOUT	TAMPER_RTC
3	3	8	A1	8	PC14_OSC32_IN	I/O	-	EVENTOUT	OSC32_IN
4	4	9	B1	9	PC15_OSC32_OUT	I/O	-	EVENTOUT	OSC32_OUT
-	-	-	-	10	PF0	I/O	FT	FSMC_A0	-
-	-	-	-	11	PF1	I/O	FT	FSMC_A1	-
-	-	-	-	12	PF2	I/O	FT	FSMC_A2	-

LQFP 48	LQFP 64	LQFP 100	BGA100	LQFP 144	Default after reset	Pinout type	I/O type	Digital functions	Simulation function
-	-	-	-	13	PF3	I/O	FT	FSMC_A3	-
-	-	-	-	14	PF4	I/O	FT	FSMC_A4	-
-	-	-	-	15	PF5	I/O	FT	FSMC_A5	-
-	-	10	C2	16	VSS_5	S	-	-	-
-	-	11	D2	17	VDD_5	S	-	-	-
-	-	-	-	18	PF6	I/O	-	TIM10_CH1、FSMC_NIORD	ADC3_IN4
-	-	-	-	19	PF7	I/O	-	TIM11_CH1、FSMC_NREG	ADC3_IN5
-	-	-	-	20	PF8	I/O	-	TIM13_CH1、FSMC_NIOWR	ADC3_IN6
-	-	-	-	21	PF9	I/O	-	TIM14_CH1、FSMC_CD	ADC3_IN7
-	-	-	-	22	PF10	I/O	-	FSMC_INTR	ADC3_IN8
5	5	12	C1	23	OSC_IN	I	-	-	PD0
6	6	13	D1	24	OSC_OUT	O	-	-	PD1
7	7	14	E1	25	NRST	I/O	-	-	-
-	8	15	F1	26	PC0	I/O	-	EVENTOUT	ADC123_IN10
-	9	16	F2	27	PC1	I/O	-	ETH_MII_MDC/ETH_RMII_MDC、EVENTOUT	ADC123_IN11
-	10	17	E2	28	PC2	I/O	-	ETH_MII_TXD2、EVENTOUT	ADC123_IN12
-	11	18	F3	29	PC3	I/O	-	ETH_MII_TX_CLK、EVENTOUT	ADC123_IN13
8	12	19	G1	30	VSSA	S	-	-	-
-	-	20	H1	31	VREF_	S	-	-	-
-	-	21	J1	32	VREF+	S	-	-	-
9	13	22	K1	33	VDDA	S	-	-	-
10	14	23	G2	34	PA0_WKUP	I/O	-	TIM5_CH1、TIM2_CH1_ETR、TIM8_ETR、USART2_CTS、ETH_MII_CRS_WKUP、EVENTOUT	ADC123_IN0/WKU P
11	15	24	H2	35	PA1	I/O	-	TIM5_CH2、TIM2_CH2、USART2_RTS、ETH_MII_RX_CLK/ETH_RMII_REF_CLK、EVENTOUT	ADC123_IN1
12	16	25	J2	36	PA2	I/O	-	TIM5_CH3、TIM9_CH1、TIM2_CH3、USART2_TX、ETH_MII_MDIO/ETH_RMII_MDIO、EVENTOUT	ADC123_IN2
13	17	26	K2	37	PA3	I/O	-	TIM5_CH4、TIM9_CH2、TIM2_CH4、USART2_RX、	ADC123_IN3
								ETH_MII_COL、EVENTOUT	
-	18	27	E4	38	VSS_4	S	-	-	-
-	19	28	F4	39	VDD_4	S	-	-	-
14	20	29	G3	40	PA4	I/O	-	SPI1_NSS、USART2_CK、SPI3_NSS/I2S3_WS、EVENTOUT	ADC12_IN4/DAC_ OUT1
15	21	30	H3	41	PA5	I/O	-	SPI1_SCK、EVENTOUT	ADC12_IN5/DAC_ OUT2
16	22	31	J3	42	PA6	I/O	-	SPI1_MISO、TIM3_CH1、TIM13_CH1、TIM8_BKIN、	ADC12_IN6

LQFP 48	LQFP 64	LQFP 100	BGA100	LQFP 144	Default after reset	Pinout type	I/O type	Digital functions	Simulation function
								TIM1_BKIN、EVENTOUT	
17	23	32	K3	43	PA7	I/O	-	SPI1_MOSI、TIM3_CH2、TIM14_CH1、TIM8_CH1N、TIM1_CH1N、ETH_MII_RX_DV/ETH_RMII_CRS_DV、 EVENTOUT	ADC12_IN7
-	24	33	G4	44	PC4	I/O	-	ETH_MII_RXD0/ETH_RMII_RXD0、EVENTOUT	ADC12_IN14
-	25	34	H4	45	PC5	I/O	-	ETH_MII_RXD1/ETH_RMII_RXD1、EVENTOUT	ADC12_IN15
18	26	35	J4	46	PB0	I/O	-	TIM3_CH3、TIM8_CH2N、TIM1_CH2N、ETH_MII_RXD2、 EVENTOUT	ADC12_IN8
19	27	36	K4	47	PB1	I/O	-	TIM3_CH4、TIM8_CH3N、TIM1_CH3N、ETH_MII_RXD3、	ADC12_IN9
								EVENTOUT	
20	28	37	G5	48	PB2	I/O	FT	BOOT1、EVENTOUT	-
-	-	-	-	49	PF11	I/O	FT	FSMC_NIOS16	-
-	-	-	-	50	PF12	I/O	FT	FSMC_A6	-
-	-	-	-	51	VSS_6	S	-	-	-
-	-	-	-	52	VDD_6	S	-	-	-
-	-	-	-	53	PF13	I/O	FT	FSMC_A7	-
-	-	-	-	54	PF14	I/O	FT	FSMC_A8	-
-	-	-	-	55	PF15	I/O	FT	FSMC_A9	-
-	-	-	-	56	PG0	I/O	FT	FSMC_A10	-
-	-	-	-	57	PG1	I/O	FT	FSMC_A11	-
-	-	38	H5	58	PE7	I/O	FT	TIM1_ETR、FSMC_D4、EVENTOUT	-
-	-	39	J5	59	PE8	I/O	FT	TIM1_CH1N、FSMC_D5、EVENTOUT	-
-	-	40	K5	60	PE9	I/O	FT	TIM1_CH1、FSMC_D6、EVENTOUT	-
-	-	-	-	61	VSS_7	S	-	-	-
-	-	-	-	62	VDD_7	S	-	-	-
-	-	41	G6	63	PE10	I/O	FT	TIM1_CH2N、FSMC_D7、EVENTOUT	-
-	-	42	H6	64	PE11	I/O	FT	TIM1_CH2、FSMC_D8、EVENTOUT	-
-	-	43	J6	65	PE12	I/O	FT	TIM1_CH3N、FSMC_D9、EVENTOUT	-
-	-	44	K6	66	PE13	I/O	FT	TIM1_CH3、FSMC_D10、EVENTOUT	-
-	-	45	G7	67	PE14	I/O	FT	TIM1_CH4、FSMC_D11、EVENTOUT	-
-	-	46	H7	68	PE15	I/O	FT	TIM1_BKIN、FSMC_D12、EVENTOUT	-
21	29	47	J7	69	PB10	I/O	FT	I2C2_SCL、TIM2_CH3、USART3_TX、ETH_MII_RX_ER、 EVENTOUT	-
22	30	48	K7	70	PB11	I/O	FT	I2C2_SDA、TIM2_CH4、	-

LQFP 48	LQFP 64	LQFP 100	BGA100	LQFP 144	Default after reset	Pinout type	I/O type	Digital functions	Simulation function
								USART3_RX、ETH_MII_TX_EN/ETH_RMII_TX_EN、EVENTOUT	
23	31	49	E7	71	VSS_1	S	-	-	-
24	32	50	F7	72	VDD_1	S	-	-	-
25	33	51	K8	73	PB12	I/O	FT	SPI2_NSS/I2S2_WS、I2C2_SMBA、TIM1_BKIN、USART3_CK、CAN2_RX、	-
								ETH_MII_TXD0/ETH_RMII_TXD0、EVENTOUT	
26	34	52	J8	74	PB13	I/O	FT	SPI2_SCK/I2S2_CK、TIM1_CH1N、USART3_CTS、CAN2_TX、ETH_MII_TXD1/ETH_RMII_TXD1、EVENTOUT	-
27	35	53	H8	75	PB14	I/O	FT	SPI2_MISO、TIM12_CH1、TIM1_CH2N、USART3_RTS、EVENTOUT	-
28	36	54	G8	76	PB15	I/O	FT	SPI2_MOSI/I2S2_SD、TIM12_CH2、TIM1_CH3N、EVENTOUT	-
-	-	55	K9	77	PD8	I/O	FT	USART3_TX、ETH_MII_RX_DV/ETH_RMII_CRS_DV、 FSMC_D13、EVENTOUT	-
-	-	56	J9	78	PD9	I/O	FT	USART3_RX、ETH_MII_RXD0/ETH_RMII_RXD0、 FSMC_D14、EVENTOUT	-
-	-	57	H9	79	PD10	I/O	FT	USART3_CK、ETH_MII_RXD1/ETH_RMII_RXD1、 FSMC_D15、EVENTOUT	-
-	-	58	G9	80	PD11	I/O	FT	USART3_CTS、ETH_MII_RXD2、FSMC_A16、EVENTOUT	-
-	-	59	K10	81	PD12	I/O	FT	TIM4_CH1、USART3_RTS、ETH_MII_RXD3、FSMC_A17、EVENTOUT	-
-	-	60	J10	82	PD13	I/O	FT	TIM4_CH2、FSMC_A18、EVENTOUT	-
-	-	-	-	83	VSS_8	S	-	-	-
-	-	-	-	84	VDD_8	S	-	-	-
-	-	61	H10	85	PD14	I/O	FT	TIM4_CH3、FSMC_D0、EVENTOUT	-
-	-	62	G10	86	PD15	I/O	FT	TIM4_CH4、FSMC_D1、EVENTOUT	-
-	-	-	-	87	PG2	I/O	FT	FSMC_A12	-
-	-	-	-	88	PG3	I/O	FT	FSMC_A13	-
-	-	-	-	89	PG4	I/O	FT	FSMC_A14	-
-	-	-	-	90	PG5	I/O	FT	FSMC_A15	-
-	-	-	-	91	PG6	I/O	FT	FSMC_INT2	-
-	-	-	-	92	PG7	I/O	FT	FSMC_INT3	-
-	-	-	-	93	PG8	I/O	FT	-	-

LQFP 48	LQFP 64	LQFP 100	BGA100	LQFP 144	Default after reset	Pinout type	I/O type	Digital functions	Simulation function
-	-	-	-	94	VSS_9	S	-	-	-
-	-	-	-	95	VDD_9	S	-	-	-
-	37	63	F10	96	PC6	I/O	FT	I2S2_MCK、TIM8_CH1、TIM3_CH1、SDIO_D6、EVENTOUT	-
-	38	64	E10	97	PC7	I/O	FT	I2S3_MCK、TIM8_CH2、TIM3_CH2、SDIO_D7、EVENTOUT	-
-	39	65	F9	98	PC8	I/O	FT	TIM8_CH3、TIM3_CH3、SDIO_D0、EVENTOUT	-
-	40	66	E9	99	PC9	I/O	FT	TIM8_CH4、TIM3_CH4、SDIO_D1、EVENTOUT	-
29	41	67	D9	100	PA8	I/O	FT	MCO、TIM1_CH1、USART1_CK、OTG_FS_SOF、EVENTOUT	-
30	42	68	C9	101	PA9	I/O	FT	TIM1_CH2、USART1_TX、OTG_FS_VBUS、EVENTOUT	-
31	43	69	D10	102	PA10	I/O	FT	TIM1_CH3、USART1_RX、OTG_FS_ID、EVENTOUT	-
32	44	70	C10	103	PA11	I/O	FT	TIM1_CH4、USART1_CTS、CAN1_RX、OTG_FS_DM、EVENTOUT	-
33	45	71	B10	104	PA12	I/O	FT	TIM1_ETR、USART1_RTS、CAN1_TX、OTG_FS_DP、EVENTOUT	-
34	46	72	A10	105	PA13	I/O	FT	JTMS_SWDIO、EVENTOUT	-
-	-	73	F8	106	Notconnected		-	-	-
35	47	74	E6	107	VSS_2	S	-	-	-
36	48	75	F6	108	VDD_2	S	-	-	-
37	49	76	A9	109	PA14	I/O	FT	JTCK_SWCLK、EVENTOUT	-
38	50	77	A8	110	PA15	I/O	FT	JTDI、SPI3_NSS/I2S3_WS、TIM2_CH1_ETR、SPI1_NSS、EVENTOUT	-
-	51	78	B9	111	PC10	I/O	FT	UART4_TX、USART3_TX、SPI3_SCK/I2S3_CK、SDIO_D2、 EVENTOUT	-
-	52	79	B8	112	PC11	I/O	FT	UART4_RX、USART3_RX、SPI3_MISO、SDIO_D3、EVENTOUT	-
-	53	80	C8	113	PC12	I/O	FT	UART5_TX、USART3_CK、SPI3_MOSI/I2S3_SD、SDIO_CK、 EVENTOUT	-
-	-	81	D8	114	PD0_IN	I/O	FT	CAN1_RX、FSMC_D2、EVENTOUT	OSC_IN
-	-	82	E8	115	PD1_OUT	I/O	FT	CAN1_TX、FSMC_D3、EVENTOUT	OSC_OUT
	54	83	B7	116	PD2	I/O	FT	UART5_RX、TIM3_ETR、SDIO_CMD、EVENTOUT	-
-	-	84	C7	117	PD3	I/O	FT	USART2_CTS、FSMC_CLK、EVENTOUT	-
-	-	85	D7	118	PD4	I/O	FT	USART2_RTS、FSMC_NOE、EVENTOUT	-

LQFP 48	LQFP 64	LQFP 100	BGA100	LQFP 144	Default after reset	Pinout type	I/O type	Digital functions	Simulation function
-	-	86	B6	119	PD5	I/O	FT	USART2_TX、FSMC_NWE、EVENTOUT	-
-	-	-	-	120	VSS_10	S	-	-	-
-	-	-	-	121	VDD_10	S	-	-	-
-	-	87	C6	122	PD6	I/O	FT	USART2_RX、FSMC_NWAIT、EVENTOUT	-
-	-	88	D6	123	PD7	I/O	FT	USART2_CK、FSMC_NE1/FSMC_NCE2、EVENTOUT	-
-	-	-	-	124	PG9	I/O	FT	FSMC_NE2/FSMC_NCE3	-
-	-	-	-	125	PG10	I/O	FT	FSMC_NCE4_1/FSMC_NE3	-
-	-	-	-	126	PG11	I/O	FT	FSMC_NCE4_2	-
-	-	-	-	127	PG12	I/O	FT	FSMC_NE4	-
-	-	-	-	128	PG13	I/O	FT	FSMC_A24	-
-	-	-	-	129	PG14	I/O	FT	FSMC_A25	-
-	-	-	-	130	VSS_11	S	-	-	-
-	-	-	-	131	VDD_11	S	-	-	-
-	-	-	-	132	PG15	I/O	FT	-	-
39	55	89	A7	133	PB3	I/O	FT	JTDO_TRACESWO、SPI3_SCK/I2S3_CK、TIM2_CH2、 SPI1_SCK、EVENTOUT	-
40	56	90	A6	134	PB4	I/O	FT	NJTRST、SPI3_MISO、TIM3_CH1、SPI1_MISO、EVENTOUT	-
41	57	91	C5	135	PB5	I/O	-	SPI3_MOSI/I2S3_SD、I2C1_SMBA、TIM3_CH2、SPI1_MOSI、 CAN2_RX、ETH_MII_PPS_OUT/ETH_RMII_PPS_OUT、 EVENTOUT	-
42	58	92	B5	136	PB6	I/O	FT	TIM4_CH1、I2C1_SCL、USART1_TX、CAN2_TX、EVENTOUT	-
43	59	93	A5	137	PB7	I/O	FT	TIM4_CH2、I2C1_SDA、USART1_RX、FSMC_NADV、EVENTOUT	-
44	60	94	D5	138	BOOT0	I	-	-	-
45	61	95	B4	139	PB8	I/O	FT	TIM4_CH3、I2C1_SCL、TIM10_CH1、CAN1_RX、ETH_MII_TXD3、SDIO_D4、EVENTOUT	-
46	62	96	A4	140	PB9	I/O	FT	TIM4_CH4、I2C1_SDA、TIM11_CH1、CAN1_TX、SDIO_D5、 EVENTOUT	-
-	-	97	D4	141	PE0	I/O	FT	TIM4_ETR、FSMC_NBL0、EVENTOUT	-
-	-	98	C4	142	PE1	I/O	FT	FSMC_NBL1、EVENTOUT	-
47	63	99	E5	143	VSS_3	S	-	-	-
48	64	100	F5	144	VDD_3	S	-	-	-

Pin function multiplexing

PORT		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI1/2/I2S2/JTAG	SPI3/I2S3/UART4/5	TIM5	TIM3/4/9/12	TIM2/13/14/I2C1/2	TIM1/8	TIM1/2/3/4/9/10/11/13/14	USART1/2/3	SPI1	SPI3/I2S3/CAN1/2	OTG	ETH	FSMC/SDIO	-	-	SYS
PA	PA0	-	-	TIM5_CH1	-	TIM2_CH1_ETR	TIM8_ETR	-	USART2_CTS	-	-	-	ETH_MII_CRS_WKUP	-	-	-	EVENTOUT
	PA1	-	-	TIM5_CH2	-	TIM2_CH2	-	-	USART2_RTS	-	-	-	ETH_MII_RX_CLK/ETH_RMII_REF_CLK	-	-	-	EVENTOUT
	PA2	-	-	TIM5_CH3	TIM9_CH1	TIM2_CH3	-	-	USART2_TX	-	-	-	ETH_MII_MDIO/ETH_RMII_MDIO	-	-	-	EVENTOUT
	PA3	-	-	TIM5_CH4	TIM9_CH2	TIM2_CH4	-	-	USART2_RX	-	-	-	ETH_MII_COL	-	-	-	EVENTOUT
	PA4	SPI1_NSS	-	-	-	-	-	-	USART2_CK	-	SPI3_NSS/I2S3_WS	-	-	-	-	-	EVENTOUT
	PA5	SPI1_SCK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA6	SPI1_MISO	-	-	TIM3_CH1	TIM13_CH1	TIM8_BKIN	TIM1_BKIN	-	-	-	-	-	-	-	-	EVENTOUT
	PA7	SPI1_MOSI	-	-	TIM3_CH2	TIM14_CH1	TIM8_CH1N	TIM1_CH1N	-	-	-	-	ETH_MII_RX_DV/ETH_RMII_CRS_DV	-	-	-	EVENTOUT
	PA8	-	-	MCO	-	-	TIM1_CH1	-	USART1_CK	-	-	OTG_FS	-	-	-	-	EVENT

PORT		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI1/2/I2S2/JTAG	SPI3/I2S3/UART4/5	TIM5	TIM3/4/9/12	TIM2/13/14/I2C1/2	TIM1/8	TIM1/2/3/4/9/10/11/13/14	USART1/2/3	SPI1	SPI3/I2S3/CAN1/2	OTG	ETH	FSMC/SDIO	-	-	SYS
												_SOF					OUT
	PA9	-	-	-	-	-	TIM1_CH2	-	USART1_TX	-	-	OTG_FS_VBUS	-	-	-	-	EVENTOUT
	PA10	-	-	-	-	-	TIM1_CH3	-	USART1_RX	-	-	OTG_FS_ID	-	-	-	-	EVENTOUT
	PA11	-	-	-	-	-	TIM1_CH4	-	USART1_CTS	-	CAN1_RX	OTG_FS_DM	-	-	-	-	EVENTOUT
	PA12	-	-	-	-	-	TIM1_ETR	-	USART1_RTS	-	CAN1_TX	OTG_FS_DP	-	-	-	-	EVENTOUT
	PA13	JTMS_SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA14	JTCK_SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PA15	JTDI	SPI3_NSS/I2S3_WS	-	-	-	-	TIM2_CH1_ETR	-	SPI1_NSS	-	-	-	-	-	-	EVENTOUT
PB	PB0	-	-	-	TIM3_CH3	-	TIM8_CH2N	TIM1_CH2N	-	-	-	-	ETH_MII_RXD2	-	-	-	EVENTOUT
	PB1	-	-	-	TIM3_CH4	-	TIM8_CH3N	TIM1_CH3N	-	-	-	-	ETH_MII_RXD3	-	-	-	EVENTOUT
	PB2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB3	JTDO_TRACESWO	SPI3_SCK/I2S3_CK	-	-	-	-	TIM2_CH2	-	SPI1_SCK	-	-	-	-	-	-	EVENTOUT
	PB4	NJTRST	SPI3_MI	-	-	-	-	TIM3_C	-	SPI1_MI	-	-	-	-	-	-	EVENT
			SO					H1		SO							OUT

PORT		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI1/2/I2S2/JTAG	**SPI3/I2S3/UART4/5**	**TIM5**	**TIM3/4/9/12**	**TIM2/13/14/I2C1/2**	**TIM1/8**	**TIM1/2/3/4/9/10/11/13/14**	**USART1/2/3**	**SPI1**	**SPI3/I2S3/CAN1/2**	**OTG**	**ETH**	**FSMC/SDIO**	**-**	**-**	**SYS**
	PB5	-	SPI3_MOSI/I2S3_SD	-	-	I2C1_SMBA	-	TIM3_CH2	-	SPI1_MOSI	CAN2_RX	-	ETH_MII_PPS_OUT/ETH_RMII_PPS_OUT	-	-	-	EVENTOUT
	PB6	-	-	-	TIM4_CH1	I2C1_SCL	-	-	USART1_TX	-	CAN2_TX	-	-	-	-	-	EVENTOUT
	PB7		-	-	TIM4_CH2	I2C1_SDA	-	-	USART1_RX	-	-	-	-	FSMC_NADV	-	-	EVENTOUT
	PB8	-	-	-	TIM4_CH3	I2C1_SCL	-	TIM10_CH1	-	-	CAN1_RX	-	ETH_MII_TXD3	SDIO_D4	-	-	EVENTOUT
	PB9	-	-	-	TIM4_CH4	I2C1_SDA	-	TIM11_CH1	-	-	CAN1_TX	-	-	SDIO_D5	-	-	EVENTOUT
	PB10	-	-	-	-	I2C2_SCL	-	TIM2_CH3	USART3_TX	-	-	-	ETH_MII_RX_ER	-	-	-	EVENTOUT
	PB11	-	-	-	-	I2C2_SDA	-	TIM2_CH4	USART3_RX	-	-	-	ETH_MII_TX_EN/ETH_RMII_TX_EN	-	-	-	EVENTOUT
	PB12	SPI2_NSS/I2S2_WS	-	-	-	I2C2_SMBA	TIM1_BKIN	-	USART3_CK	-	CAN2_RX	-	ETH_MII_TXD0/ETH_RMII_TXD0	-	-	-	EVENTOUT
	PB13	SPI2_SCK/I2S2_CK	-	-	-	-	TIM1_CH1N	-	USART3_CTS	-	CAN2_TX	-	ETH_MII_TXD1/ETH_RMII_TXD1	-	-	-	EVENTOUT

PORT		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI1/2/I2S2/JTAG	**SPI3/I2S3/UART4/5**	**TIM5**	**TIM3/4/9/12**	**TIM2/13/14/I2C1/2**	**TIM1/8**	**TIM1/2/3/4/9/10/11/13/14**	**USART1/2/3**	**SPI1**	**SPI3/I2S3/CAN1/2**	**OTG**	**ETH**	**FSMC/SDIO**	**-**	**-**	**SYS**
	PB14	SPI2_MISO	-	-	TIM12_CH1	-	TIM1_CH2N	-	USART3_RTS	-	-	-	-	-	-	-	EVENTOUT
	PB15	SPI2_MOSI/I2S2_SD	-	-	TIM12_CH2	-	TIM1_CH3N	-	-	-	-	-	-	-	-	-	EVENTOUT
PC	PC0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC1	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_MDC/ETH_RMII_MDC	-	-	-	EVENTOUT
	PC2	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_TXD2	-	-	-	EVENTOUT
	PC3	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_TX_CLK	-	-	-	EVENTOUT
	PC4	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RXD0/ETH_RMII_RXD0	-	-	-	EVENTOUT
	PC5	-	-	-	-	-	-	-	-	-	-	-	ETH_MII_RXD1/ETH_RMII_RXD1	-	-	-	EVENTOUT
	PC6	I2S2_MCK	-	-	-	-	TIM8_CH1	TIM3_CH1	-	-	-	-	-	SDIO_D6	-	-	EVENTOUT
	PC7	-	I2S3_MCK	-	-	-	TIM8_CH2	TIM3_CH2	-	-	-	-	-	SDIO_D7	-	-	EVENTOUT

PORT		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI1/2/I2S2/JTAG	**SPI3/I2S3/UART4/5**	**TIM5**	**TIM3/4/9/12**	**TIM2/13/14/I2C1/2**	**TIM1/8**	**TIM1/2/3/4/9/10/11/13/14**	**USART1/2/3**	**SPI1**	**SPI3/I2S3/CAN1/2**	**OTG**	**ETH**	**FSMC/SDIO**	**-**	**-**	**SYS**
	PC8	-	-	-	-	-	TIM8_CH3	TIM3_CH3	-	-	-	-	-	SDIO_D0	-	-	EVENTOUT
	PC9	-	-	-	-	-	TIM8_CH4	TIM3_CH4	-	-	-	-	-	SDIO_D1	-	-	EVENTOUT
	PC10	-	UART4_TX	-	-	-	-	-	USART3_TX	-	SPI3_SCK/I2S3_CK	-	-	SDIO_D2	-	-	EVENTOUT
	PC11	-	UART4_RX	-	-	-	-	-	USART3_RX	-	SPI3_MISO	-	-	SDIO_D3	-	-	EVENTOUT
	PC12	-	UART5_TX	-	-	-	-	-	USART3_CK	-	SPI3_MOSI/I2S3_SD	-	-	SDIO_CK	-	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PD	PD0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	FSMC_D2	-	-	EVENTOUT
	PD1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	-	FSMC_D3	-	-	EVENTOUT
	PD2	-	UART5_RX	-	TIM3_ETR	-	-	-	-	-	-	-	-	SDIO_CMD	-	-	EVENTOUT
	PD3	-	-	-	-	-	-	-	USART2	-	-	-	-	FSMC_	-	-	EVENT
									_CTS					CLK			OUT

PORT		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI1/2/I2S2/JTAG	SPI3/I2S3/UART4/5	TIM5	TIM3/4/9/12	TIM2/13/14/I2C1/2	TIM1/8	TIM1/2/3/4/9/10/11/13/14	USART1/2/3	SPI1	SPI3/I2S3/CAN1/2	OTG	ETH	FSMC/SDIO	-	-	SYS
	PD4	-	-	-	-	-	-	-	USART2_RTS	-	-	-	-	FSMC_NOE	-	-	EVENTOUT
	PD5	-	-	-	-	-	-	-	USART2_TX	-	-	-	-	FSMC_NWE	-	-	EVENTOUT
	PD6	-	-	-	-	-	-	-	USART2_RX	-	-	-	-	FSMC_NWAIT	-	-	EVENTOUT
	PD7	-	-	-	-	-	-	-	USART2_CK	-	-	-	-	FSMC_NE1/FSMC_NCE2	-	-	EVENTOUT
	PD8	-	-	-	-	-	-	-	USART3_TX	-	-	-	ETH_MII_RX_DV/ETH_RMII_CRS_DV	FSMC_D13	-	-	EVENTOUT
	PD9	-	-	-	-	-	-	-	USART3_RX	-	-	-	ETH_MII_RXD0/ETH_RMII_RXD0	FSMC_D14	-	-	EVENTOUT
	PD10	-	-	-	-	-	-	-	USART3_CK	-	-	-	ETH_MII_RXD1/ETH_RMII_RXD1	FSMC_D15	-	-	EVENTOUT
	PD11	-	-	-	-	-	-	-	USART3_CTS	-	-	-	ETH_MII_RXD2	FSMC_A16	-	-	EVENTOUT
	PD12	-	-	-	-	-	-	TIM4_CH1	USART3_RTS	-	-	-	ETH_MII_RXD3	FSMC_A17	-	-	EVENTOUT
	PD13	-	-	-	-	-	-	TIM4_CH2	-	-	-	-	-	FSMC_A18	-	-	EVENT

PORT		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI1/2/I2S2/JTAG	SPI3/I2S3/UART4/5	TIM5	TIM3/4/9/12	TIM2/13/14/I2C1/2	TIM1/8	TIM1/2/3/4/9/10/11/13/14	USART1/2/3	SPI1	SPI3/I2S3/CAN1/2	OTG	ETH	FSMC/SDIO	-	-	SYS
																	OUT
	PD14	-	-	-	-	-	-	TIM4_CH3	-	-	-	-	-	FSMC_D0	-	-	EVENTOUT
	PD15	-	-	-	-	-	-	TIM4_CH4	-	-	-	-	-	FSMC_D1	-	-	EVENTOUT
PE	PE0	-	-	-	TIM4_ETR	-	-	-	-	-	-	-	-	FSMC_NBL0	-	-	EVENTOUT
	PE1	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_NBL1	-	-	EVENTOUT
	PE2	TRACECK	-	-	-	-	-	-	-	-	-	-	-	FSMC_A23	-	-	EVENTOUT
	PE3	TRACED0	-	-	-	-	-	-	-	-	-	-	-	FSMC_A19	-	-	EVENTOUT
	PE4	TRACED1	-	-	-	-	-	-	-	-	-	-	-	FSMC_A20	-	-	EVENTOUT
	PE5	TRACED2	-	-	-	-	-	TIM9_CH1	-	-	-	-	-	FSMC_A21	-	-	EVENTOUT
	PE6	TRACED3	-	-	-	-	-	TIM9_CH2	-	-	-	-	-	FSMC_A22	-	-	EVENTOUT
	PE7	-	-	-	-	-	-	TIM1_ETR	-	-	-	-	-	FSMC_D4	-	-	EVENTOUT
	PE8	-	-	-	-	-	-	TIM1_CH1N	-	-	-	-	-	FSMC_D5	-	-	EVENTOUT
	PE9	-	-	-	-	-	-	TIM1_CH1	-	-	-	-	-	FSMC_D6	-	-	EVENTOUT

PORT		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI1/2/I2S2/JTAG	SPI3/I2S3/UART4/5	TIM5	TIM3/4/9/12	TIM2/13/14/I2C1/2	TIM1/8	TIM1/2/3/4/9/10/11/13/14	USART1/2/3	SPI1	SPI3/I2S3/CAN1/2	OTG	ETH	FSMC/SDIO	-	-	SYS
	PE10	-	-	-	-	-	-	TIM1_CH2N	-	-	-	-	-	FSMC_D7	-	-	EVENTOUT
	PE11	-	-	-	-	-	-	TIM1_CH2	-	-	-	-	-	FSMC_D8	-	-	EVENTOUT
	PE12	-	-	-	-	-	-	TIM1_CH3N	-	-	-	-	-	FSMC_D9	-	-	EVENTOUT
	PE13	-	-	-	-	-	-	TIM1_CH3	-	-	-	-	-	FSMC_D10	-	-	EVENTOUT
	PE14	-	-	-	-	-	-	TIM1_CH4	-	-	-	-	-	FSMC_D11	-	-	EVENTOUT
	PE15	-	-	-	-	-	-	TIM1_BKIN	-	-	-	-	-	FSMC_D12	-	-	EVENTOUT
PF	PF0	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A0	-	-	-
	PF1	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A1	-	-	-
	PF2	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A2	-	-	-
	PF3	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A3	-	-	-
	PF4	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A4	-	-	-
	PF5	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A5	-	-	-
	PF6	-	-	-	-	-	-	TIM10_CH1	-	-	-	-	-	FSMC_NIORD	-	-	-
	PF7	-	-	-	-	-	-	TIM11_CH1	-	-	-	-	-	FSMC_NREG	-	-	-
	PF8	-	-	-	-	-	-	TIM13_CH1	-	-	-	-	-	FSMC_NIOWR	-	-	-
	PF9	-	-	-	-	-	-	TIM14_CH1	-	-	-	-	-	FSMC_CD	-	-	-

PORT		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI1/2/I2S2/JTAG	SPI3/I2S3/UART4/5	TIM5	TIM3/4/9/12	TIM2/13/14/I2C1/2	TIM1/8	TIM1/2/3/4/9/10/11/13/14	USART1/2/3	SPI1	SPI3/I2S3/CAN1/2	OTG	ETH	FSMC/SDIO	-	-	SYS
	PF10	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_INTR	-	-	-
	PF11	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_NIOS16	-	-	-
	PF12	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A6	-	-	-
	PF13	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A7	-	-	-
	PF14	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A8	-	-	-
	PF15	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A9	-	-	-
PG	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A10	-	-	-
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A11	-	-	-
	PG2	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A12	-	-	-
	PG3	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A13	-	-	-
	PG4	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A14	-	-	-
	PG5	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A15	-	-	-
	PG6	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_INT2	-	-	-
	PG7	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_INT3	-	-	-
	PG8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PG9	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_NE2/FSMC_NCE3	-	-	-
	PG10	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_NCE4_1/FSMC_NE3	-	-	-
	PG11	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_NCE4_2	-	-	-

PORT		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SPI1/2/I2S2/JTAG	SPI3/I2S3/UART4/5	TIM5	TIM3/4/9/12	TIM2/13/14/I2C1/2	TIM1/8	TIM1/2/3/4/9/10/11/13/14	USART1/2/3	SPI1	SPI3/I2S3/CAN1/2	OTG	ETH	FSMC/SDIO	-	-	SYS
	PG12	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_NE4	-	-	-
	PG13	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A24	-	-	-
	PG14	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A25	-	-	-
	PG15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Functional Description
CPU

The ARM Cortex™-M3 32-bit RISC processor is the latest generation of ARM for embedded systems. processor. It was developed to meet the needs of MCU, reduce the number of pins and reduce power consumption
A low-cost platform that provides both excellent computing performance and fast interrupt response
It has excellent code efficiency and offers significant savings in terms of memory footprint typically associated with 8-bit and 16-bit devices.
Provides the high performance expected from an ARM core

The BST32F1 series integrates the Cortex™-M3 32-bit RISC core processor, so it is compatible with all
The operating frequency is 72MHz, which reduces the number of pins and low power consumption.
It provides excellent computing performance and advanced system response to interrupts, which meets the needs of MCU implementation.
Low-cost platform.

Memory Mapping

For detailed information on the memory map and address boundaries of all peripherals, refer to the BST32F1 Series User Manual.
User Manual.

Embedded FLASH

The BST32F1 series products have built-in Flash memory up to 512KB, which can store programs and data.
according to.

On-chip SRAM

All products have built-in:
128KB system SRAM
4KB backup SRAM
Supports CPU access only and can retain data in Standby or VBAT mode

Variable Storage Controller (FSMC)

The Scalable Storage Controller (FSMC) includes three storage controllers:
SRAM/PSRAM memory controller
NOR FLASH controller
NAND FLASH controller
Key features of the FSMC controller include:
Static memory mapped device interface:
Static random access memory (SRAM)
NOR FLASH memory/NAND FLASH memory
PSRAM
NAND FLASH, ECC hardware check available up to 8KB data
8, 16, 32-bit data bus width
Each memory has independent chip select control
Each memory can be configured independently
FSMC_CLK maximum synchronous access frequency is HCLK/2

Direct Memory Access Controller (DMA)

The product has 2 general-purpose DMA controllers with a total of 12 channels (DMA1 has 7 channels, DMA2
Each channel is directly connected to a dedicated hardware DMA request.
The functions are configured by software. Circular buffer management is supported.
DMA-capable peripherals include: SPI, I2C, USART, general purpose, basic and advanced control timers
TIMx, DAC, SDIO, ADC.

Nested Vectored Interrupt Controller (NVIC)

The product has a built-in nested vectored interrupt controller with 16 programmable priority levels, using 4 bits
Interrupt priority, 68 maskable interrupt channels (excluding 16 interrupt lines of Cortex™-M3).

External Interrupt/Event Controller (EXTI)

The external interrupt (EXTI) is directly connected to the NVIC. EXTI contains 20 edge detectors for

Generate an interrupt request. Each interrupt line can be independently configured with its trigger event (rising edge, falling edge
edge, or both edges), and can be individually masked. Up to 16 of the external interrupt lines can be
Select the connection in GPIO.

Clock

At power-on reset, the core first uses the 8MHz internal HSI RC oscillator as the default clock.
The user can select the RC oscillator or external 4-16MHz clock source as the system clock source through register configuration.
The system clock can monitor the clock status and automatically switch to the internal RC oscillator when a clock failure is detected.
oscillator and also generates a software interrupt (if enabled).
The clock source can be multiplied to 72MHz by PLL inside the chip.
Clock monitoring and interrupt management.

Startup Mode

The boot mode can be selected through the BOOT pin and can be selected from the following three modes:
Boot from main flash memory
Boot from system memory
Boot from built-in SRAM

Power Supply Solution
Power supply solution
VDD = 2.2ÿ5.5V: VDD pin is used for GPIO pin and internal modules such as voltage regulator
(LDO) power supply
VDDA = 2.2ÿ5.5 V: ADC and DAC are powered through the VDDA pin . VDDA and VSSA Must be at the same potential as VDD and VSS
VBAT = 2.0 ~ 5.5 V: The VBAT pin allows external batteries, external supercapacitors to power the device.
The device can be powered from the VBAT domain, or from VDD when there is no external battery or external supercapacitor .
When no VDD is present, the VBAT pin (through the internal power switch) powers the RTC

Reset

This product integrates power-on reset (POR) and low-power management reset.
A low-power management reset is generated when the device is in stop mode.

Power supply monitoring

All products integrate a power-on reset (POR)/power-down reset (PDR) circuit and
At power-on, the POR/PDR is activated to ensure the MCU works properly.
The operating voltage is above 2.2v. When the 2.0v POR threshold level is reached, register configuration begins.
When VDD is lower than the specified threshold VPOR/PDR, the product will maintain the reset state without external reset circuit.
Hold reset mode.
The product also integrates a brownout reset (BOR), which is disabled by default and can be used to monitor VDD/VDDA.
A reset will occur when the voltage is below the detection threshold. The detection threshold is configurable with 8 levels in total.
The product also has an embedded programmable voltage detector (PVD) which can be used to monitor
VDD/VDDA power supply, threshold is configurable. PVD threshold can be configured directly through software.
16 gear configurations, can be turned off or enabled by the application program, when VDD/VDDA is lower than VPVD
threshold and/or VDD/VDDA is above the VPVD threshold, an interrupt is generated.
The program generates a warning message and puts the MCU into a safe state.

Internal voltage regulator (LDO)
There are two LDOs, Main-LDO and LPLDO. Main-LDO supplies power to the main logic.
LPLDO supplies power to the backup logic. Main-LDO supports three working modes:
MR Mode
MR mode is the normal operating mode of LDO. It has the strongest driving capability and can be used in Run mode.
mode or Sleep mode
LPR mode
LPR mode is the low power consumption mode of LDO. In this mode, the driving capability of LDO is reduced.
The power consumption of the controller itself is also minimized. LPR can only be used in Stop mode.
Power-down
In Power Down mode, the LDO is turned off and the 1.5V power output to the Core Domain is cut off.
This mode is only valid when entering Standby mode. Table 3-1 shows the chip in different working modes.
The operating modes that the step-down regulator can support

Table 3-1 LDO configuration mode and device operating mode

Mode Name	Enter	Wake	Maun LDO
Sleep	WIFI	Arbitrary interruption	MR Mode
	WFE	Wake-up event	

Stop	SLEEPDEEP bit +WFI or WFE	Any EXTI line (configured in the EXTI register, internal and external)	MR or LPR mode
Standby	PDDS bit +SLEEPDEEP position +WFI or WFE	WKUP pin rising edge, RTC, NRST pin external reset, IWDG reset	closure

Low Power Mode

The product supports three low power consumption modes:
Sleep: CPU stops, other peripherals can work normally
Stop: CPU stops, all high-frequency clocks stop
Standby: The Core Domain is powered off and all high-frequency clocks

VBAT Operation

When VDD is not powered, the chip can be powered by an external battery or super capacitor through the VBAT pin . The domain power supply, including: RTC, backup registers, and backup SRAM can all be powered by VBAT
Note: WhenVBAT When the chip is powered, external interrupts andRTC The alar/m event does not remove it from the VBAT Exit from working mode out.

Real-time clock (RTC), backup SRAM, backup register BKR

The real-time clock is an independent timer. The RTC module has a set of counters that count continuously.
Under the corresponding software configuration, the clock calendar function can be provided.
Modifying the value of the counter can reset the system
The current time and date.
The RTC and backup SRAM and backup register (BPR) are powered by a switch and are valid at VDD.
The switch selects VDD for power supply when the power is on, otherwise the power is supplied by the VBAT pin.
The RTC and backup SRAM, The BKP register is not reset.

Timer and Watchdog

The chip includes 2 advanced control timers, 10 general timers, 2 basic timers, 2 watch timers,

Table 3-2 compares the features of the advanced control timer, general timer, and basic timer. sex.

Timer Type	Timer	Counter	Counter Type resolution	Prescaler factor	DMA request is generated	Capture/Compare Channel	Complementary Output	Maximum interface clock (MHz) Complementary ou	Maximum timer clock (MHz)
Advanced Control	TIM1 TIM8	16 bit	Increment, decrement, increment/decrement	Any integer between 1and 65536	Yes	4	Yes	72	72
General	TIM2 TIM5	16 bit	Increment, Decrement, Increment/Decrement	Any integer between 1and 65536	Yes	4	No	72	36
	TIM3 TIM4	16 bit	Increment, Decrement, Increment/Decrement	Any integer between 1and 65536	Yes	4	No	72	36
	TIM9	16 bit	increment	Any integer between 1and 65536	No	2	No	72	72
	TIM10 TIM11	16 bit	increment	Any integer between 1and 65536	No	1	No	72	72
	TIM12	16 bit	increment	Any integer between 1and 65536	No	2	No	72	36
	TIM13 TIM14	16 bit	increment	Any integer between 1and 65536	No	1	No	72	36
Basics	TIM6 TIM7	16 bit	increment	Any integer between 1and 65536	Yes	0	No	72	36

Advanced Control Timer (TIM1, TIM8)

Advanced control timers (TIM1, TIM8) can be viewed as three-phase PWM multiplexed on 6 channels
They feature complementary PWM outputs with programmable dead-time insertion and can also be used as complete pass-through
Use with a timer.

4 independent channels can be used for:
Input capture
Output comparison
PWM generation (edge or center aligned mode)
Single pulse mode output
Advanced control timers can work with TIMx timers through the timer interconnection function to provide synchronization
Or event interconnection function.
TIM1 and TIM8 support the generation of independent DMA requests.

General purpose timer (TIMx)
The chip has 10 built-in synchronous general-purpose timers (see Table 3-2 for the differences).
TIM2, TIM3, TIM4 and TIM5
The BST32F1 series includes four full-featured general-purpose timers: TIM2, TIM3, TIM4, and TIM5.
It is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler.
All have 4 independent channels for input capture/output compare, PWM, and single pulse mode output.
In the largest package, up to 16 input capture/output compare/PWM are available.
TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together or through the timer chain feature
Works with other general purpose timers and advanced control timers TIM1 and TIM8 to achieve synchronization or
Event link.
Any general purpose timer can be used to generate PWM outputs.
TIM2, TIM3, TIM4, and TIM5 can generate independent DMA requests.
The MCU can process the digital outputs of 1 to 4 Hall Effect sensors.
TIM9, TIM10, TIM11, TIM12, TIM13, TIM14
These timers are based on a 16-bit auto-reload up-counter and a 16-bit prescaler.
TIM10, TIM11, TIM13, TIM14 have an independent channel, while TIM9 and TIM12
It has two independent channels for input capture/output compare, PWM, and single pulse mode output.
They can be synchronized with TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers.
As a simple time base.

Basic timers TIM6 and TIM7

These timers are primarily used to generate DAC trigger signals and waveforms, but can also be used as a general purpose 16-bit time base.
TIM6 and TIM7 support the generation of independent DMA requests
Independent Watchdog

The independent watchdog is based on a 12-bit down counter and 8 prescalers.
The internal RC provides the clock. Since the internal RC is independent of the main clock, it can be used in shutdown and standby modes.

It can be used as a watchdog to reset the device if a problem occurs, or as a free-running The timer can be set to provide timeout management for the application or software configuration.

Window Watchdog

The window watchdog is based on a 7-bit down counter that can be set to free-running. Resets the device if a problem occurs. It is driven by the main clock. It has an early warning interrupt function and is clocked
The counter can be frozen in debug mode.

SysTick Timer
This timer is designed for use in real-time operating systems, but can also be used as a standard down counter. It has the following features:
sex:
24-bit down counter
Automatic reload function
When the counter reaches 0, a maskable system interrupt is generated
Programmable clock source

Inter-Integrated Circuit Interface (I2C)
There are 2 I2Cs embedded in the device. Please refer to Table 3-3 to understand their functional implementation.
The I2C bus interface handles the communication between the chip and the I2C bus, controlling the timing, protocol, and
negotiation and arbitration.
The chip's I2C peripherals meet the following characteristics:
Compatible with I2C bus specification:
Master-slave mode, allowing multiple hosts.
Standard mode (Sm) with a maximum bit rate of 100 kb/s
Fast mode (Fm) with a maximum bit rate of 400 kb/s
7-bit and 10-bit addressing modes, allowing multiple 7-bit slave addresses
Programmable setup and hold time
Optional clock stretching
Compatible with SMBUS bus 2.0 specification
Hardware PEC (Packet Error Check) generation and acknowledgement with ACK control
Support Address Resolution Protocol (ARP)
SMBus Alert
1-byte buffer supporting DMA

Table 3-3 I2C Implementation

I2C Features (1)	I2C1 /2
Standard mode (up to 100 kbit/s)	x
Fast mode (up to 400kbit/s)	x
SMBus Hardware Support	x

1. X :support.

Universal Synchronous/Asynchronous Receiver/Transmitter (USART)
The BST32F1 series has three built-in universal synchronous/asynchronous receivers and transmitters (USART1, USART2,
USART3) and two Universal Asynchronous Receiver Transmitters (UART4 and UART5).
It supports asynchronous communication, IrDA SIR ENDEC, multi-processor communication, single-line half-duplex communication and LIN
Master/slave mode.
The USART1 serial port can communicate at a speed of up to 4.5Mbit/s. The communication speeds of other serial ports are 2.25Mbit/s.
USART1, USART2, USART3 also support hardware flow control (CTS/RTS), smart card mode
In addition to UART5, other serial ports Both support DMA communication.

Serial Peripheral Interface (SPI)
The chip has 3 SPIs, supporting master-slave mode, full-duplex, half-duplex and simplex communication modes.
Up to 18Mbit/s. The 3-bit prescaler can generate 8 main mode frequencies, and the frame can be configured to 8-16 bits.
All SPIs can use the DMA controller.

Controller Area Network (CAN)
Supports up to 2 CANs, compatible with CAN 2.0A and B specifications, with baud rates up to 1 Mbit/s.
Receive and send standard frames with 11-bit identifiers and extended frames with 29-bit identifiers. Each CAN
There are three transmit mailboxes, two three-stage receive FIFOs, and 28 adjustable shared filter banks.
The dual CANs share 512 bytes of SRAM memory (CAN2 cannot access it directly).

Universal Serial Bus on-the-go full speed (OTG_FS)
The device has a built-in USB OTG full-speed (12Mb/s) device/host/OTG transceiver
The USB OTG FS peripheral is compatible with the USB 2.0 specification and the OTG 1.0 specification.
The USB OTG controller requires a dedicated
Use a 48 MHz clock generated by a PLL connected to the HSE oscillator.
The main features are:
1.25KB of SRAM is only used by endpoints (not shared with other peripherals)
4 bidirectional control endpoints
Built-in HNP/SNP/IP (no external resistor required)
For OTG/Host mode, a power switch is required to prevent bus-powered devices from being connected
SOF output can be used to synchronize external DAC audio clock in synchronous mode
According to the USB 2.0 specification, the supported transfer rates are:
Host mode: full speed and low speed
Device mode: Full speed

Ethernet MAC interface: with dedicated DMA and support for IEEE 1588 standard
The BST32F1 series provides a media access controller (MAC) compliant with the IEEE-

802.3-2002 standard.
Through the standard media independent interface (MII) and reduced media independent interface (RMII)
For Ethernet LAN communication. The chip requires an external physical interface device (PHY) to connect to the LAN
The PHY is connected to the chip's MII port and uses up to 17 signal
1 signal (MII) or 9 signals (RMII), and can use 25MHz (MII) or 50MHz (RMII)
It outputs the clock. It has the following features:
Support 10/100 Mbit/s data transmission rate
Dedicated DMA controller allows high-speed transfer between SRAM and descriptors
Tagged MAC frame format (support VLAN)
Half-duplex (CSMA/CD) and full-duplex operation
Support MAC control sublayer (control frame)
32-bit CRC generation and deletion
Several address filtering modes for physical addresses and multicast addresses (multicast and group addresses)
Each sent or received frame supports a 32-bit status code
Internal FIFO is used for sending/receiving buffer, both sending FIFO and receiving FIFO are 2KB.
Supports hardware PTP (Precision Time Protocol) compliant with IEEE 1588, timestamp comparator
Connect to TIM2 input trigger.
Trigger an interrupt when the system time is greater than the target time

General Purpose Input/Output (GPIOs)

Each GPIO pin can be configured by software as an output (push-pull or open-drain), input (with or without
Most GPIO pins have digital or analog multiplexing functions. Yes. All GPIOs are capable of passing large currents.
If desired, the I/O configuration can be locked after a specific sequence to prevent accidental writes to the I/O registers operate.
The I/O switching on the APB2 can be up to 18MHz.

Analog-to-Digital Converter (ADC)

The BST32F1 series has three built-in 12-bit analog-to-digital converters, each ADC can share up to 16
external channels and perform conversions in single shot or scan mode. In scan mode, a group of selected
The analog input performs automatic conversion.
Additional logic functions built into the ADC interface allow:
Synchronous sampling and holding
Cross-sample and hold
Work independently
The ADC can use the DMA controller.

The analog watchdog function can be used to monitor the switching status of one, multiple or all selected channels very accurately.
When the transition voltage exceeds the programmed threshold, an interrupt is generated.
To synchronize A/D conversion and timers, standard timers (TIMx) and advanced control timers can be used.
The events generated by the (TIM1) are internally connected to the ADC start trigger and injection trigger respectively.

Digital-to-Analog Converter (DAC)
Two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signals
The selected design structure is composed of an integrated resistor string and an amplifier with an inverter structure.
The dual digital interface supports the following functions:
Two DAC converters: one for each output channel
8-bit or 12-bit monotonic output
In 12-bit mode, data is left-aligned or right-aligned
Synchronous update function
Generate noise waves
Generate triangle wave
DAC dual channels convert individually or simultaneously
Each channel has DMA function
Conversion by external trigger signal
Input reference voltage VREF+
The BST32F1 series uses 8 DAC trigger inputs. The DAC channels are updated through the timer output
These outputs are also connected to different DMA channels.

Temperature Sensor
The temperature sensor must produce a voltage that varies linearly with temperature. The conversion range is 2 V to 5.5 V.
The sensor is internally connected to the input channel of ADC1_IN16, which is used to convert the sensor output voltage
Converts the voltage into a digital value.

Cyclic Redundancy Check Calculation Unit (CRC)
The CRC (Cyclic Redundancy Check) calculation unit uses a polynomial generator with configurable value and size.
Generates a CRC code from a 32-bit data word. In many applications, CRC is often used to verify
Integrity of data transmission or storage.
Supports fully programmable polynomials
Support configurable data size
Support programmable CRC initial value
Input buffers to avoid bus congestion
Support reversibility option of IO data

True Random Number Generator (RNG)

The random signal source can generate true random number seeds for generating 64-bit true random numbers.

is disabled to reduce power consumption, the RNG module can generate pseudo-random sequences. The CPU can read the generatedRandom numbers. RNG main features:

Can generate 64-bit true random numbers

Random signal sources are disabled to reduce power consumption

Can generate pseudo-random sequences

Random numbers generated by random sources can be directly used

By monitoring abnormal behavior (producing stable values, or producing stable sequences of values)

Hash Processor (HASH)

The hash processor is fully compatible with the Secure Hash Algorithm (SHA-1, SHA-224 and SHA-256), MD5

(Message Digest Algorithm 5) hash algorithm and HMAC (Keyed-Hash Message Authentication

HMAC algorithm uses hash function to verify the message.

This method requires two calls to the SHA-1, SHA-224, SHA-256, or MD5 hash function.

(264–1) bits of the message, the hash processor computes the message digest (160 bits for the SHA-1 algorithm,

SHA-256 algorithm is 256 bits, SHA-224 algorithm is 224 bits, and MD5 algorithm is 128 bits).

Cryptographic Processor (CRYP)

With the help of the Cryptographic Processor (CRYP), DES, Triple-DES (3DES) or AES algorithms can be used

Encrypt and decrypt data. The encryption processor is fully compatible with the following standards:

Federal Information Processing Standards Publication (FIPS PUB 46-3, October 1999) and the U.S.

The Data Encryption Standard (DES) specified by the American National Standards Institute (ANSI X9.52) and

3DES (TDES)

The Federal Information Processing Standards Publication (FIPS PUB 197, November 2001) Advanced Encryption Standard (AES)

Supports multiple key sizes and chaining modes:

AES chaining modes ECB/CBC/OFB/CTR, supporting 128, 192 or 256 bit encryption Key size

DES/TDES chaining modes ECB and CBC, supporting standard 56-bit keys (each Key with 8-bit parity check)

Serial Wire JTAG Debug Port (SWJ-DP)

The built-in ARM SWJ-DP interface is a combination of JTAG and serial wire debug ports, which can be implemented

The JTAG interface is used to connect to the serial single-wire debug interface or JTAG interface. The TMS and TCK signals of JTAG are respectively connected to

SWDIO and SWCLK are shared, and the specified sequence on the TMS pin is used to communicate between JTAG-DP and
Switch between SW and DP

Electrical characteristics

Parameter conditions

All voltages are referenced to VSS.

Minimum and Maximum Values

All devices are tested during production at minimum and maximum values at an ambient temperature of
TA = 25°C and TAmax (depending on the temperature range of the selected device).

Typical values

Typical data are tested under the conditions of TA = 25ÿ, VDD = 3.3 V.

Absolute Maximum Ratings

The chip cannot be operated under any conditions exceeding this value. If exceeded, it may cause permanent damage to the chip.
And long-term operation at the maximum rating may affect the chip's reliability.

Limit voltage characteristics

Table 4-1 Limit voltage list

symbol	Rating	Minimum	Maximum	unit
VDD	External mains power supply (includedVDDA,VDD,VBAT）	-0.3	6.0	
VIN	FT Input voltage on pin	VSS-0.3	VSS+5.5	
	Any other input voltage on the pin	VSS-0.3	5.5	
	BOOT Input voltage on pin	VSS	5.5	V
|△VSSx|	Variations between different power supply pins	-	50	mV
|△VDDx|	Variations between different ground pins	-	50	mV
VESD(HBM)	Electrostatic Discharge Voltage (Human Body Model)	+25°C 2000V		

Limiting current characteristics

Table 4-2 Limiting current characteristics

symbol	Rating	Maximum	unit
ΣIVDD	Flow into all V DDTotal current of the power line (current source)(1)	200	mA
ΣIVSS	From all V SSThe total current flowing in the ground	-200	

	wire (Sink Current)(1)		
IIO	AnyI/O and control pin output current sink	25	
	AnyI/O and control pin output source current	-25	
IINJ(PIN)	FT,RST andB Injection current on the pin	-5/+0	
	TTaInjection current on the pin	±5	
ΣIINJ(PIN)	Total injected current (all I/Oand control pins)	±25	

Use these
GPIO
Must give VBAT

Extreme temperature characteristics
Storage temperature range (TSTG): -65°C to +150°C
Maximum junction temperature (TJ): 150°C

Working parameters
Recommended working conditions

Table 4-3 Recommended working conditions

symbol	parameter	condition	Minimum	Maximum	unit
fHCLK	internalAHB Clock frequency	-	0	72	MHz
fPCLK1	internalAPB1 Clock frequency	-	0	36	
fPCLK2	internalAPB2 Clock frequency	-	0	72	

VDD	Standard operating voltage	USB Disable	2.2	5.5	V
		USB Enable	3.0	5.5	V
VDDA	Analog operating voltage (exceptADC)	Must be withV DDEquipotential	2.2	5.5	V
	Analog operating voltage（ADC）		2.4	5.5	
VBAT	Backup working voltage	-	2.0	5.5	V

Working conditions during power-on/power-off

Table 4-4 Working conditions during power-on/power-off

symbol	parameter	Minimum	Maximum	unit
tVDD	V DDRise time rate	0	∞	μs/V
	V DDFall time rate	20	∞	

Reset and Power Control Module Characteristics

The parameters given in Table 4-5 are under the ambient temperature and VDD supply voltage conditions summarized in Table 4-3.

Table 4-5 Resulted from the test.

symbol	parameter	Minimum	Maximum	unit
tVDD	VDD rise time rate	0	∞	μs/V
	V DDFall time rate	20	∞	

Reset and Power Control Module Characteristics

The parameters given in Table 4-5 are under the ambient temperature and VDD supply voltage conditions summarized in Table 4-3.

Resulted from the test.

characteristic	symbol	condition	Limit value		unit
		(Unless otherwise specified, VDD=2.2V～5.5V, -55℃≤TA≤125℃)	Minimum	maximum	
POR release voltage	V_r		2	2.1	V
POR reset voltage	V_d		1.8	1.9	V
BOR release voltage	V_{rb}	BOR_LV<2:0>=000	2	2.2	V
		BOR_LV<2:0>=001	2.1	2.3	V
		BOR_LV<2:0>=010	2.2	2.4	V
		BOR_LV<2:0>=011	2.3	2.5	V
		BOR_LV<2:0>=100	2.4	2.6	V
		BOR_LV<2:0>=101	2.5	2.7	V
		BOR_LV<2:0>=110	2.6	2.8	V
		BOR_LV<2:0>=111	2.7	2.9	V
BOR reset voltage	V_{db}	BOR_LV<2:0>=000	1.9	2.1	V
		BOR_LV<2:0>=001	2	2.2	V
		BOR_LV<2:0>=010	2.1	2.3	V
		BOR_LV<2:0>=011	2.2	2.4	V
		BOR_LV<2:0>=100	2.3	2.5	V
		BOR_LV<2:0>=101	2.4	2.6	V
		BOR_LV<2:0>=110	2.5	2.7	V
		BOR_LV<2:0>=111	2.6	2.8	V
PVD release voltage	V_{rp}	PVD_LV<3:0>=0000	2.1	2.3	V
		PVD_LV<3:0>=0001	2.2	2.4	V
PVD release voltage	V_{rp}	PVD_LV<3:0>=0010	2.3	2.5	V
		PVD_LV<3:0>=0011	2.4	2.6	V
		PVD_LV<3:0>=0100	2.5	2.7	V
		PVD_LV<3:0>=0101	2.6	2.8	V
		PVD_LV<3:0>=0110	2.7	2.9	V
		PVD_LV<3:0>=0111	2.8	3	V
		PVD_LV<3:0>=1000	2.9	3.1	V
		PVD_LV<3:0>=1001	3.2	3.4	V
		PVD_LV<3:0>=1010	3.5	3.7	V
		PVD_LV<3:0>=1011	3.8	4	V
		PVD_LV<3:0>=1100	4.1	4.3	V
		PVD_LV<3:0>=1101	4.4	4.6	V
		PVD_LV<3:0>=1110	4.7	4.9	V
		PVD_LV<3:0>=1111	5	5.2	V
PVD power-off voltage	V_{dp}	PVD_LV<3:0>=0000	2	2.2	V
		PVD_LV<3:0>=0001	2.1	2.3	V

		PVD_LV<3:0>=0010	2.2	2.4	V
		PVD_LV<3:0>=0011	2.3	2.5	V
		PVD_LV<3:0>=0100	2.4	2.6	V
		PVD_LV<3:0>=0101	2.5	2.7	V
		PVD_LV<3:0>=0110	2.6	2.8	V
		PVD_LV<3:0>=0111	2.7	2.9	V
		PVD_LV<3:0>=1000	2.8	3	V
		PVD_LV<3:0>=1001	3.1	3.3	V
		PVD_LV<3:0>=1010	3.4	3.6	V
		PVD_LV<3:0>=1011	3.7	3.9	V
		PVD_LV<3:0>=1100	4	4.2	V
		PVD_LV<3:0>=1101	4.3	4.5	V
		PVD_LV<3:0>=1110	4.6	4.8	V
PVD power-off voltage	V_{dp}	PVD_LV<3:0>=1111	4.9	5.1	V

Supply current characteristics

Current consumption is a composite indicator of multiple parameters and factors, derived from comprehensive evaluation and not tested in production.
These parameters and factors include: operating voltage, ambient temperature, GPIO pin loading, product software
configuration, operating frequency, GPIO toggle rate, program location in memory, and the code executed

Table 4-6 Current characteristics in different working modes

characteristic	symbol	condition (Unless otherwise specified,V_{DD}=V_{DDA}=2.2V～5.5V ,-55℃≤T_A≤125℃)	Limit value		unit
			Minimum	maximum	
RUNMode supply current	I_{DD-RUN}	In running mode, the main frequency72MHz ,All peripherals enabled (V_{DD}=5.0V)	-	100	mA

SLEEPMode supply current	$I_{DD-SLEEP}$	SleepmodelThe main frequency is 72MHz , all peripherals stop(V_{DD}=5.0V)	-	50	mA
StopMode supply current	$I_{DD-STOP}$	V_{DD}=5.0V, LSI stops	-	25	mA
Standby mode supply current	$I_{DD-STBY}$	V_{DD} =5.0V, RTC stops, LSEstop	-	1	mA
VBATMode supply current	$I_{DD-VBAT}$	V_{DD}Power off, RTC stopped, LSEstop	-	500	μA

External clock source characteristics

High-speed external user clock generated by an external source

The characteristics given in Table 4-7 are based on the ambient temperature and power supply conditions summarized in Table 4-3 using a high-speed external clock source. Measured under source voltage conditions

Table 4-7 High-speed external user clock characteristics

symbol	parameter	condition	Minimum	Typical Value	Maximum	unit
f_{HSE_ext}	External user clock source frequency (1)	-	1	-8	50	MHz

V_{HSEH}	OSC_INInput pin high level voltage		0.7V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_INInput pin low level voltage		V_{SS}	-	0.3V_{DD}	
$t_{w(HSE)}t_{f(HSE)}$	OSC_IN High or low time (1)		5	-	-	ns
$t_{r(HSE)}t_{f(HSE)}$	OSC_INRise or fall time (1)		-	-	20	
$C_{in(HSE)}$	OSC_INInput Capacitance (1)	-	-	5	-	pF
DuCy (HSE)	Duty Cycle	-	45	-	55	%
I_L	OSC_INInput leakage current	$V_{SS}≤V_{IN}≤V_{DD}$	-	-	±1	μA

Guaranteed by design, not tested in production.
Low-speed external user clock generated by an external source
The characteristics given in Table 4-8 are based on the low speed external clock source at the ambient temperature and
Measured at power supply voltage.

Table 4-8 Low-speed external user clock characteristics

symbol	parameter	condition	Minimum	Typical Value	Maximum	unit
f_{LSE_ext}	User external clock source frequency (1)	-		32.768	1000	kHz
V_{LSEH}	OSC_INInput pin high level voltage		0.7V_{DD}	-	V_{DD}	V
V_{LSEL}	OSC_INInput pin low level voltage		V_{SS}	-	0.3V_{DD}	
$t_{w(LSE)}t_{f(LSE)}$	OSC_IN High or low time (1)		450	-	-	ns
$t_{r(LSE)}t_{f(LSE)}$	OSC_INRise or fall time (1)		-	-	50	
$C_{in(LSE)}$	OSC_INInput Capacitance (1)	-	-	5		pF
DuCy (LSE)	Duty Cycle	-	30	-	70	%
I_L	OSC_INInput leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

Guaranteed by design, not tested in production

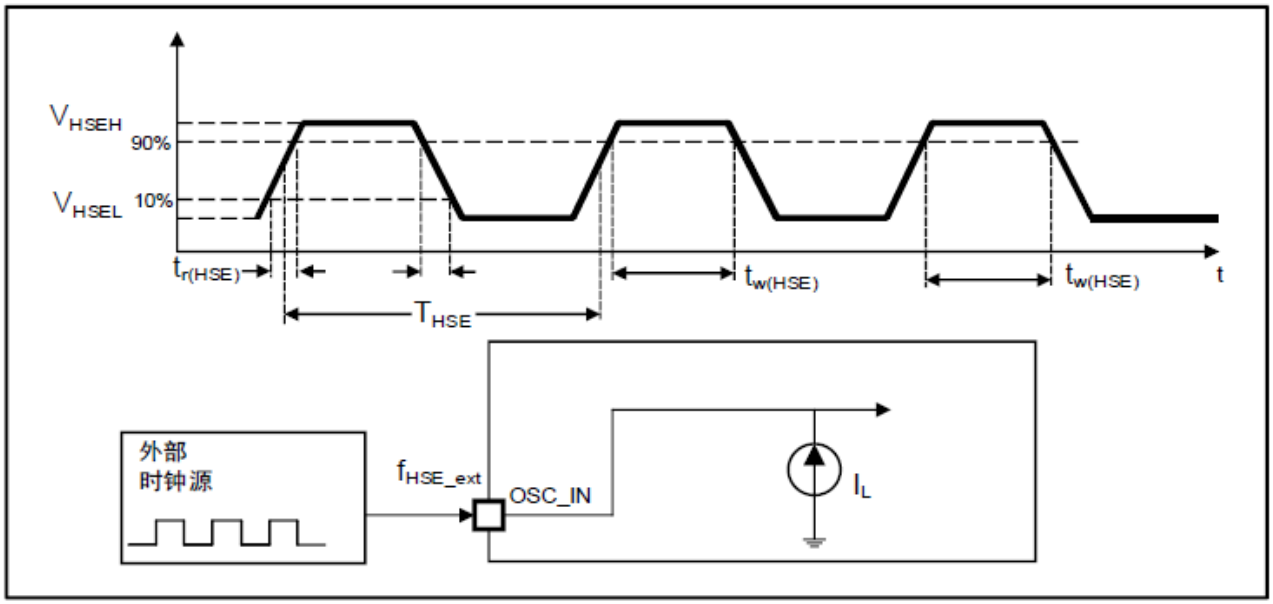


Figure 4-1 High-speed external clock source AC timing diagram

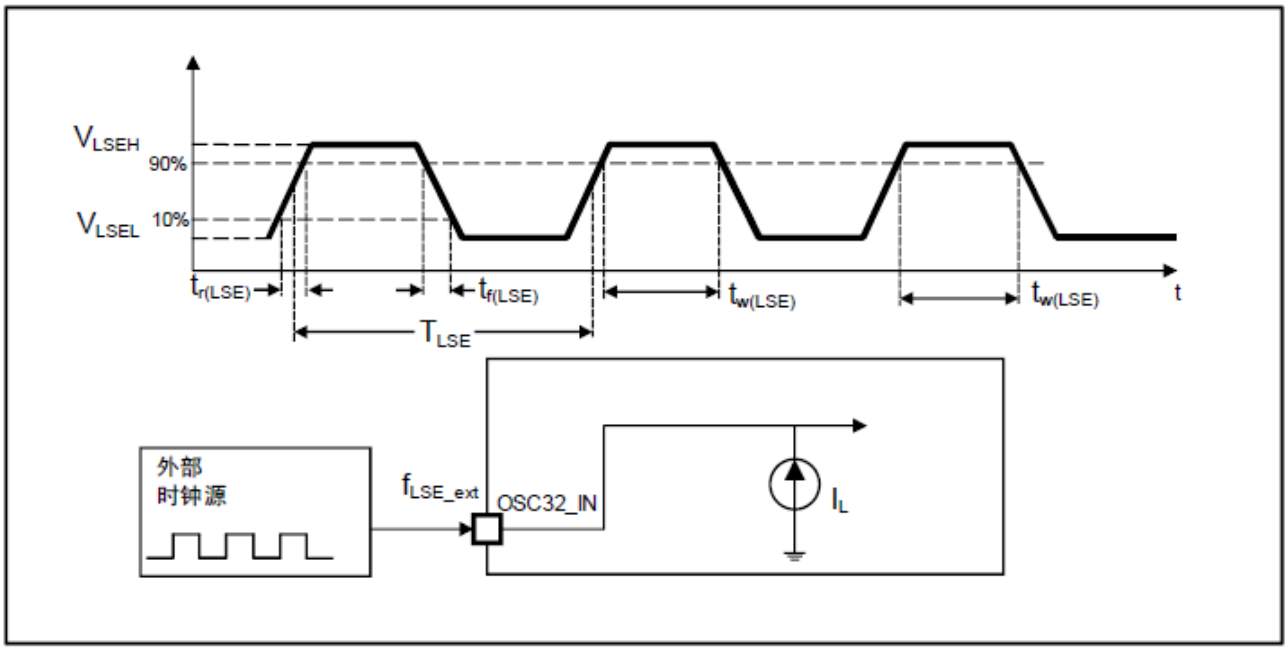


Figure 4-2 Low-speed external clock source AC timing diagram

High-speed external clock generated by crystal/ceramic oscillator
The high-speed external (HSE) clock can be generated using a 4 to 16 MHz crystal/ceramic resonator oscillator.
The information presented in this section is determined through characterization results using the
In the application, the resonator and load capacitors must be as close as possible.
oscillator pins to minimize output distortion and oscillation stabilization time

Table 4-9 HSE oscillator characteristics (1) (2)

symbol	parameter	condition	Minimum	Typical Value	Maximum	unit
f_{OSC_IN}	Oscillator frequency	-	4		16	MHz
R_F	Feedback Register	-	-	200	-	kΩ
C	The recommended load capacitance and the equivalent series connection of the crystalParallel resistance (R_S) (3)	R_S= 30Ω	-	30	-	pF
i_2	HSE Drive current	V_{DD} =3.3V,V_{IN}=V_{SS} and30pF Load	-	-	1	mA
$t_{SU(HSE)}$(4)	Startup time	V_{DD}Stablize	-	2	-	ms

The resonat/orcharacteristics given by the crystal ceramic resonator manufacturer.
Based on characterization, not tested in production
RF
The relatively low value of the register provides good protection against problems caused by leakage or changes in bias conditions in humid environments
tSU(HSE)The start-up time is from software enableHSE Start measuring until a stable 8MHz
For CL1 and CL2, it is recommended to use a crystal or resonator designed for high frequency applications.
A high-quality external ceramic capacitor between 5 pF and 25 pF (typical) is required (see

Figure 4-3). CL1 and CL2 are usually the same size. The crystal manufacturer usually specifies the load capacitors.
It is a series combination of CL1 and CL2. When determining the specifications of CL1 and CL2, the PCB and
The capacitance of the MCU pins is taken into account (the capacitance of the pin to the board can be roughly estimated to be 10 pF).

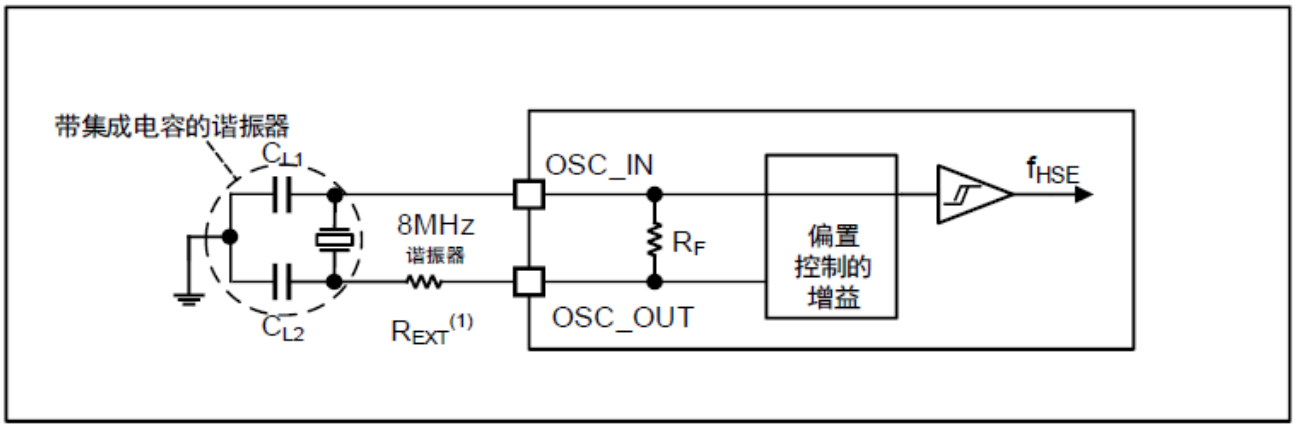


Figure 4-3 Typical application using 8MHz crystal oscillator

Low speed external clock generated by crystal/ceramic oscillator
The low speed external (LSE) clock can be composed of a 32.768 kHz crystal/ceramic resonator. The information presented in this section is determined by the results of characterization. In applications, the resonator
The load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and start-up stability.
For detailed information on resonator characteristics (frequency, packaging, accuracy, etc.), please consult the crystal oscillator Resonator Manufacturer.

Table 4-10 LSE oscillator characteristics (fLSE = 32.768kHz) (1)

symbol	parameter	condition	Minimum	Typical Value	Maximum	unit
R_F	Feedback resistor	-	-	5	-	MΩ
$C_{(2)}$	Recommended load capacitance and crystal equivalent series resistanceResistance (Rs）(3)	R_S= 30kΩ	-	-	15	pF

I_2	LSEDrive current	V_{DD}= 3.3V,V_{IN}=V_{SS}		-	-	1.4	μA
$t_{SU(LSE)(4)}$	Startup time	V_{DD}Stablize	T_A=50℃	-	1.5	-	s
			T_A=25℃	-	2.5	-	
			T_A=10℃	-	4	-	
			T_A=0℃	-	6	-	
			T_A=-10℃	-	10	-	
			T_A=-20℃	-	17	-	
			T_A=-30℃	-	32	-	
			T_A=-40℃	-	60	-	

1. Based on characterization, not production tested.
2. Refer to the notes paragraph in the table below and the application note AN2867 “ST Microcontroller Oscillation Design Guide”
3. The choice of oscillator can be optimized using a high quality resonator with a small RS value (such as MSIV-TIN32.768KHz)
4. tSU(LSE) is the start-up time measured from the moment it is enabled (by software) to a stable 32.768KHz oscillation.

This value is measured for a standard crystal and can vary significantly from manufacturer to manufacturer. Note: For CL1 and CL2, it is recommended to use a crystal or resonator designed for high frequency applications and sized between 5 p and 25 p. pF (typical) high-quality external ceramic capacitors (see
). CL1 and CL2 are usually the same size. The crystal manufacturer specifies that the load capacitors are CL1 and CL2.
Combination. The load capacitance CL has the following formula: CL = CL1 × CL2 / (CL1 + CL2) + Cstray, where Cstray is the pin capacitance and the capacitance associated with the board or trace pcb, which is between 2pF and 7pF.
Warning: To avoid exceeding the maximum value of CL1 and CL2 (15pF), it is strongly recommended to use a resonator with a load capacitance of CL ≤ 7pF, and do not use a resonator with a load capacitance of 12.5pF.
Example: If a resonator with a load capacitance of CL = 6pF and Cstray = 2pF is selected, then CL1 = CL2 = 8pF

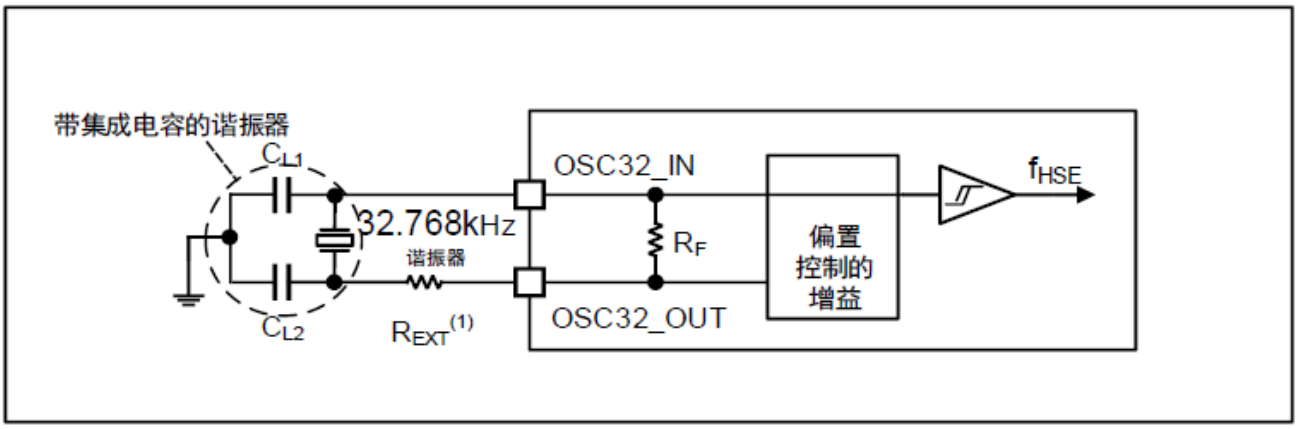


Figure 4-4 Typical application of 32.768kHz crystal oscillator

Internal Clock Characteristics

The parameters given in Table 4-11 are obtained under the ambient temperature and VDD supply voltage conditions summarized in Table 4-3.

High Speed Internal (HS) RC Oscillator

Table 4-11 HIS Oscillator Characteristics(1)

symbol	parameter	condition	Minimum	Typical Value	Maximum	unit
f_{HSI}	frequency	-	7.5	8	8.5	MHz
	HSIUser Adjustable Scale(2)	-		1(3)		%
	HSI Oscillator Accuracy	T_A=125℃	-2	-	2	%
		T_A=25℃	-1		2	%
		T_A=-55℃	-2		2	%
$t_{su(HSI)}$(2)	HSI Oscillator stabilization time	-		4		μs

1. Unless otherwise specified, VDD=3.3V, TA=-40 to 105℃.
2. Guaranteed by design, not tested in production.
3. Guaranteed by characterization results, not tested in production.

Table 4-12 LSI Oscillator Characteristics (1)

symbol	parameter	Minimum	Typical Value	Maximum	unit
f_{LSI} (2)	frequency	30	40	60	kHz
$t_{su(LSI)}$ (3)	LSI Oscillator start-up time	-	-	85	µs
$I_{DD(LSI)}$ (3)	LSIOscillator Power Consumption	-	0.65	1.2	µA

Unless otherwise specified, VDD = 3.3V, TA = -40 to 105°C.
2. Guaranteed by characterization results, not tested in production.
3. Guaranteed by design, not tested in production.

The wake-up times given in Table 4-13 are measured during the wake-up phase using an 8MHz HSI RC oscillator. The clock source used to wake up the device depends on the current operating mode:
 Stop or Standby mode: The clock source is the RC oscillator.
 Sleep mode: The clock source is set upon entry.

All times are from tests performed at ambient temperature and VDD voltage conditions summarized in Table 4-3.

Table 4-13 Low-Power Mode Wake-up Times

symbol	parameter	Typical Value	unit
$t_{WUSLEEP}$ (1)	Wake up from sleep mode	1.8	µs
t_{WUSTOP} (1)	Wake-up from Stop Mode (Regulator in Run Mode)	3.6	µs
	Stop mode wakeup (regulator in low power mode)	5.4	

$t_{WUSTDBY}$ (1)	Wake up from standby mode	50	µs

1. Wake-up time is measured from event to first instruction read by user application.

4.2.7 PLL Characteristics

The parameters given in Table 4-14 are tested under the temperature and VDD supply voltage conditions summarized in Table 4-7.

Table 4-14 PLL Characteristics

symbol	parameter	Minimum(1)	Typical Value	Maximum(1)	unit
f_{PLL_IN}	PLLInput Clock(2)	1	8.0	25	MHz
	PLLInput clock duty cycle	40	-	60	ns
f_{PLL_OUT}	PLLMultiplied output clock	16	-	72	MHz
t_{LOCK}	PLLPhase lock time	-		350	µs
Jitter	Periodic Jitter	-		300	ps

1. Determined by characterization, not tested in production
2. Be careful to use the appropriate multiplication factor so that the PLL input clock is compatible with the range defined by fPLL_OUT.

Memory (FLASH) Characteristics

Flash Memory

Table 4-15 Flash Memory Characteristics

symbol	parameter	VDD=1.35~1.65V		Unit
		Minimum	Maximum	
TPROG	Byte Programming Time	6	7,5	µs
TERASE	Sector erase time	4	5	ms
	Full chip erase time	30	40	ms

Table 4-16 Flash memory tolerance and data storage tolerance and data storage tolerance and data storage tolerance

symbol	parameter	Minimum specifications	unit
$N_{(1)END}$	Tolerance	100000	cycles
$T_{DR(2)}$	Data storage	20	Years

1. Durability test conditions: room temperature, 1.5V VDD.
2. Data storage: 20 years@25℃.

Electrical sensitivity EMC

Test the ESD and LU of sampled products using specific measurement methods.
Electrostatic discharge (ESD)
Based on

Table 4-17 ESD Absolute Maximum Ratings Absolute Maximum Ratings

symbol	Rating	condition	Classification	Maximum(1)	unit
$V_{ESD(HBM)}$	Electrostatic dischargePressure Human Modeltype)	TA = +25°C ,conform to ANSI/ESDA/JEDEC JS-001-2012standard	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage(Charging equipmentModel)	TA = +25 °C,conform to ANSI/ESD S5.3.1-2009Standard, package LQFP208	3	250	

		TA = +25 °C, Compliant with ANSI/ESD S5.3.1-2009Standard, package LQFP208	4	500	

Electrostatic Latch-up

To evaluate latch-up performance, two complementary static tests are performed on the six devices:

 Overvoltage applied to each power pin.

 Current injection applied to each input, output, and configurable GPIO pin.

These tests comply with the EIA/JESD 78A IC latch-up standard.

Table 4-18 Electrical Sensitivity Electrical

Symbolic parameters	parameter	condition	Classification
LU	Static blocking classification	TA=+125°C, per JESD78A	Class II Category A

I/O Current Injection Characteristics

Normally, current injection into I/O pins due to external voltage below VSS or above VDD (3V I/O pins as standard) should be avoided during product operation. However, to illustrate the robustness of the microcontroller when an abnormal injection occurs unexpectedly, a sensitivity test is performed on the samples during the device specific assessment.

Functional sensitivity of I/O current

A simple application is executed on the device while current is injected into the I/O pins set to floating input mode to stress the device. While injecting current into each I/O pin, check the A fault is indicated if the following parameters are out of range: ADC error exceeds a certain limit (>5 LSB TUE), induced leakage current on adjacent pins exceeds normal limits, or other functional faults occur (e.g., reset, oscillator frequency offset).

The test results are shown in Table 4-19.

Table 4-19 I/O Current Injection Sensitivity Current Injection Sensitivity Current Injection Sensitivity (1)

symbol	illustrate	Functional sensitivity		unit
		Injecting negative current	Inject positive current	
I_{INJ}	OSC_IN32, OSC_OUT32, PA4, PA5, PC13 Injection current on the pin	-0	0	mA
	allFT Injection current on the pin	-5	0	
	Any other pin injection current	-5	5	

I/O Port Characteristics

General Input/Output Characteristics

All I/Os are compatible with CMOS and TTL

Table 4-20 GPIO static characteristics

characteristic	symbol	condition (Unless otherwise specified,V_{DD}=2.2V～5.5V ,-55℃≤T_A≤125℃)	Limit value		unit
			Minimum	maximum	
I/OInput low level voltage	V_{IL}	removePA10,PA12External pins	-	0.3*V_{DD}	V
I/OInput high level voltage	V_{IH}	removePA10,PA12External pins	0.7*V_{DD}	-	V

		V_{DD}=5.5V,V_{IN}=V_{DD}orV_{SS} ,removePA10,PA12External pins	-	±3	μA
		V_{DD}=3.3V,V_{IN} =5.5V, exceptPA10,PA12External pins	-	±5	μA
		V_{DD}=5.5V,V_{IN}=V_{DD}orV_{SS} ,PA10,PA12Pinout	-	±3	uA
I/OInput leakage current	I_{LKG}				
		V_{DD}=5.5V ,I_{IO}=20mA,all IOPinout	-	1.4	V
		V_{DD}=3.3V ,I_{IO}=8mA,all IOPinout	-	0.3*V_{DD}	V
		V_{DD}=2.2V ,I_{IO}=6mA,all IOPinout	-	0.8	V
I/OOutput low level voltage	V_{OL}				
		V_{DD} =5.5V,I_{IO} =20mA, exceptPC14,PC15,OSC_IN ,OSC_OUTExternal pins	0.7*V_{DD}	-	V
		V_{DD}=5.5V ,I_{IO}=4mA, PC14 ,PC15,OSC_IN, OSC_OUTPinout	0.7*V_{DD}	-	V
		V_{DD}=3.3V ,I_{IO}=8mA,removePC14 ,PC15,OSC_IN, OSC_OUTExternal pins	0.7*V_{DD}	-	V
I/OOutput high level voltage	V_{OH}				

		V_{DD}=3.3V ,I_{IO}=1mA, PC14 ,PC15,OSC_IN, OSC_OUTPinout	0.7*V_{DD}	-	V
		V_{DD}=2.2V ,I_{IO}=1mA, PC14 ,PC15,OSC_IN, OSC_OUTPinout	0.7*V_{DD}	-	V
Input pull-up current	|I_{PU}|	V_{DD}=3.3V, exceptP A10, PA12 and otherPinout	60	110	uA
		V_{DD}=3.3V, PA10,PA12 pins	0	2	uA
Input pull-down current	|I_{PD}|	V_{DD}=3.3V, exceptP A10, PA12 and otherPinout	60	110	uA
Pull-up resistor	R_{PU}	V_{IN}=V_{SS}	30	50	kΩ
Pull-down resistor	R_{PD}	V_{IN}=V_{DD}	30	50	kΩ

Output Drive Current Output Drive Current Output Drive Current Output Drive Current Output Drive Current Output Drive Current
GPIO (General Purpose Input/Output) can provide a maximum of ±8mA source or sink current, and (under relaxed VOL/VOH conditions) can source or sink up to ±20 mA.
In user applications, the number of I/O pins that can drive current must be limited, especially:
 The total source current drawn by all I/Os from VDD, plus the total source current drawn by the MCU, plus the maximum operating source current drawn by the MCU from VDD, must not exceed the absolute maximum rating of IVDD (see Table 4-2).
 The total source current drawn by all I/Os from VSS, plus the total source current drawn by the MCU, plus the maximum operating source current drawn by the MCU from VSS, must not exceed the absolute maximum rating of ΣIVSS (see Table 4-2).
Input/Output AC Characteristics
The definitions and values of the Input/Output AC Characteristics are given in The definitions and values of the characteristics are given in Table 4-21.
Unless otherwise specified, the parameters given in Table 4-21 are tested under the ambient temperature and VDD supply voltage conditions summarized in Table 4-3.

Table 4-21 I/O AC Characteristics (1)

symbol	parameter	condition	Minimum	Typical Value	Maximum	unit
tEXTIpw	EXTIThe pulse width of the external signal detected by the controller	-	100	-	-	ns

1. Guaranteed by design, not production tested.

NRST Pin Characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor RPU (see Table 4-25 NRST Pin Characteristics).
Unless otherwise specified, the parameters given in Table 4-22 are tested under the ambient temperature and VDD supply voltage conditions summarized in Table 4-3.

Table 4-22 NRST Pin Characteristics

symbol	parameter		condition	Minimum	Typical Value	Maximum	unit
$V_{IL(NRST)(1)}$	NRST	Input low voltage	-	–0.5	-	0.8	V
$V_{IH(NRST)(1)}$	NRST	Input high voltage	-	2	-	V_{DD}+0.5	
symbol	**parameter**		**condition**	**Minimum**	**Typical Value**	**Maximum**	**unit**
$V_{hys(NRST)}$	NRST Schmitt trigger hysteresis voltage		-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistance(2)		$V_{IN}= V_{SS}$	30	40	50	kΩ
$V_{F(NRST)(1)}$	NRST Input filter pulse		-	-	-	100	ns
$V_{NF(NRST)(1)}$	NRST Input unfiltered pulse		V_{DD}> 2.7 V	300	-	-	ns

1. Guaranteed by design, not tested in production
2. The pull-up resistor is designed as a real resistor in series with a switchable PMOS. The PMOS has a minimal effect on the series resistance (about 10%).

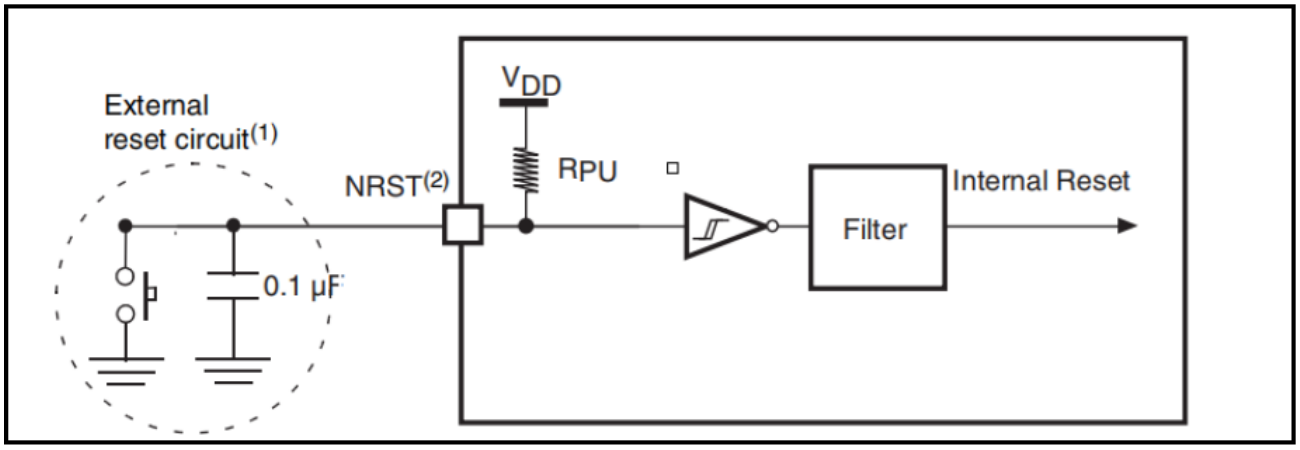


Figure 4-5 Recommended NRST pin protection

1. This reset network protects the device from reset.
2. The user must ensure that the voltage level on the NRST pin can drop below the maximum level of VIL(NRST) specified in Table 4-22. Otherwise, the device will not perform a reset.

TIM counter characteristics

The parameters in Table 4-23 are guaranteed by design.

For details on the input/output multiplexing function characteristics (compare, input capture, external clock, external clock PWM output), see 4.2.111 I/O port characteristics.

Table 4-23 TIMx(1) characteristics

symbol	parameter	condition(3)	Minimum	Maximum	unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ =72MHz	13.9	-	ns
f_{EXT}	CH1 arrive CH4The external clock frequency of the timer on	-	0	$f_{TTIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ =72MHz	0	36	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	When the internal clock is selected, the counter clock period is16 Bit	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ =72MHz	0.0139	910	µs

t_{MAX_COUNT}	The maximum possible count of the counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=72MHz	-	59.6	s

1. TIMx is a general term for TIM1, TIM2, TIM3, TIM4, TIM5 timers.

Communication Interface

I2C Interface Characteristics Interface Characteristics Interface Characteristics Interface Characteristics

Unless otherwise specified, the parameters given in Table 4-24 are tested under the ambient temperature, fPCLK1 frequency and VDD supply voltage conditions summarized in Table 4-3.

The I2C interface in the BST32F1 series complies with the requirements of the standard I2C communication protocol, but has the following limitations: The I/O pins mapped by SDA and SCL are not "real" open-drain pins. When configured as open-drain pins, the PMOS connected between the I/O pin and VDD will be disabled, but still exists.

The I2C characteristics are listed in Table 4-24. For details on the input/output multiplexing function characteristics (SDA and SCL), see 4.2.111 I/O Port Characteristics.

Table 4-24 I2C Features

symbol	**parameter**	**Standard Mode I2C(1)**		**Fast Mode I2C(1)(2)**	**unit**
		Minimum	Maximum	Minimum	
$t_{w(SCLL)}$	SCL Clock low time	4.7	-	1.3	μs
$t_{w(SCLH)}$	SCL Clock high time	4.0	-	0.6	
$t_{su(SDA)}$	SDA Build Time	250	-	100	ns
$t_{h(SDA)}$	SDA Data retention time	0(3)	-	0(4)	
$t_{r(SDA)}t_{r(SCL)}$	SDA andSCL Rise time	-	1000	20 + 0.1C_b	
$t_{f(SDA)}t_{f(SCL)}$	SDA andSCL Fall time	-	300	- 300	

$t_{h(STA)}$	Start condition hold time	4.0	-	0.6 -	μs
$t_{su(STA)}$	Repeated start condition setup time	4.7	-	0.6 -	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6 -	μs
$t_{w(STO:STA)}$	Stop to start time (bus idle)	4.7	-	1.3 -	μs
C_b	Capacitive load per bus	-	400	- 400	pF

1. Guaranteed by design, not production tested.
2. fPCLK1 must be at least 2 MHz to achieve the standard mode I2C frequency. It must be at least 4 MHz to achieve the fast mode I2C frequency, must be an integer multiple of 10 MHz to achieve the maximum I2C fast mode clock of 400 kHz.
3. If the SCL signal is not required to be stretched low, the maximum hold time of the start condition only needs to be met.
4. The device must provide a hold time of at least 300 ns for the SDA signal to cross the unknown falling edge of SCL.

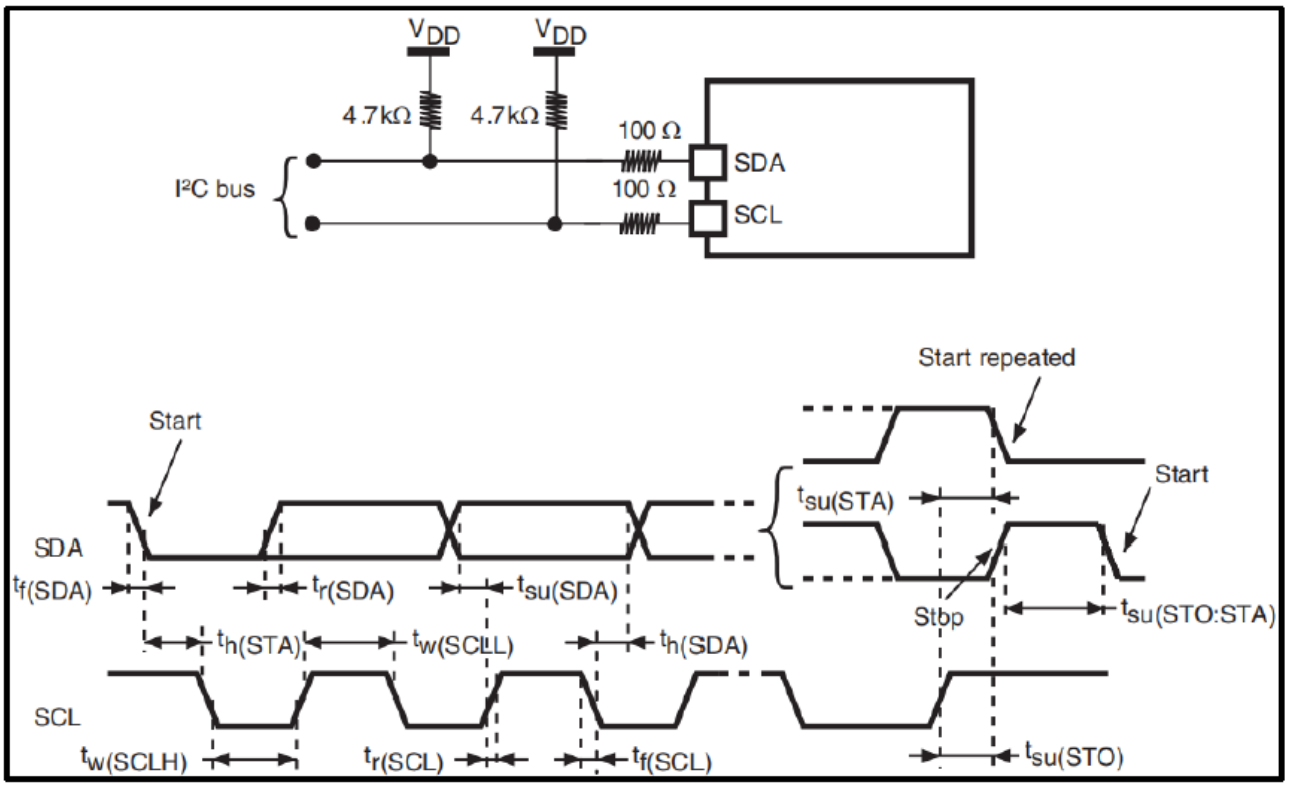


Figure 4-6 I2C bus AC waveform and measurement circuit

1. Measurement points are based on CMOS levels: 0.3VDD and 0.7VDD.

Table 4-25 SCL frequency (fPCLK1 = 36 MHz, VDD = VDD_I2C = 3.3 V) (1) (2)

f_{SCL} (kHz)	**I2C_CCR Value** **R_P = 4.7 kΩ**
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. RP = external pull-up resistor, fSCL = I2C speed.
2. The achieved speed tolerance is ±5% for speeds around 200 kHz. For other speed ranges, the achieved speed tolerance is ±2%. These variations depend on the accuracy of external components used in the design of the application.

I2S - SPI Interface Characteristics

Unless otherwise stated, the SPI parameters in Table 4-26 and the I2S parameters in Table 4-27 are tested under the ambient temperature, fPCLKX frequency and VDD voltage conditions summarized in Table 4-3.

For details on the input/output multiplexing function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I2S), see 4.2.10 I/O Current Injection Characteristics.

Table 4-26 SPI Characteristics

symbol	parameter	condition	Minimum	Maximum	unit
f_{SCK} $1/t_{c(SCK)}$	SPI Clock frequency	Main Mode	-	18	MHz
		Slave Mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI The timing of the rising and falling edges of the clock	Capacitive load: C = 30 pF	-	8	ns
DuCy(SCK)	SPI The duty cycle of the input clock	Slave Mode	30	70	%
$t_{su(NSS)}$	NSS Build Time	Slave Mode	4 t_{PCLK}	-	ns
$t_{h(NSS)}$	NSS Keep time	Slave Mode	2 t_{PCLK}	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCKHigh and low time	Main Mode, f_{PCLK}= 36 MHz, PreFrequency division= 4	50	60	
$t_{su(MI)}$	Data input setup time	Main Mode	4	-	
$t_{su(SI)}$		Slave Mode	5	-	
$t_{h(MI)}$	Data input hold time	Main Mode	5	-	
$t_{h(SI)}$		Slave Mode	5	-	

$t_{a(SO)}$	Data output access time	Slave Mode, f_{PCLK}= 20 MHz	-	3*t_{PCLK}	
$t_{v(SO)}$	Data output valid time	Slave Mode(EnableAfter edge)	-	34	
$t_{v(MO)}$	Data output valid time	Main Mode(EnableAfter edge)	-	8	
$t_{h(SO)}$	Data output hold time	Slave Mode(EnableAfter edge)	32	-	
$t_{h(MO)}$		Main Mode(EnableAfter edge)	10	-	

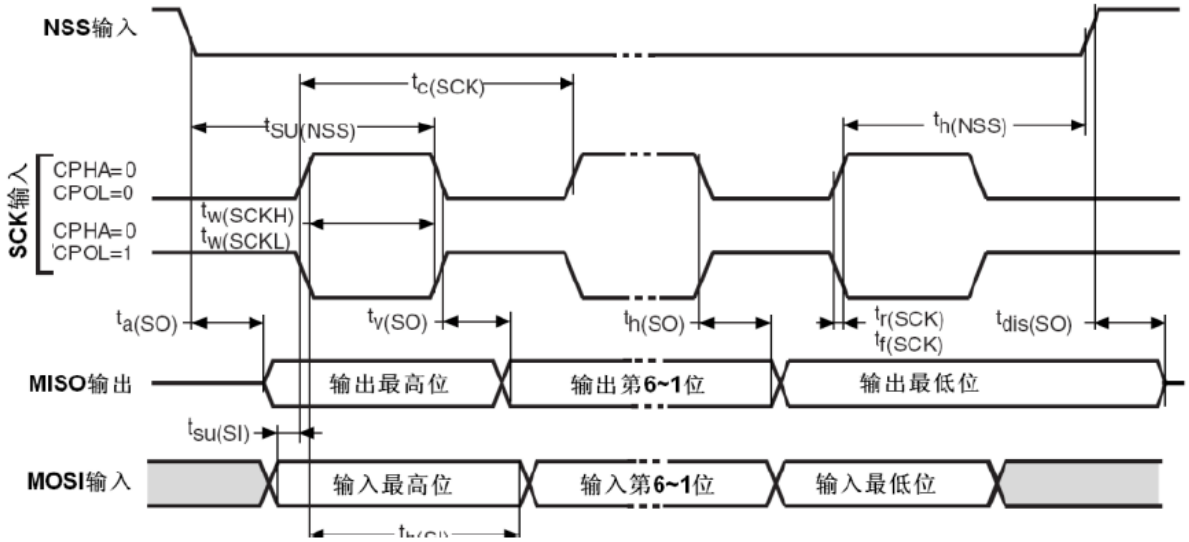


Figure 4-7 SPI Timing Diagram - Slave Mode, Slave Mode, Slave Mode, CPHA=0

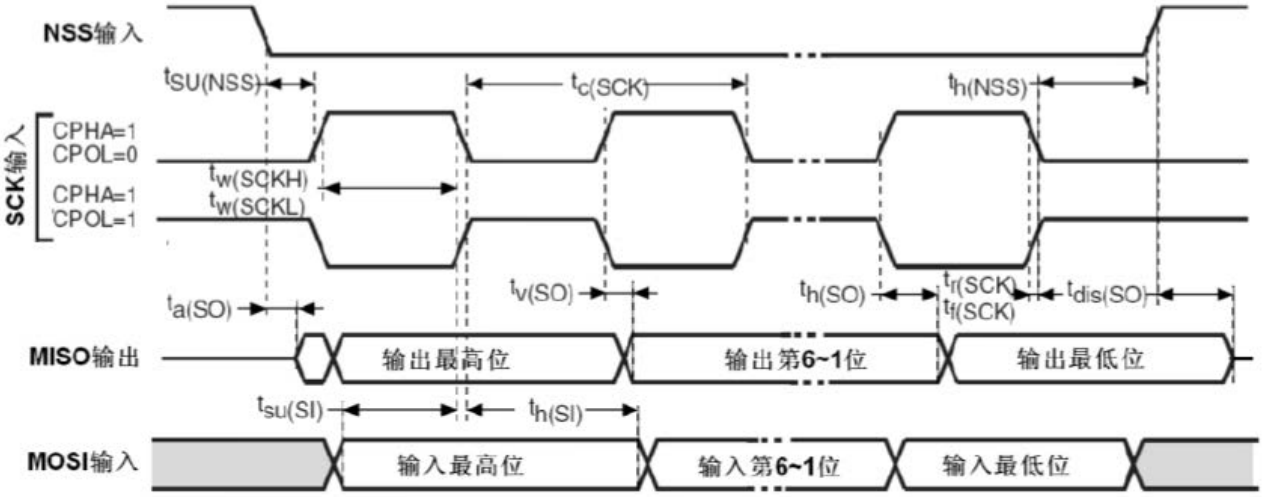


Figure 4-8 SPI Timing Diagram - Slave Mode, Slave Mode, Slave Mode, CPHA=1(1)

1. Measurement points based on CMOS levels: 0.3VDD and 0.7VDD

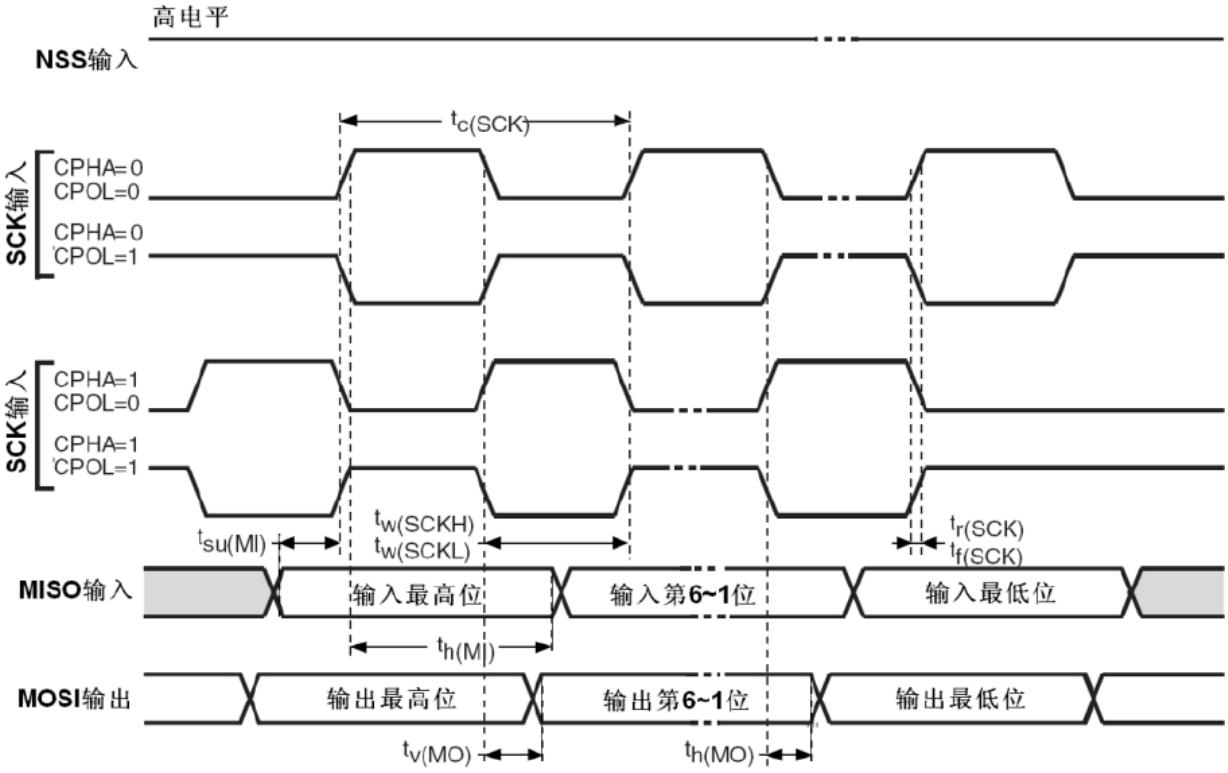
4-9 SPI Timing Diagram Timing Diagram - Master Mode Master Mode (1)

1. Measurement points based on CMOS levels: 0.3VDD and 0.7VDD

Table 4-27 I2S Features 4-9 SPI Timing Diagram Timing Diagram - Master Mode Master Mode (1)

1. Measurement points based on CMOS levels: 0.3VDD and 0.7VDD

Table 4-27 I2S Features



SPI Timing Diagram Timing Diagram - Master Mode Master Mode (1)

1. Measurement points based on CMOS levels: 0.3VDD and 0.7VDD

Table 4-27 I2S Features

symbol	parameter	condition		Minimum	Maximum	unit
f_{CK} 1/$t_{c(CK)}$	I2S Clock frequency	Master Data : 16Bit ,Audio frequency = 48K		1.52	1.54	MHz
		from		0	6.5	
$t_{r(CK)}$ $t_{f(CK)}$	I2S Clock rising and falling edge time	Capacitive load C_L = 50 pF		-	8	ns
$t_{w(CKH)(1)}$	I2S Clock high time	hostf $_{PCLK}$ = 16 MHz,Audio frequency = 48 K		317	320	
$t_{w(CKL)(1)}$	I2S Clock low time			333	336	
$t_{v(WS)}$ (1)	WS Validity period	Main Mode		3	-	
$t_{h(WS)}$ (1)	WS Keep time	Main Mode	I2S2	0	-	
			I2S3	0	-	
$t_{su(WS)}$ (1)	WS Build Time	Slave Mode	I2S2	4	-	
			I2S3	9	-	
$t_{h(WS)}$ (1)	WS Keep time	Slave Mode		0	-	
DuCy(SCK)	I2S is the duty cycle of the input clock	Slave Mode		30	70	%
$t_{su(SD\_MR)(1)}$	Data input setup time	Main Receiver	I2S2	8	-	ns
			I2S3	10	-	
$t_{su(SD\_SR)(1)}$		From the receiver	I2S2	3	-	
			I2S3	8	-	
$t_{h(SD\_MR)(1)}$	Data input hold time	Main Receiver	I2S2	2	-	
			I2S3	4	-	
$t_{h(SD\_SR)(1)}$			I2S2	2	-	

		From the receiver	I2S3	4	-	
$t_{v(SD\_ST)(1)(3)}$	Data output valid time	From the transmitter(After enabling edge)	I2S2	23	-	
			I2S3	33	-	
$t_{h(SD\_ST)(1)}$	Data output hold time	From the transmitter(After enabling edge)	I2S2	29	-	
			I2S3	27	-	
$t_{v(SD\_MT)(1)}$	Data output valid time	Master Transmitter(After enabling edge)	I2S2	-	5	
			I2S3	-	2	
$t_{h(SD\_MT)(1)}$	Data output hold time	Master Transmitter(After enabling edge)	I2S2	11	-	
			I2S3	4	-	

Based on design characterization results, not production tested

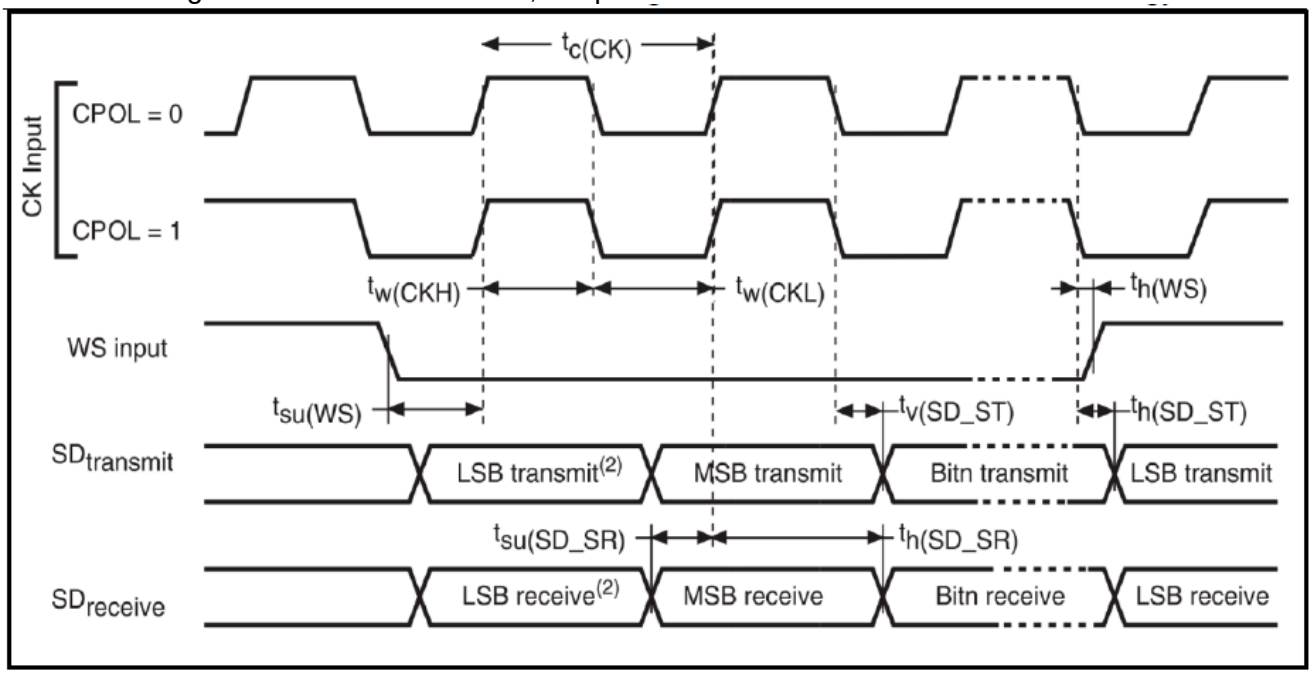


Figure 4-10 I2S Slave Mode Timing Diagram (Philips Protocol) (1)

1. Measurement points based on CMOS levels: 0.3VDD and 0.7VDD.
2. LSB of the previous transmitted byte is transmitted/received. No LSB is transmitted/received before the first byte.

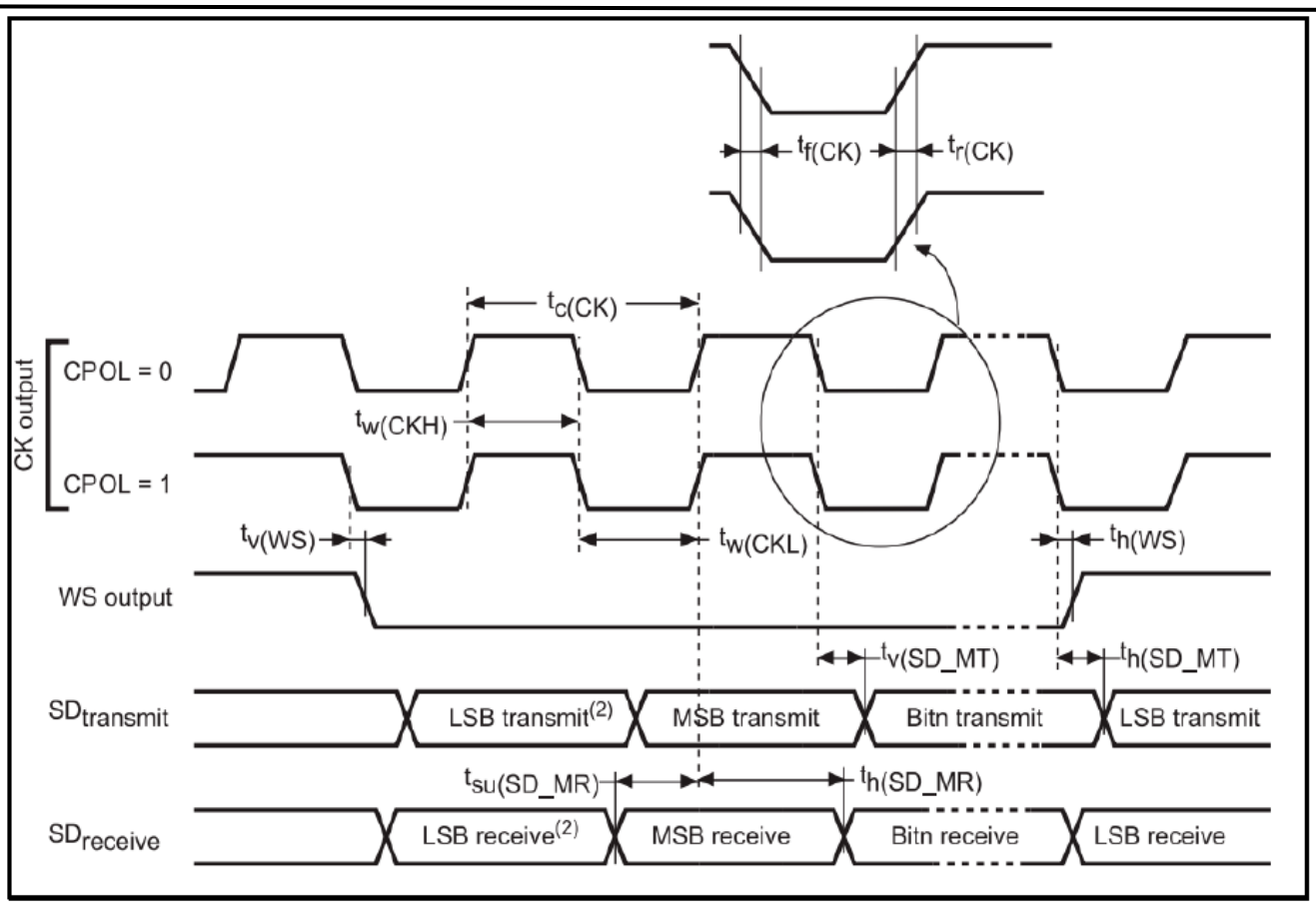


Figure 4-11 I2S Master Mode Timing Diagram (Philips Protocol) (1)

1. Based on design/characteristic analysis results, not tested in production.
2. LSB of the previous transmitted byte is transmitted/received. No LSB is transmitted/received before the first byte.

USB OTG Full Speed (FS) Features

The USB OTG interface is certified by USB-IF (Full Speed).

Table 4-28 USB OTG FS Startup Time

symbol	parameter	Maximum	unit
$t_{STARTU(1)P}$	USB OTG FS transceiver startup time	1	μs

1. Guaranteed by design, not tested in production.

Table 4-29 USB OTG FS DC electrical characteristics DC electrical characteristics DC

symbol		parameter	condition	Minimum(1)	Typical Value	Maximum(1)	unit
Input Level	V_{DD}	USB OTG full speed transceiver operating voltage	-	3.0(2)	-	3.6	V
	V_{DI} (3)	Differential Input Sensitivity	I(USBDP, USBDM)	0.2	-	-	V
	V_{CM} (3)	Differential common mode range	IncludeV_{DI}scope	0.8	-	2.5	
	V_{SE} (3)	Single-ended receiver threshold	-	1.3	-	2.0	
Output Level	V_{OL}	Static output low level	1.5 kΩof RLConnect to 3.6 V(4)		-	0.3	V
	V_{OH}	Static output high level	15 kΩof RLConnect to V_{SS} (4)	2.8	-	3.6	
R_{PD}		PA11, PA12 Up and DownPull-up resistor	V_{IN}= V_{DD}	17	21	24	kΩ
		PA9 Pull-down resistor		0.65	1.1	2.0	
R_{PU}		PA12 Pull-up resistor	V_{IN}= V_{SS}	1.5	1.8	2.1	

	PA9 Pull-up resistor	V_{IN}= V_{SS}	0.25	0.37	0.55	

1. All voltages are measured based on local grounding.
2. The BST32F1 series still guarantees USB OTG full-speed transceiver functionality when the operating voltage drops to 2.7V, but does not guarantee full USB OTG full-speed electrical characteristics, which are degraded within the VDD voltage range of 2.7V to 3.0V.
3. Guaranteed by design, not production tested.
4. RL is connected to the USB OTG full-speed

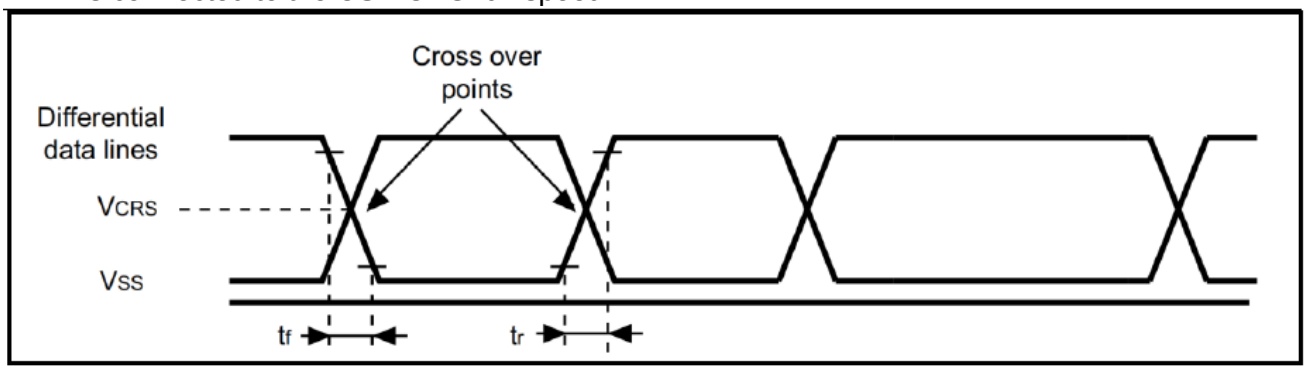


Figure 4-12 USB OTG full-speed timing: Definition of the rise and fall time of the data signal Full-speed timing: Definition of the rise and fall time of the data signal Full-speed timing: Definition of the rise and fall time of the data signal Full-speed timing: Definition of the rise and fall time of the data signal Full-speed timing: Definition of the rise and fall time of the data signal Full-speed timing: Definition of the rise and fall time of the data signal Full-speed timing: Definition of the rise and fall time of the data signal

Table 4-30 USB OTG full-speed electrical characteristics Full-speed electrical characteristics (1)

Driver characteristics					
symbol	parameter	condition	Minimum	Maximum	unit
t_r	Rise time(2)	C_L= 50 pF	4	20	ns
t_f	Fall time(2)	C_L= 50 pF	4	20	ns
t_{rfm}	rise/Fall Time Matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design, not production tested.
2. Measured within 10% to 90% of the data signal range, please refer to the USB Specification -

Chapter 7 (Version 2.0) for more details.

Ethernet Characteristics

Table 4-31 gives the Ethernet operating voltage

Table 4-31 Ethernet DC Characteristics

symbol		parameter	Minimum (1)	Maximum (1)	unit
Input Level	V_{DD}	Ethernet operating voltage	3.0	3.6	V

1. All voltages are measured at local grounding.

Table 4-32 shows the Ethernet MAC signal list for the SMI (station management interface), and Figure 4-13 shows the Ethernet MAC signal list for the SMI (station management interface).

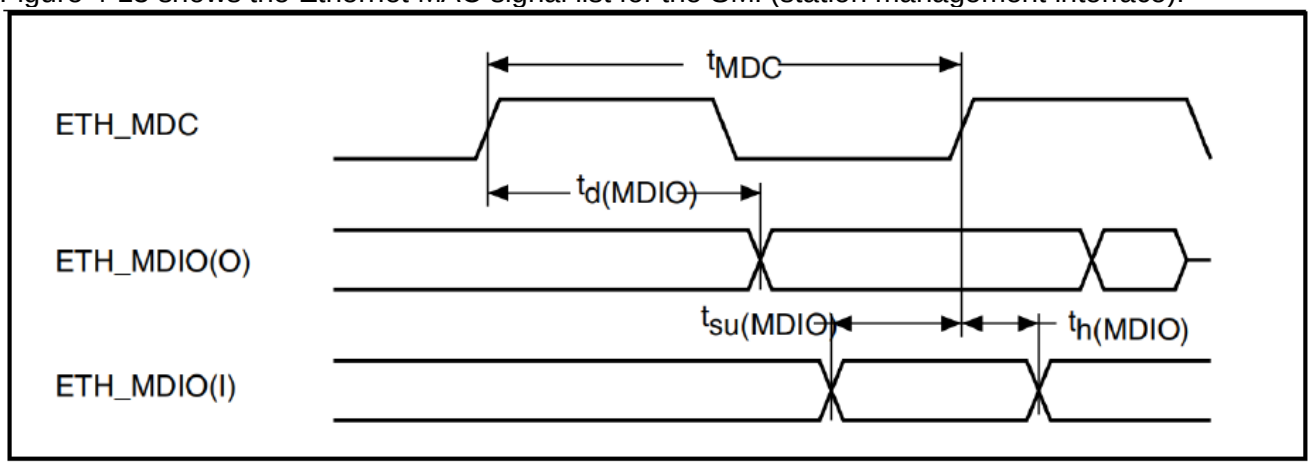


Figure 4-13 Ethernet Ethernet SMI timing diagram

Table 4-32 Dynamic characteristics: Dynamic characteristics: Ethernet MAC signal of SMI

symbol	parameter	Minimum	Typical Value	Maximum	unit
t_{MDC}	MDCCycle time(1.71 MHz, AHB = 72 MHz)	583	583.5	584	ns
$t_{d(MDIO)}$	MDIO Write data valid time	13.5	14.5	15.5	ns
$t_{su(MDIO)}$	Read data setup time	35	-	-	ns

$t_{h(MDIO)}$	Read data hold time	0	-	-	ns

Table 4-33 gives the Ethernet MAC signal list of RMII, and Figure 4-14 gives the Ethernet MAC signal list of RMII.

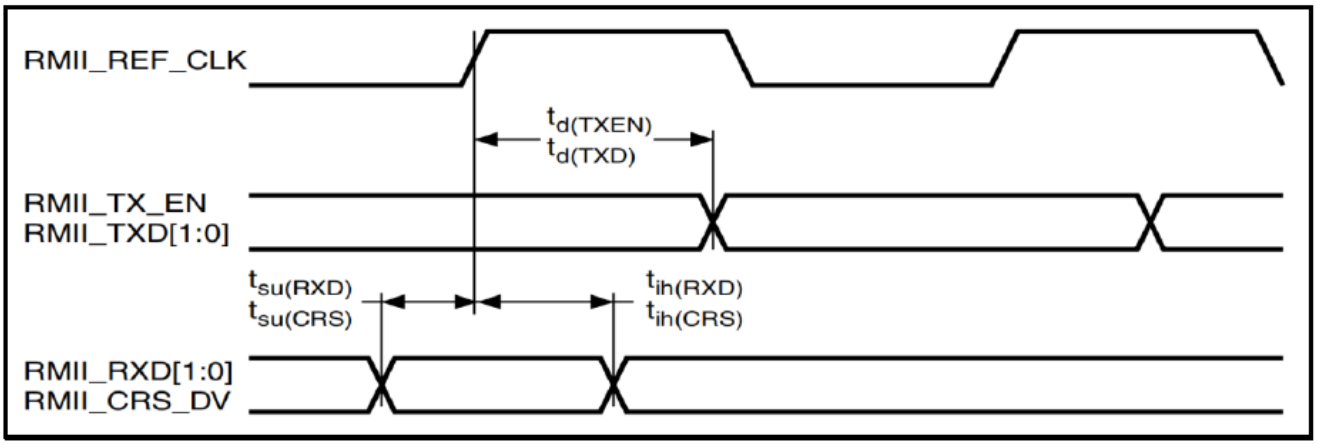


Figure 4-14 Ethernet Ethernet RMII timing diagram

Table 4-33 Dynamic characteristics: Dynamic characteristics: RMII Ethernet MAC signal

symbol	parameter	Minimum	Typical Value	Maximum	unit
$t_{su(RXD)}$	Receive data setup time	4	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2	-	-	ns
$t_{su(DV)}$	Carrier sense setup time	4	-	-	ns
$t_{ih(DV)}$	Carrier sense hold time	2	-	-	ns
$t_{d(TXEN)}$	Send enable valid delay time	8	10	16	ns

$t_{d(TXD)}$	Send data valid delay time	7	10	16	ns

Table 4-34 gives a list of Ethernet MAC signals for MII Ethernet. Figure 4-15 gives

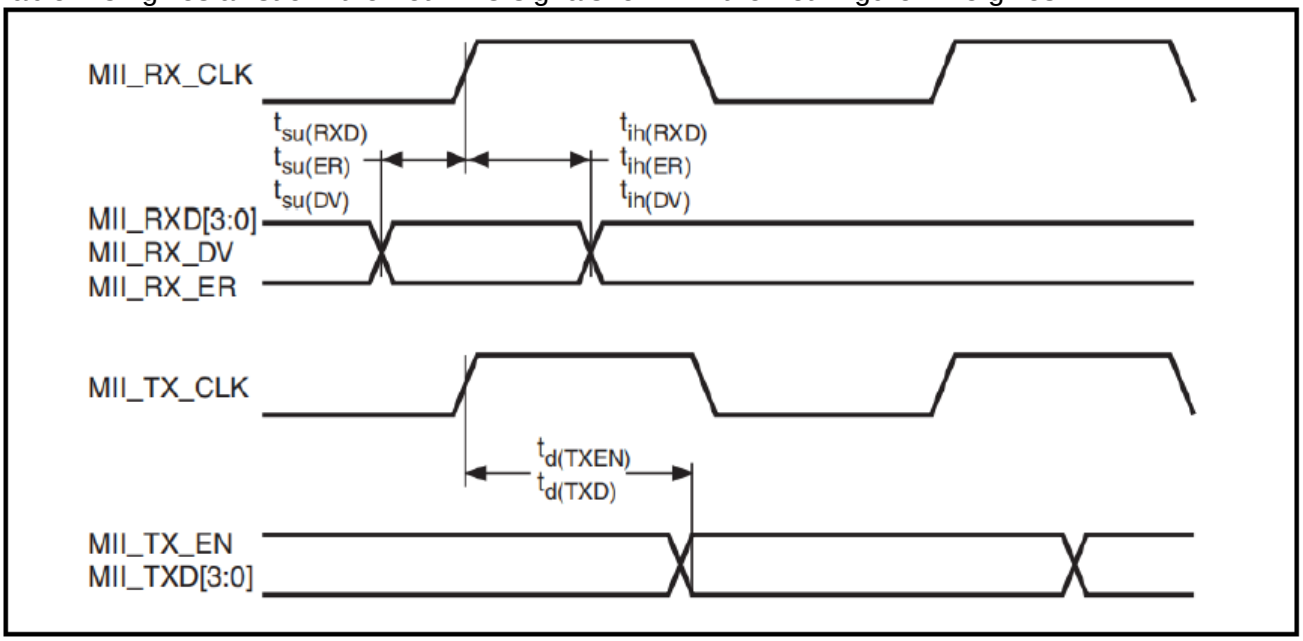


Figure 4-15 Ethernet Ethernet MII timing diagram Timing diagram

Table 4-34 Dynamic characteristics: Dynamic characteristics: Ethernet MAC signal of MII

symbol	parameter	Minimum	Typical Value	Maximum	unit
$t_{su(RXD)}$	Receive data setup time	10	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	10	-	-	ns
$t_{su(DV)}$	Data valid setup time	10	-	-	ns
$t_{ih(DV)}$	Data valid retention time	10	-	-	ns
$t_{su(ER)}$	Error settling time	10	-	-	ns

$t_{ih(ER)}$	Error holding time	10	-	-	ns
$t_{d(TXEN)}$	Send enable valid delay time	14	16	18	ns
$t_{d(TXD)}$	Send data valid delay time	13	16	20	ns

CAN (Local Area Network Controller) Interface Characteristics

For more detailed information about the input/output multiplexing function characteristics (CANTX and CANRX), refer to Section 4.2.10 I/O Current Injection Characteristics.

12-bit ADC Characteristics

Table 4-35 ADC Characteristics

characteristic	symbol	condition (Unless otherwise specified, V_{DD}=2.2V～5.5V ,-55℃≤T_A≤125℃)	Limit value		unit
			Minimum	maximum	unit
Supply voltage	V_{DDA}	V_{DD}≥V_{DDA}	2.4	5.5	V
Positive reference voltage	V_{REF+}	V_{DD}≥V_{DDA}	2.4	V_{DDA}	V
Differential nonlinearity error	*ED*	V_{DD}=V_{DDA}=3.3V,f_{ADC}=12MHz	-	±3	LSB
Integral nonlinearity error	*EL*	V_{DD}=V_{DDA}=3.3V,f_{ADC}=12MHz	-	±4	LSB
Gain Error	*EG*	V_{DD}=V_{DDA}=3.3V,f_{ADC}=14MHz	-	±4	LSB
Offset Error	*EO*	V_{DD}=V_{DDA}=3.3V,f_{ADC}=14MHz	-	±4	LSB

Signal-to-Noise Ratio	*SNR*	V_{DD}=V_{DDA}=3.3V,f_{ADC}=12MHz	60	-	dB
Total Harmonic Distortion	*THD*	V_{DD}=V_{DDA} =3.3V*F*in = 20kHz	-	-60	dB

DAC electrical characteristics

Table 4-36 DAC characteristics

characteristic	symbol	condition (Unless otherwise specified,V_{DD}=2.2V～5.5V ,-55℃≤T_A≤125℃)	Limit value		unit
			Minimum	maximum	
Analog supply voltage	V_{DDA}		2.2	5.5	V
Positive reference supply voltage	V_{REF+}	V_{REF+}≤V_{DDA}	2.2	VDDA	V
Differential nonlinearity error	*DNL*		-	±3	LSB
Integral nonlinearity error	*INL*		-	±3	LSB
Offset Error	*Offset*	V_{DDA}=V_{DD}= 3.3V,No load ,Output 0x800	-	±10	LSB
		V_{DDA}=V_{DD}= 3.3V,No load ,Output 0x000	-	±10	LSB
Gain Error	*Gain error*		-	±1.5	%

Temperature sensor characteristics

Table 4-37 TS characteristics

symbol	parameter	Minimum	Typical Value	Maximum	unit
T(1) L	V SENSELinearity with respect to temperature	-	±1	±2	℃
Avg_Slope (1)	Average slope	4.0	4.3	4.6	mV/℃
V (1)25	25℃Voltage at	1.34	1.43	1.52	V
t STAR (2)T	Startup time	4	-	10	μs
T(2)(3）S_temp	When reading the temperatureADC Sampling time		-	17.1	μs

1. Guaranteed by characterization results, not production tested.
2. Guaranteed by design, not production tested.
3. The minimum sampling time can be determined by the application through multiple iterations.

Package size

LQFP48 Package

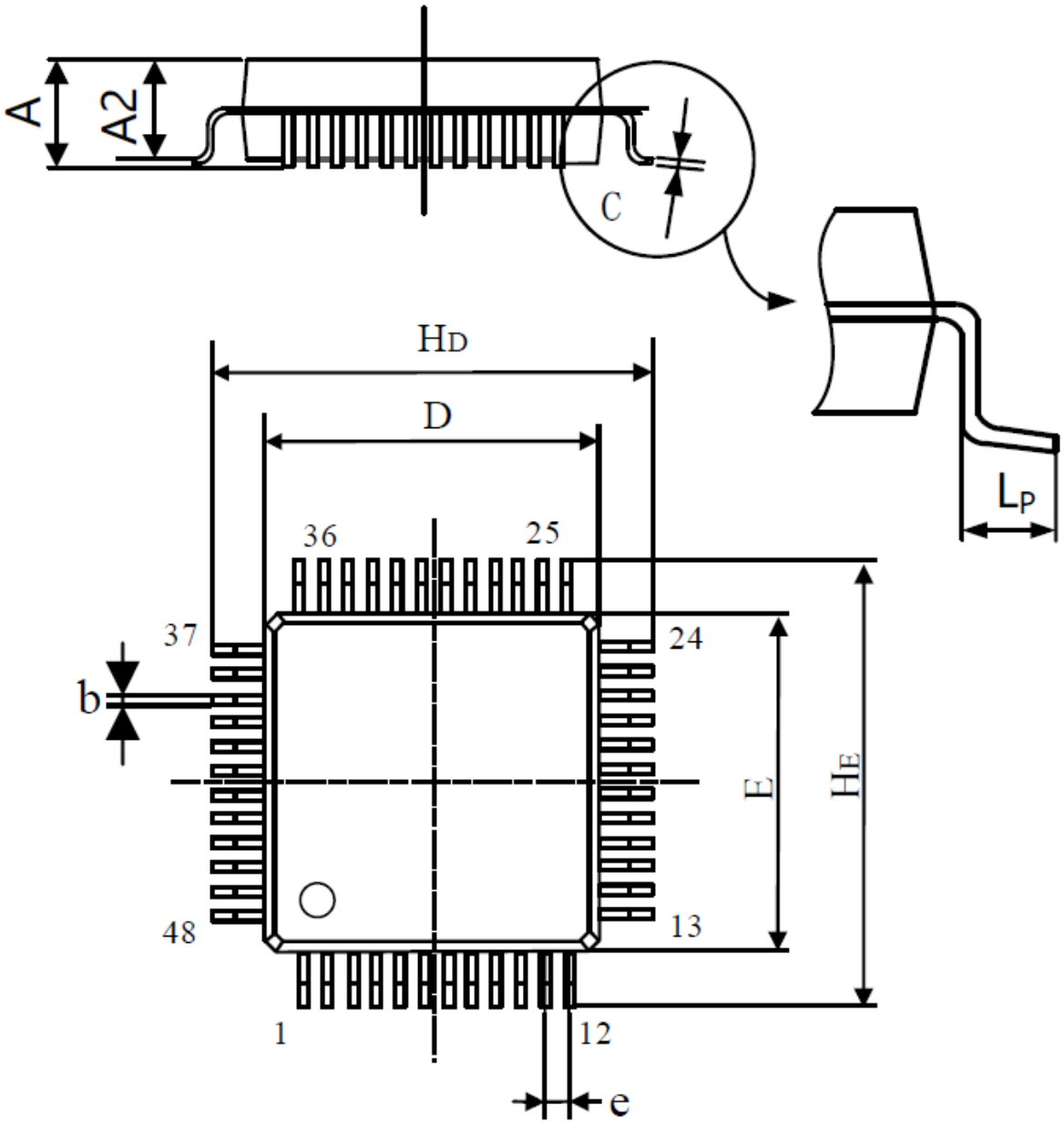


Figure 5-1 BST32F1 series LQFP48 package diagram

Table 5-1 BST32F1 series LQFP48 package size description

Dimension symbols		Numeric	
	Minimum	Typical Value	Maximum
A	-	-	1.80
A2	1.20	1.40	1.60
b	0.15	-	0.29

c	0.10	-	0.20
D	6.80	-	7.20
E	6.80	-	7.20
H_D	8.70	9.00	9.30
H_E	8.70	-	9.30
e	-	0.50	-
L_P	0.40	-	0.74

LQFP64 package

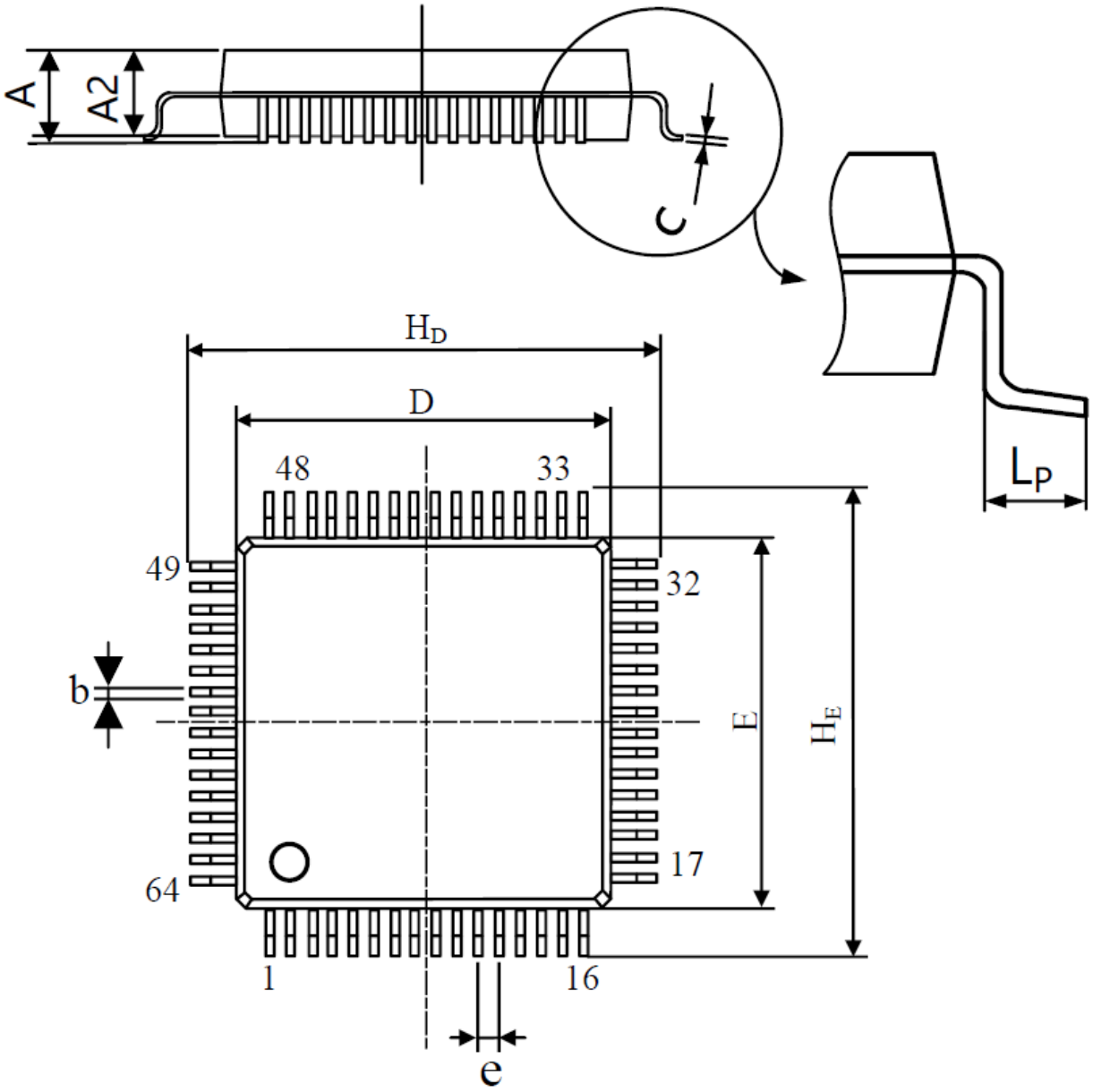


Figure 5-2 BST32F1 series LQFP64 package diagram
Table 5-2 BST32F1 series LQFP64 package size description

Unit is mm

Dimension symbols		Numeric	
	Minimum	Typical Value	Maximum
A	-	-	1.70
A2	1.25	-	1.55
b	0.14	-	0.30
c	0.10	-	0.20
D	9.80	-	10.20
E	9.80	-	10.20
e	-	0.50	-
H_D	11.70	-	12.30
H_E	11.70	-	12.30
L_P	0.40	-	0.80

LQFP100 package

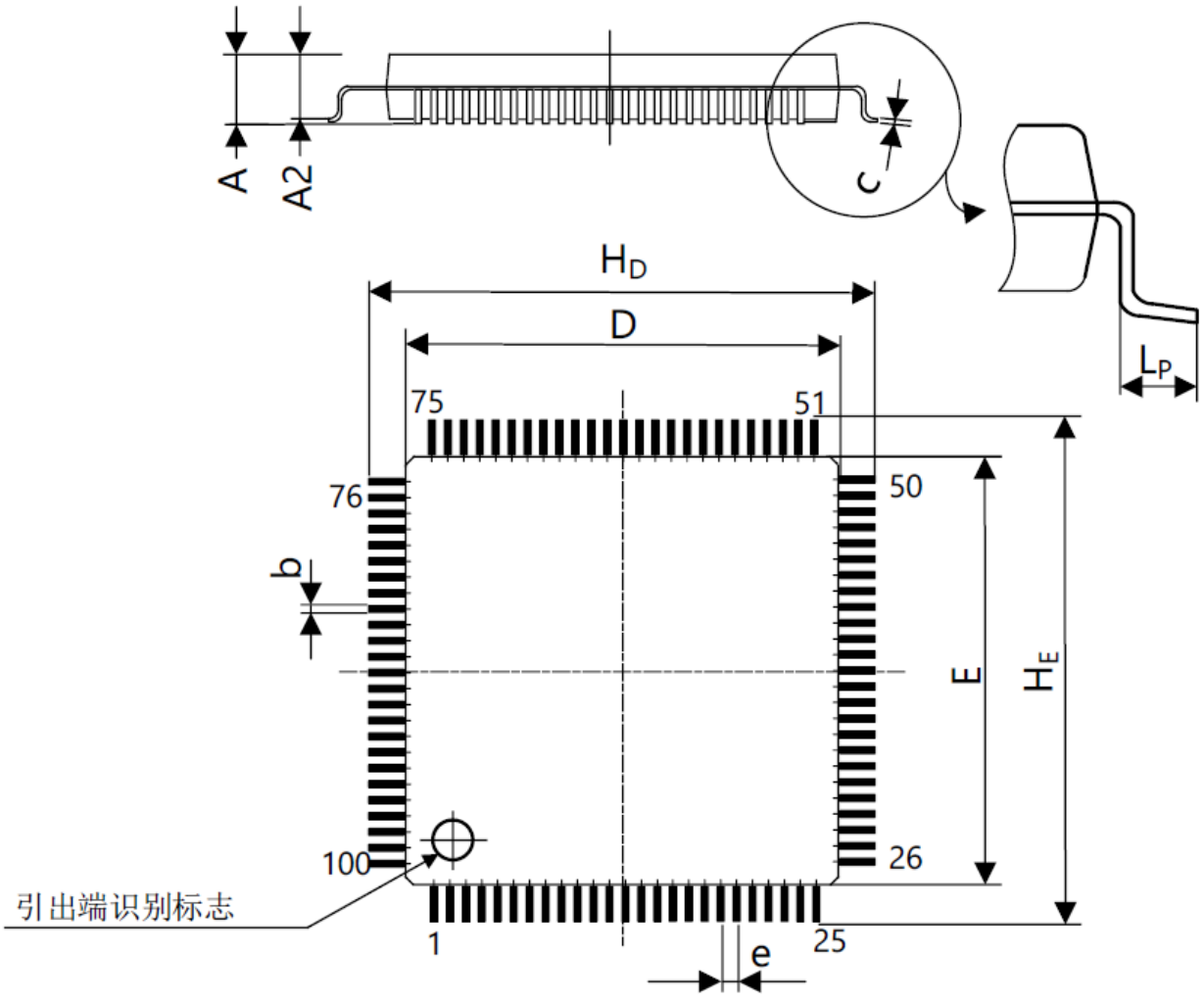


Figure 5-3 BST32F1 series LQFP100 package diagram

Table 5-3 BST32F1 series LQFP100 package size description

symbol	Value, unit: mm		
	Minimum	Nominal	Maximum
symbol		Value, unit: mm	
A	-	-	1.30
A2	0.85	-	1.15
D	13.80	-	14.20
E	13.80	-	14.20
H_D	15.70	-	16.30
H_E	15.70	-	16.30
e	-	0.50	-
b	0.140	-	0.30
c	0.06	-	0.23
L_P	0.40	-	0.80

PBGA100 Package

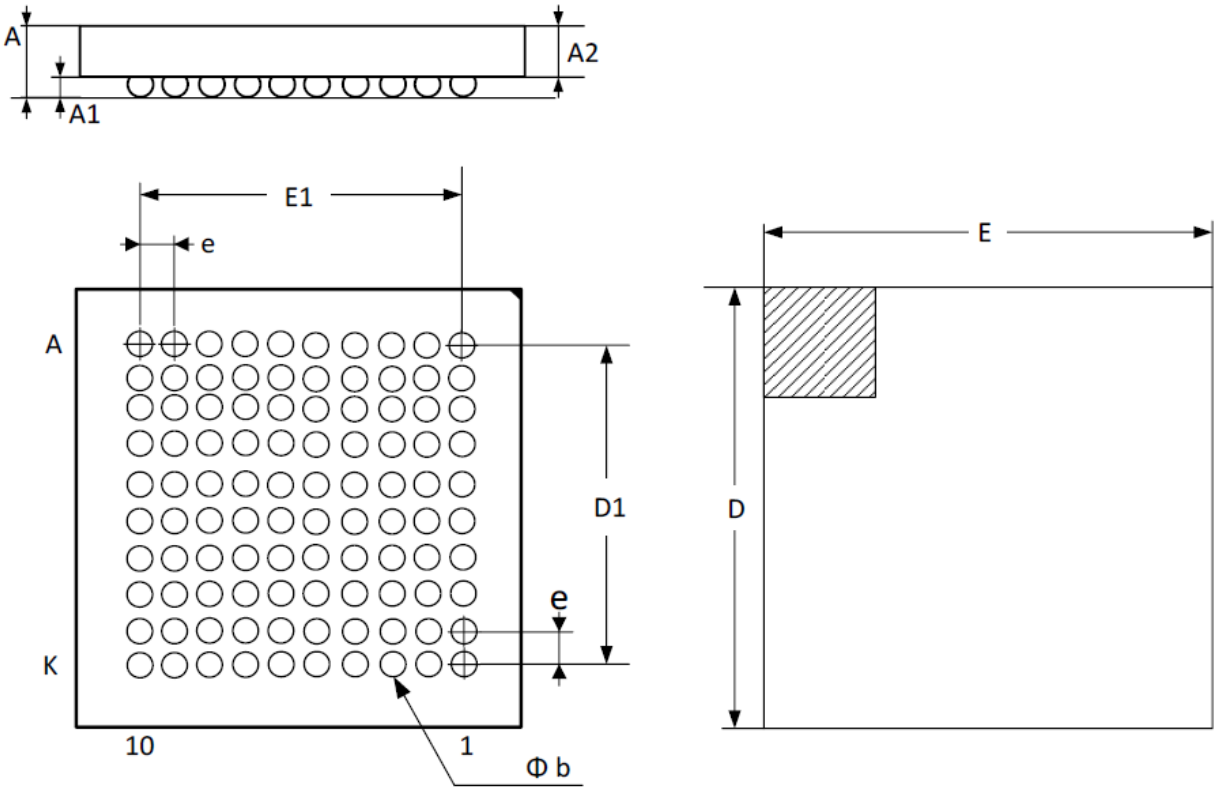


Figure 5-4 BST32F1 series BGA100 package diagram

Table 5-4 Package size description

Unit: mm

Dimension symbols	Numeric		
	Minimum	Typical Value	Maximum
A	-	-	1.48
A1	0.30	-	0.50
A2	0.72	-	1.10
D1	-	7.20	-
H_E	9.80	10.00	10.20
E1	-	7.20	-
e	-	0.80	-
Φb	0.40	-	0.60

LQFP144 Package

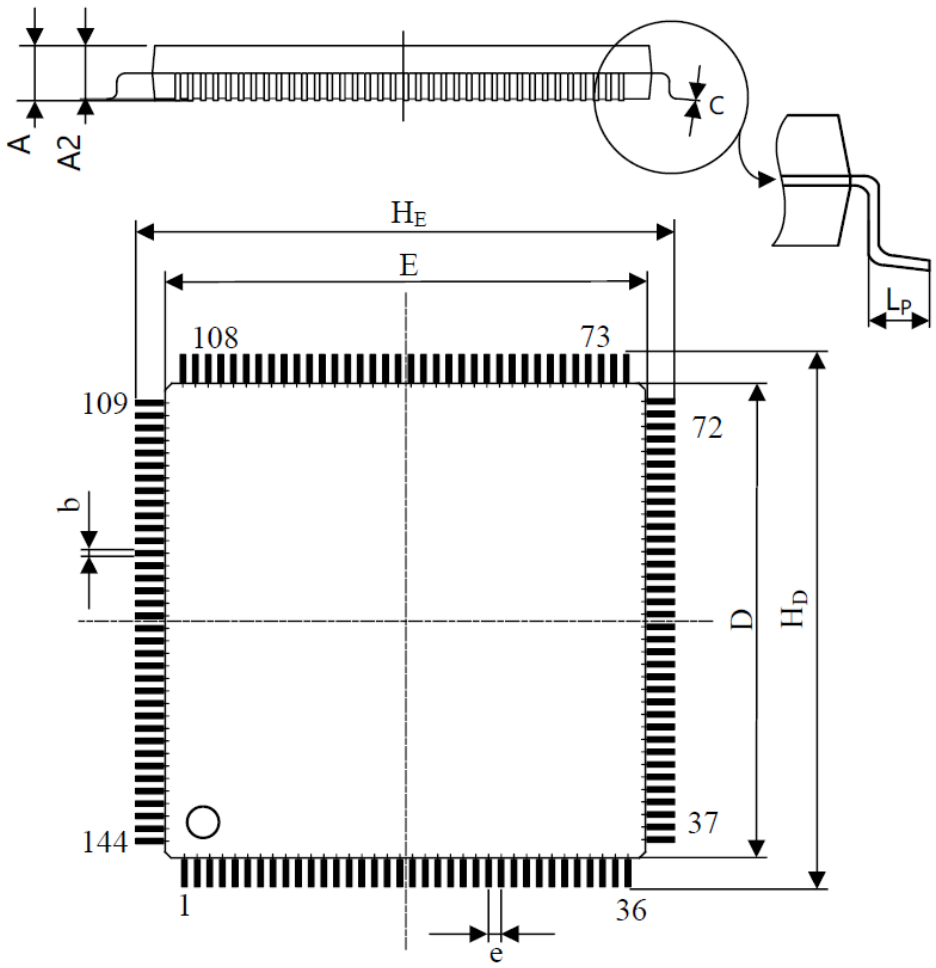


Figure 5-5 BST32F1 series LQFP144 package diagram
Table 5-5 BST32F1 series LQFP144 package size description

Dimension symbols		Value (mm)	
	Minimum	typical	maximum
A	-	-	1.70
A2	1.25	-	1.55
b	0.14	-	0.30
c	0.06	-	0.23
Dimension symbols		**Value (mm)**	
D	19.70	-	20.30
e	-	0.50	-
E	19.70	20.00	20.30
H_D	21.70	-	22.30
H_E	21.70	-	22.30
L_P	0.40	-	0.80

Ordering Information

Table 6-1 Product Ordering Information

Product Model	Package	MOQ	MPQ	Package	Operating temperature	grade
BST32F103-ALQFP48I	LQFP48	1	1	tray	-40°~85°	industry
BST32F103-ALQFP48E	LQFP48	1	1	tray	-55°~125°	Military Temperature
BST32F103-ALQFP64I	LQFP64	1	1	tray	-40°~85°	industry
BST32F103-ALQFP64E	LQFP64	1	1	tray	-55°~125°	Military Temperature
BST32F103-ALQFP64M3	LQFP64	1	1	tray	-55°~125°	N1
BST32F103-ALQFP100I	LQFP100	1	1	tray	-40°~85°	industry
BST32F103-ALQFP100E	LQFP100	1	1	tray	-55°~125°	Military Temperature

BST32F103-ALQFP100M3	LQFP100	1	1	tray	-55°~125°	N1
BST32F103-ALQFP144I	LQFP144	1	1	tray	-40°~85°	industry
BST32F103-ALQFP144E	LQFP144	1	1	tray	-55°~125°	Military Temperature
BST32F103-ALQFP144M3	LQFP144	1	1	tray	-55°~125°	N1
BST32F107PBGA100I	LQFP100	1	1	tray	-40°~85°	industry
BST32F107PBGA100E	PBGA100	1	1	tray	-40°~125°	Military Temperature
BST32F107PBGA100M3	PBGA100	1	1	tray	-55°~125°	N1

Supplementary information:

1. For the quality grade of M, N1, and E products, please contact the local market contact window
2. For ceramic seal series products, please contact the local sales for confirmation
3. For more F1 series products, please contact the local sales for consultation