BST3045

1. Product Overview

The BST3045 is a high-performance low-dropout linear regulated power supply that uses an ultra-low noise and ultra-high power supply rejection ratio (PSRR) architecture to power noise-sensitive signal acquisition and wireless communication applications. The BST3045 is designed as a high-performance current reference followed by a high-performance voltage buffer, which can be easily paralleled to further reduce noise, increase output current and improve heat dissipation on the PCB. The BST3045 can provide 500mA under a typical dropout voltage of 180mV. The typical value of the normal operating quiescent current is 3.1 mA, and it is less than 1μA in shutdown mode. The device adjusts the output voltage through off-chip resistors and can maintain unity gain operation over a wide output voltage range (1V to 15V), providing almost constant output noise, PSRR, bandwidth and load regulation, and these performances are independent of the output voltage. In addition, the regulated power supply also has programmable current limit, fast startup and a programmable power good signal to indicate output voltage regulation. The BST3045 device is encapsulated in a miniature DFN10 plastic package.

2. Product Features

- Ultra-low RMS noise: 2 μV $_{RMS.}$
- Ultra-low spot noise: 6 nV/√Hz (at 10kHz)
- Ultra-high PSRR: 62dB (at 2MHz).
- Output current : 500mA.
- Wide input voltage range: 2.6V to 20V.
- A single SET pin capacitor improves noise and PSRR.
- 100μA SET Pin Current: ±1% Initial Accuracy.
- A single SET pin resistor sets the output voltage.
- Programmable Current Limit.
- Low dropout voltage: 180mV.
- Output voltage range: 1V to 15V.
- Programmable power good.
- Quick start capability.
- High-precision enable/undervoltage lockout.
- Multiple devices can be paralleled to reduce noise and provide higher current.
- Second level of protection: internal current limiting.
- Minimum output capacitance: 10μF (ceramic).
- DFN10 plastic package.

3. Functional Block Diagram

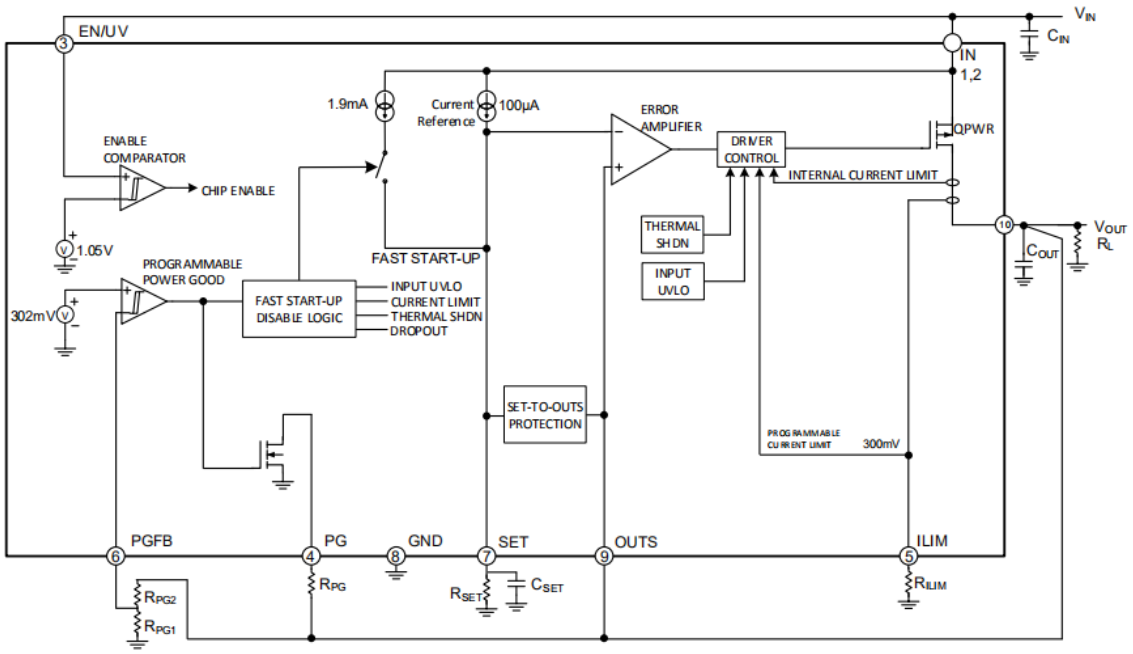


Figure 1. Functional Block Diagram

Pin Information

Pin Assignment Diagram

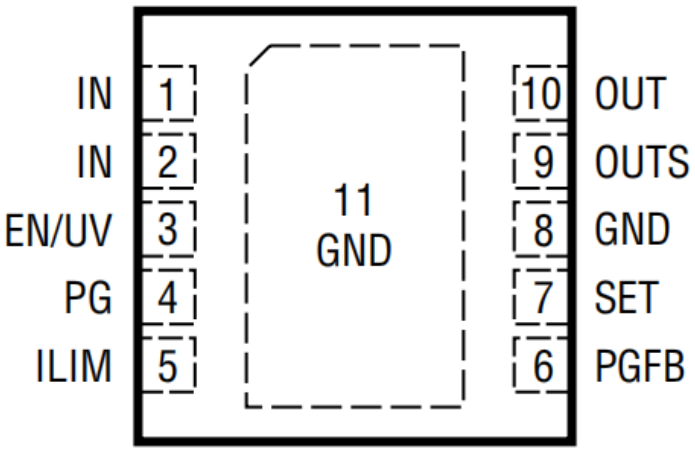


Figure 2. BST3045 pinout diagram

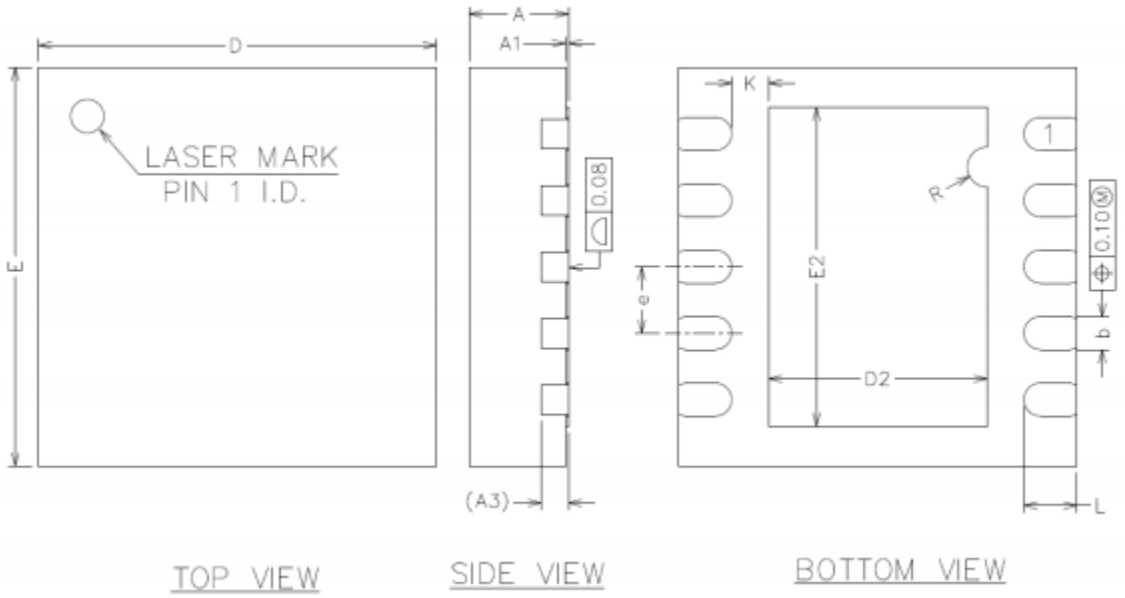
Pin Description

Table 1. Pin Description

Pins	Pin Name	Functional Description
1, 2	IN	Input. Regulator supply pin. The BST3045 requires a typical 4.7 µF bypass capacitor on the IN pin. Applications with higher input capacitance may require more input capacitance to prevent input supply droop.
3	EN/UV	Enable/ UVLO. Pulling the EN/UV pin of the BST3045 low puts the device in shutdown mode. The quiescent current in shutdown mode is less than 1 µA, and the output voltage is cut off. Alternatively, the EN/UV pin can set an input supply undervoltage lockout (UVLO) threshold using a resistor divider between IN, EN/UV, and GND. The BST3045 turns on when the EN/UV pin voltage exceeds 1.07 V on its rising edge and has a 100 mV hysteresis on its falling edge. Normal operation can be maintained with the EN/UV pin voltage above the input voltage. Connect EN/UV to IN when not used alone. Do not leave the EN/UV pin floating.
4	PG	Power Good. PG is an open-drain flag that indicates output voltage regulation. If PGFB is above 295 mV, PG is pulled high. If the power-good indicator function is not required, leave the PG pin floating.
5	ILIM	Current Limit Programming Pin. Connect a resistor from ILIM to GND to set the current limit. For best accuracy, use GND pin of the BST3045 using a Kelvin connection. The nominal value of the programmed scale factor is 278 mA·kΩ. The ILIM pin also acts as a current monitoring pin with a range of 0 V to 300 mV. If the programmable current limit function is not required, connect ILIM to GND.
6	PGFB	Power Good Feedback. If PGFB exceeds 295 mV on its rising edge and has 46 mV hysteresis on its falling edge, the PG pin is pulled high. Connecting an external resistor divider between the OUT, PGFB, and GND pins sets the programmable power good threshold using the following equation: 0.295 V (1 + R_{PG2} / R_{PG1}). PGFB is also responsible for activating the fast start circuitry. If the power good and fast start features are not required, connect PGFB to IN.
7	SET	Voltage Set. This pin is the inverting input of the error amplifier and the regulation set point of the BST3045. The SET pin provides a precise 100 µA current that flows through an external resistor connected between SET and GND. The output voltage is determined by VSET = ISET • RSET. The output voltage range is 1 V to 15 V. Adding a capacitor from SET to GND improves noise, PSRR, and transient response at the expense of increased startup time. For optimum load regulation, connect the ground end of the SET pin resistor directly to the load using a Kelvin connection.
8,11	GND	The exposed back side is an electrical connection to GND. To ensure proper electrical and thermal performance, the exposed back side should be soldered to the PCB ground and connected directly to the GND pin.
9	OUTS	Output Sense. This pin is the noninverting input to the error amplifier. For best transient performance and load regulation, connect OUTS directly to the output capacitor and the load using Kelvin connections. Also, connect the GND connections of the output capacitor and the SET pin capacitor directly together. In addition, the input and output capacitors (and their GND connections) should be placed very close together.
10	OUT	Output. This pin supplies power to the load. For stability, use a 10 µF (minimum) output capacitor with a low ESR of 50 mΩ and an ESL of less than 2 nH. Large load transients require a larger output capacitor to limit the peak voltage transient.

4. Product appearance

DFN package



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.20	0.25	0.30
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.60	1.65	1.80
E2	2.30	2.40	2.50
e	0.45	0.50	0.55
K	0.175	0.275	0.375
L	0.30	0.40	0.50
R		0.15REF	

Figure 2. Plastic DFN package dimensions

5. Electrical parameters

Unless otherwise noted, V_{IN} = max(V_{OUT} + 1V, 2.7 V), I_{OUT} = 10mA, C_{IN} = C_{OUT} = 10μF, T_J = -55 °C to +125 °C (for min./max. specifications), T_A = 25 °C (for typical specifications).

Table 2. Electrical properties

parameter	symbol	condition	Minimum	Typical Value	Maximum	unit
Minimum I N pin voltage	*V IN _UVLO*	*I LOAD* =10mA, *V IN UVLO* rises		2.4	2.55	V
		V IN UVLO Hysteresis		100		mV
SET Pin Current	*I SET*	*V IN* =4V, *I LOAD* = 1mA, *V OUT* = 3V	99	100	101	μA
		2.7V< *V IN* <20V, 1V< *V OUT* <15V, 1mA < *I LOAD* < 500mA (Note 1)	98	100	102	μA
Quick Start SET Pin Current		*V PGFB* =289mV, *V IN* = 4V, *V SET* = 3V		3.9		mA
Output offset voltage (Note 2)	*V OS*	*V IN* =4V, *I LOAD* = 1mA, *V OUT* = 3V	-3		3	mV
		2.7V< *V IN* <20V, 1V< *V OUT* <15V, 1mA < *I LOAD* < 500mA (Note 1)	-6		8	mV
Voltage Regulation: ΔI SET	*Line_ISET*	*V IN* =2.7V to 20V, *I LOAD* =1mA, *V OUT* =1.8V		5	50	nA/V
Voltage Regulation: ΔV OS	*Line_Vos*	*V IN* =2.7V to 20V, *I LOAD* =1mA, *V OUT* =1.8V (Note 2)		3	50	μV/V
Load Regulation: ΔI SET	*Load_ISET*	*I LOAD* =1mA to 500mA, *V IN* =4V, *V OUT* =3V		0.15	1.5	nA/mA
Load Regulation: ΔV OS	*Load_Vos*	*I LOAD* =1mA to 500mA, *V IN* =4V, *V OUT* =3V (Note 2)		0.7	8	mV
I SET changes with V SET	*ISET_VSET*	*V SET* =1V to 15V, *V IN* =16V, *I LOAD* = 1mA		350	700	nA
V OS changes with V SET	*Vos _VSET*	*V SET* =1.5V to 15V, *V IN* =16V, *I LOAD* = 1mA (Note 2)		1.8	8	mV
Quiescent Current V IN = V OUT (NOMINAL)	*Q*	*ILOAD = 10μA*		3.1		mA
		I LOAD =1mA		3.6		mA
		I LOAD =50mA		4.1		mA
		I LOAD =100mA		5.9		mA
		I LOAD =500mA		7.9		mA
Dropout voltage	*V D*	*I LOAD* =50mA		172	260	mV
		I LOAD =300mA (Note 3)		176	268	mV
		I LOAD =500mA (Note 3)		179	270	mV
Output noise spectrum density		*I LOAD* =500mA, frequency = 10Hz, *COUT = 10μF, CSET* = 4.7μF, 1V ≤ V_{OUT} ≤ 15V		99		nV/√Hz
		ILOAD = 500mA, frequency = *10k* Hz, *COUT = 10μF, CSET* = 4.7μF, 1V ≤ V_{OUT} ≤ 15V		6		nV/√Hz
Output RMS Noise (Note 2, 4)	*OUT NOISE*	*I LOAD* =500mA, *BW* =10Hz to 100kHz, COUT = 10μF, *C SET* = 0.47μF		5		μV RMS
		I LOAD =500mA, *BW* =10Hz to 100kHz, *COUT* = 10μF, *C SET* = 4.7μF		2		μV RMS
Supply voltage ripple rejection 1.5V ≤ V_{OUT} ≤ 15V (Note 2, 4)	*P SSR*	*V RIPPLE* = 500mV PP, *f RIPPLE* = 120Hz, *I LOAD* =500mA, *C OUT* = 10 μF, *C SET* = 4.7 μF		92		dB
		V RIPPLE = 150 mV PP, *f RIPPLE* = 10 k Hz, *I LOAD* =200mA, *C OUT* = 10 μF, *C SET* = 4.7 μF		9 3		dB

parameter	symbol	condition	Minimum	Typical Value	Maximum	unit
EN/UV Pin Threshold	*EN_UVLO*	EN/UV Threshold Rising (Turn On), VIN = 4V	1.04	1.07	1.1	V
EN/UV Pin Hysteresis	*EN _HYS*	*EN/UV* Threshold Hysteresis, V_{IN} = 4V		100		mV
EN/UV Pin Current	*IEN*	$V_{EN/UV}$ = 0V, *V* = 20V			1.5	μA
		$V_{EN/UV}$ = 1.24V, *V* = 20V		127	300	nA
		$V_{EN/UV}$ = 20V, *V* = 0V		0.03	2	μA
Quiescent current in shutdown mode (VEN/UV = 0V)	I_{SD}	V_{IN} =4V		0.5	4	μA
					10	μA
Internal Current Limit	I_{LIMIT}			1300		mA
Programmable Current Limit		Programming scale factor: 2.6V < V_{IN} < 20V (Note 6)		278		mA • kΩ
		V_{IN} =4V, V_{OUT} =0V, *RILIM* =649 Ω		428		mA
		V_{IN} =4V, V_{OUT} =0V, *RILIM* =2.55 kΩ		109		mA
PGFB Threshold	*PGFB_UVLO*	*PGFB* threshold rises		295		mV
PGFB Hysteresis	*PGFB_HYS*	*PGFB* Threshold Hysteresis		4 6		mV
PGFB Pin Current	I_{PGFB}	V_{IN} =4V, *VGFB* =300mV		3		nA
PG output low voltage	V_{PG}	*IPG = 100μA*		14	70	mV
PG leakage current	I_{PG}	*VPG = 20V*			1	μA
Thermal shutdown	TS_{SD}	T_J Rise		152		°C
		Hysteresis		15		°C
Startup time	T_{START_UP}	*VOUT* =5V, I_{LOAD} = 500mA, C_{SET} = 0.47μF, V_{IN} = 6V, V_{PGFB} = 6V		55		ms
		VOUT =5V, I_{LOAD} = 500mA, C_{SET} = 4.7μF, V_{IN} = 6V, V_{PGFB} = 6V		550		ms
		VOUT =5V, I_{LOAD} = 500mA, C_{SET} = 4.7μF, V_{IN} = 6V, R_{PG_BOT} = 47.5 kΩ, R_{PG_TOP} = 700 kΩ		7		ms

Note 1: Maximum junction temperature limits operating conditions. Stable output voltage specifications do not apply to all possible input voltage and output current combinations. If operating at maximum output current, the input voltage range is limited. If operating at maximum input voltage, the output current range is limited.

Note 2: OUTS is directly connected to OUT.

Note 3: Dropout voltage is the minimum input-output voltage difference required to maintain regulation at a specified output current. The dropout voltage is measured when the output is 1% out of regulation. This definition will produce a higher dropout voltage than the hard dropout voltage measured at VIN = VOUT (NOMINAL). The maximum dropout voltage specifications at 100mA and 500mA are not guaranteed due to production test limitations caused by Kelvin detection of the package pins.

Note 4: Adding a capacitor across the SET pin resistor reduces the output voltage noise. Adding this capacitor bypasses the thermal noise of the SET pin resistor and the noise of the reference current. The output noise is then equal to the error amplifier noise. Using a SET pin bypass capacitor also increases the startup time.