BST3042

1. Product Overview

BST3042 is a high-performance low-dropout linear regulated power supply. Its ultra-low noise and ultra-high power supply rejection ratio (PSRR) architecture is used to power noise-sensitive signal acquisition and wireless communication applications. BST3042 is designed as a high-performance current reference followed by a high-performance voltage buffer, which can be easily connected in parallel to further reduce noise, increase output current and improve heat dissipation on the PCB. BST3042 can provide 200mA under a typical dropout voltage of 353mV. The typical value of the quiescent current in normal operation is 1.9mA, and it is less than 1μA in shutdown mode. The device adjusts the output voltage through off-chip resistors and can maintain unity gain operation over a wide output voltage range (1.5V to 15V), thereby providing almost constant output noise, PSRR, bandwidth and load regulation, and these performances are independent of the output voltage. In addition, the regulated power supply also has programmable current limit, fast startup and a programmable power good signal to indicate output voltage regulation.
The BST3042 device is packaged in a miniature DFN10 plastic package.

2. Product Features

- Ultra-low RMS noise: 1.2 μV RMS.
- Ultra-low spot noise: 2.8nV/√Hz (at 10kHz)
- Ultra-high PSRR: 80dB (at 1MHz).
- Output current: 200mA.
- Wide input voltage range: 2.6V to 20V.
- A single SET pin capacitor improves noise and PSRR.
- 100μA SET Pin Current: ±1% Initial Accuracy.
- A single SET pin resistor sets the output voltage.
- Programmable Current Limit.
- Low dropout voltage: 353mV.
- Output voltage range: 1.5V to 15V.
- Programmable power good.
- Quick start capability.
- High-precision enable/undervoltage lockout.
- Multiple devices can be paralleled to reduce noise and provide higher current.
- Second level of protection: internal current limiting.
- Minimum output capacitance: 4.7μF (ceramic).
- DFN10 plastic package.

3. Functional Block Diagram

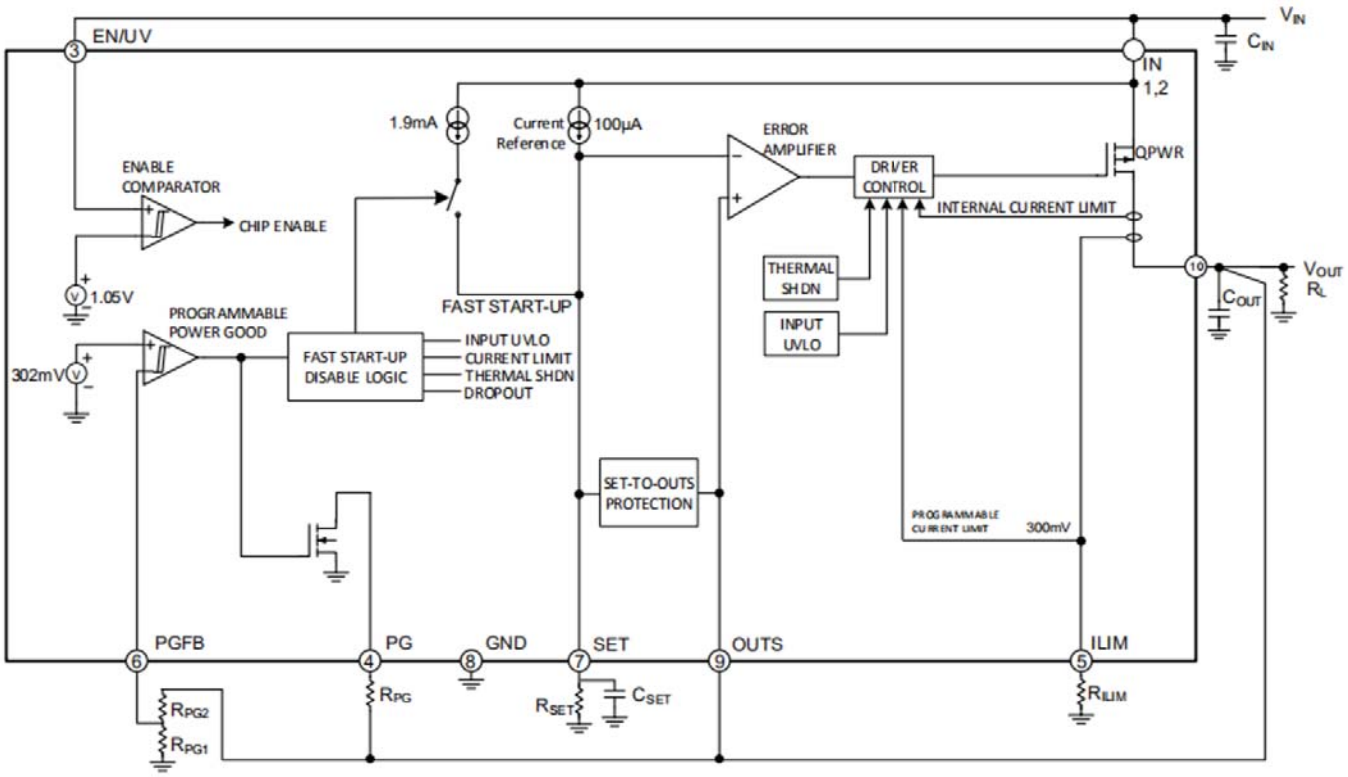

Figure 1. Functional Block Diagram

Pin Information

Pin Assignment Diagram

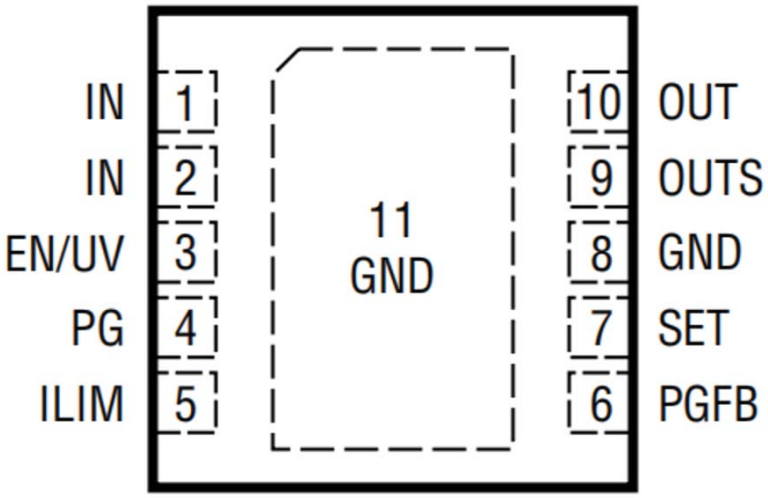

Figure 2. BST3042 pinout diagram

Table 1. Pin Description

Pins	Pin Name	Functional Description
1, 2	IN	Input. Regulator supply pin. The BST3042 requires a typical 4.7 μF bypass capacitor on the IN pin. Applications with higher input capacitance may require more input capacitance to prevent input supply droop.
3	EN/UV	Enable/ UVLO. Pulling the EN/UV pin of the BST3042 low puts the device in shutdown mode. The quiescent current in shutdown mode is less than 1 μA, and the output voltage is cut off. Alternatively, the EN/UV pin can also set an input supply undervoltage lockout (UVLO) threshold using a resistor divider between IN, EN/UV, and GND. The BST3042 turns on when the EN/UV pin voltage exceeds 1.05 V on its rising edge and has a 100 mV hysteresis on its falling edge. Normal operation can be maintained with the EN/UV pin voltage above the input voltage. Connect EN/UV to IN when not used alone. Do not leave the EN/UV pin floating.
4	PG	Power Good. PG is an open-drain flag that indicates output voltage regulation. If PGFB is above 302 mV, PG is pulled high. If the power-good indicator function is not required, leave the PG pin floating.
5	ILIM	Current Limit Programming Pin. Connect a resistor from ILIM to GND to set the current limit. For best accuracy, use GND pin of the BST3042 using a Kelvin connection. The nominal value of the programmed scale factor is 128 mA·kΩ. The ILIM pin also acts as a current monitoring pin with a range of 0 V to 300 mV. If the programmable current limit function is not required, connect ILIM to GND.
6	PGFB	Power Good Feedback. If PGFB exceeds 302 mV on its rising edge and has 60 mV hysteresis on its falling edge, the PG pin is pulled high. Connecting an external resistor divider between the OUT, PGFB, and GND pins sets the programmable power good threshold using the following equation: 0.302 V (1 + R PG2 / R PG1). PGFB is also responsible for activating the fast start circuit. If the power good and fast start features are not required, connect PGFB to IN.
7	SET	Voltage Set. This pin is the inverting input of the error amplifier and the regulation set point of the BST3042. The SET pin provides a precise 100 μA current that flows through an external resistor connected between SET and GND. The output voltage is determined by VSET = ISET • RSET. The output voltage range is 1.5 V to 15 V. Adding a capacitor from SET to GND improves noise, PSRR, and transient response at the expense of increased startup time. For optimum load regulation, connect the ground end of the SET pin resistor directly to the load using a Kelvin connection.
8,11	GND	The exposed back side is an electrical connection to GND. To ensure proper electrical and thermal performance, the exposed back side should be soldered to the PCB ground and connected directly to the GND pin.
9	OUTS	Output Sense. This pin is the noninverting input to the error amplifier. For best transient performance and load regulation, connect OUTS directly to the output capacitor and the load using Kelvin connections. Also, connect the GND connections of the output capacitor and the SET pin capacitor directly together. In addition, the input and output capacitors (and their GND connections) should be placed very close together.
10	OUT	Output. This pin supplies power to the load. For stability, use a 4.7 μF (minimum) output capacitor with a low ESR of 50 mΩ and an ESL of less than 2 nH. Large load transients require a larger output capacitor to limit the peak voltage transient.

4. Product appearance

DFN package

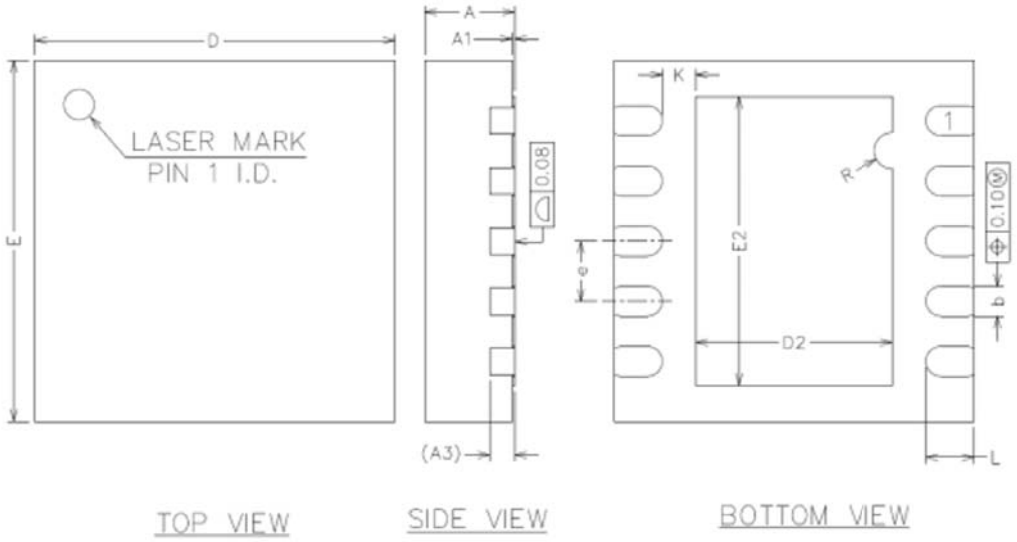

Figure 3. Plastic DFN package dimensions

5. Electrical parameters

Unless otherwise noted, V_{IN} = max(V_{OUT} + 1V, 2.7 V), I_{OUT} = 10mA, C_{IN} =C_{OUT} = 4.7μF, T_J = -55 °C to +125 °C (for min./max. specifications), T_A = 25 °C (for typical specifications).

Table 2. Electrical properties

parameter	symbol	condition	Minimum	Typical Value	Maximum	unit
Voltage Regulation	$\Delta_{V\,OS}$	V_{IN} =2.7V to 20V, I_{LOAD} =1mA, V_{OUT} =1.8V		2	twenty one	μV/V
Load Regulation	ΔI_{SET}	I_{LOAD} =1mA to 200mA, V_{IN} =4V, V_{OUT} =3V		0.8	5	nA/mA
Load Regulation	ΔV_{OS}	I_{LOAD} =1mA to 200mA, V_{IN} =4V, V_{OUT} =3V		0.1	1.6	mV
I_{SET} changes with V_{SET}		V_{SET} =1.5V to 15V, V_{IN} =16V, I_{LOAD} = 1mA		100		nA
V OS changes with V_{SET}		V_{SET} =1.5V to 15V, V_{IN} =16V, I_{LOAD} = 1mA		0.7	8	mV
Quiescent Current V IN = V_{OUT} (NOMINAL)	Q	I_{LOAD} = 10μA		1.9	2.5	mA
		I_{LOAD} =1mA		2.1	2.6	mA
		I_{LOAD} =50mA		2.5	3.2	mA
		I_{LOAD} =100mA		2.9	3.5	mA
		I_{LOAD} =200mA		3.6	5	mA
Dropout voltage		I_{LOAD} =1mA		3 42	3 85	mV
		I_{LOAD} =50mA		3 44	3 89	mV
		I_{LOAD} =100mA		3 47	3 93	mV
		I_{LOAD} =200mA		3 53	3 98	mV
Output noise spectrum Density		I_{LOAD} =200mA, frequency = 10Hz, COUT = 4.7μF, CSET = 4.7μF, 1.5V ≤ V_{OUT} ≤ 15V		1 12		nV/√Hz
		I_{LOAD} = 200mA, frequency = 10k Hz, C_{OUT} = 4.7μF, CSET = 4.7μF, 1.5V ≤ V_{OUT} ≤ 15V		2.8		nV/√Hz
Output RMS Noise		I_{LOAD} =200mA, BW =10Hz to 100kHz, C_{OUT} = 4.7μF, C_{SET} = 0.47μF		2.25		μV RMS
		I_{LOAD} =200mA, BW =10Hz, to 100kHz, C_{OUT} = 4.7μF, C_{SET} = 4.7μF		1.2		μV RMS
Supply voltage $_{RIPPLE}$ rejection 1.5V ≤ VOUT ≤ 15V		V_{RIPPLE} = 500mV PP, f_{RIPPLE} = 120Hz, I_{LOAD} =200mA, C_{OUT} = 4.7 μF, C_{SET} = 4.7 μF		8 7		dB
		V_{RIPPLE} = 150 mV PP, f_{RIPPLE} = 10 k Hz, I_{LOAD} =200mA, C_{OUT} = 4.7 μF, C_{SET} = 4.7 μF		9 2		dB
EN/UV Pin Threshold		EN/UV Threshold Rising (Turn On), V_{IN} = 4V	1.046	1.05	1.068	V
EN/UV Pin Hysteresis		EN/UV Threshold Hysteresis, V_{IN} = 4V		1 00		mV
EN/UV Pin Current		$V_{EN/UV}$ = 0V, V = 20V			1.5	μA
		$V_{EN/UV}$ = 1.24V, V = 20V		0.1	2	μA
		$V_{EN/UV}$ = 20V, V = 0V		0.01	0.4	μA
Quiescent current in shutdown mode (VEN/UV = 0V)		V_{IN} =4V		0.4	10	μA
					10	μA

Table 2. Electrical properties

parameter	symbol	condition	Minimum	Typical Value	Maximum	unit
Internal Current Limit			200	400	600	mA
Programmable Current Limit		Programming scale factor: 2.6V < V_{IN} < 20V		128		mA · kΩ
		V_{IN} =4V, V_{OUT} =0V, RILIM =649 Ω		197		mA
		V_{IN} =4V, V_{OUT} =0V, RILIM =2.55 kΩ		50		mA
PGFB Threshold		PGFB threshold rises	2 92	3 04	3 16	mV
PGFB Hysteresis		PGFB Threshold Hysteresis		4 6		mV
PGFB Pin Current		V_{IN} =4V, VGFB =300mV		3		nA
PG $_{OUT}$put low voltage		IPG = 100μA		16	70	mV
PG leakage current		VPG = 20V			0.5	μA
Thermal shutdown		T J Rise		160		°C
		Hysteresis		15		°C
Startup time		V_{OUT} =5V, I_{LOAD} = 200mA, C_{SET} = 0.47μF, V_{IN} = 6V, V_{PGFB} = 6V		55		ms
		V_{OUT} =5V, I_{LOAD} = 200mA, C_{SET} = 4.7μF, V_{IN} = 6V, V_{PGFB} = 6V		550		ms
		V_{OUT} =5V, I_{LOAD} = 200mA, C_{SET} = 4.7μF, V_{IN} = 6V, R_{PG1} =50kΩ		10		ms